

STEREO CASSETTE DECK

MODEL NO. AD-3800H, E, K, G

AIWA®
(SERVICE MANUAL)

Code No. 04-380-000-53



DATE OF ISSUE 10/1981

SPECIFICATIONS

Semiconductors:	22 ICs, 125 transistors, 103 diodes, 50 LED's	(WTD-A)	More than 58/64 dB (METAL, DOLBY NR B-type/C-type)
Power supply:	H model AC 120V/220V/240V switchable 50/60 Hz E model AC 220V, 50/60 Hz K model AC 240V, 50/60 Hz G model AC 240V, 50/60 Hz		More than 58/64 dB (CrO ₂ , DOLBY NR B-type/C-type)
Power consumption:	24W		More than 54/62 dB
Dimensions:	420(W) x 110(H) x 265(D) mm		More than 58/64 dB (FeCr, DOLBY NR B-type/C-type)
Weight:	5.1kg		(LH, DOLBY NR B-type/C-type)
Track type:	4 tracks 2 channels		More than 30 dB
Tape speed:	4.8 cm/s ± 1.5%		
Wow and flutter:	Less than 0.025% (WRMS)		
Automatic stop system:	Full auto stop		
Automatic shut-off action time:	Less than 5s.		
Pinch roller pressure:	Take up 350 ⁺³⁰ ₋₂₀ g (3.43 ^{+0.294} _{-0.196} N) Supply 180 ⁺³⁰ ₋₂₀ g (1.764 ^{+0.294} _{-0.196} N)	Motor: Head: Inputs:	85 kHz METAL 20 ~ 20,000 Hz CrO ₂ 20 ~ 19,000 Hz FeCr 20 ~ 20,000 Hz LH 20 ~ 17,000 Hz DC EG motor DX head (for Rec/Pb) Ferrite head (for Erase) MIC max. sensitivity 0.3 mV (200Ω~10kΩ suitable) LINE IN max. sensitivity 50 mV (Optimum load impedance more than 50 kΩ)
Take-up torque:	50 ± 10g-cm (0.49 ± 0.098m N.m)		
FF & rewind torque:	150 ⁺⁵⁰ ₋₃₀ g-cm (1.47 ^{+0.49} _{-0.294} m N.m)		
FF & rewind time:	70 ± 10s. (C-60)		
Playback output: (TTA-161)	706 ± 50 mV		
Playback noise:	120μS/70μS Less than 2.7/2.0mV (DOLBY NR OFF) Less than 1.7/1.6 mV (DOLBY NR B type) Less than 1.5/1.4mV (DOLBY NR C type)		
Rec./Pb distortion:	Less than 1% (METAL) Less than (CrO ₂) Less than 1% (FeCr) Less than 1.3% (LH)		
Rec./Pb SN ratio: (Unweighted)	More than 45/49 dB (METAL, DOLBY NR B-type OFF/ON) More than 45/49 dB (CrO ₂ , DOLBY NR B-type OFF/ON) More than 45/49 dB (FeCr, DOLBY NR B-type OFF/ON)		
			<ul style="list-style-type: none"> • Specifications and external appearance are subject to change without due to product improvement. • Noise reduction system manufactured under license from Dolby Laboratories Licensing Corporation. • Dolby and the  symbol are trademarks of Dolby Laboratories Licensing Corporation.

DISASSEMBLY INSTRUCTIONS

1. Removing the Cabinet, Steel

1) Remove 6 screws. (See figure 1)

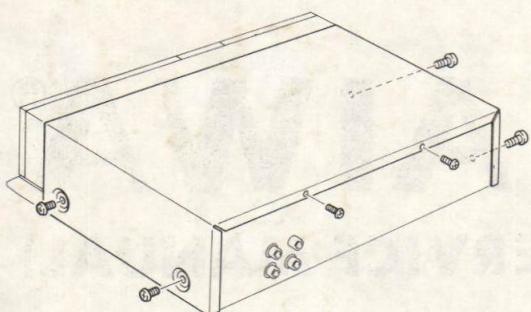


Fig. 1

3) Remove 8 screws. (See figure 4)

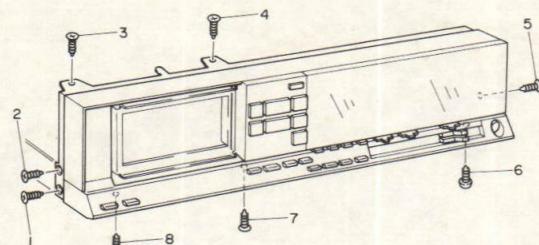


Fig. 4

2. Removing the Front, Panel

1) After depress eject button to open cassette box, pull cassette lid to remove in the direction of arrow.
(See figure 2)

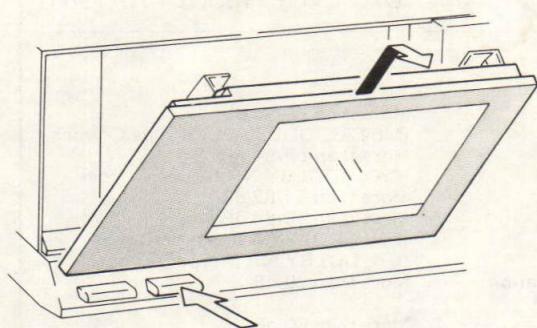


Fig. 2

2) Remove 2 screws to take off cassette plate.
(See figure 3)

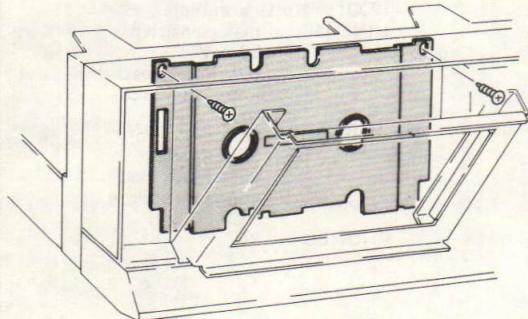


Fig. 3

3. Removing the Mechanism

1) Remove 2 screws. (See figure 5)

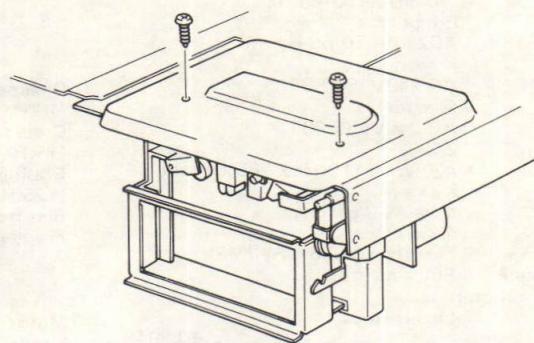
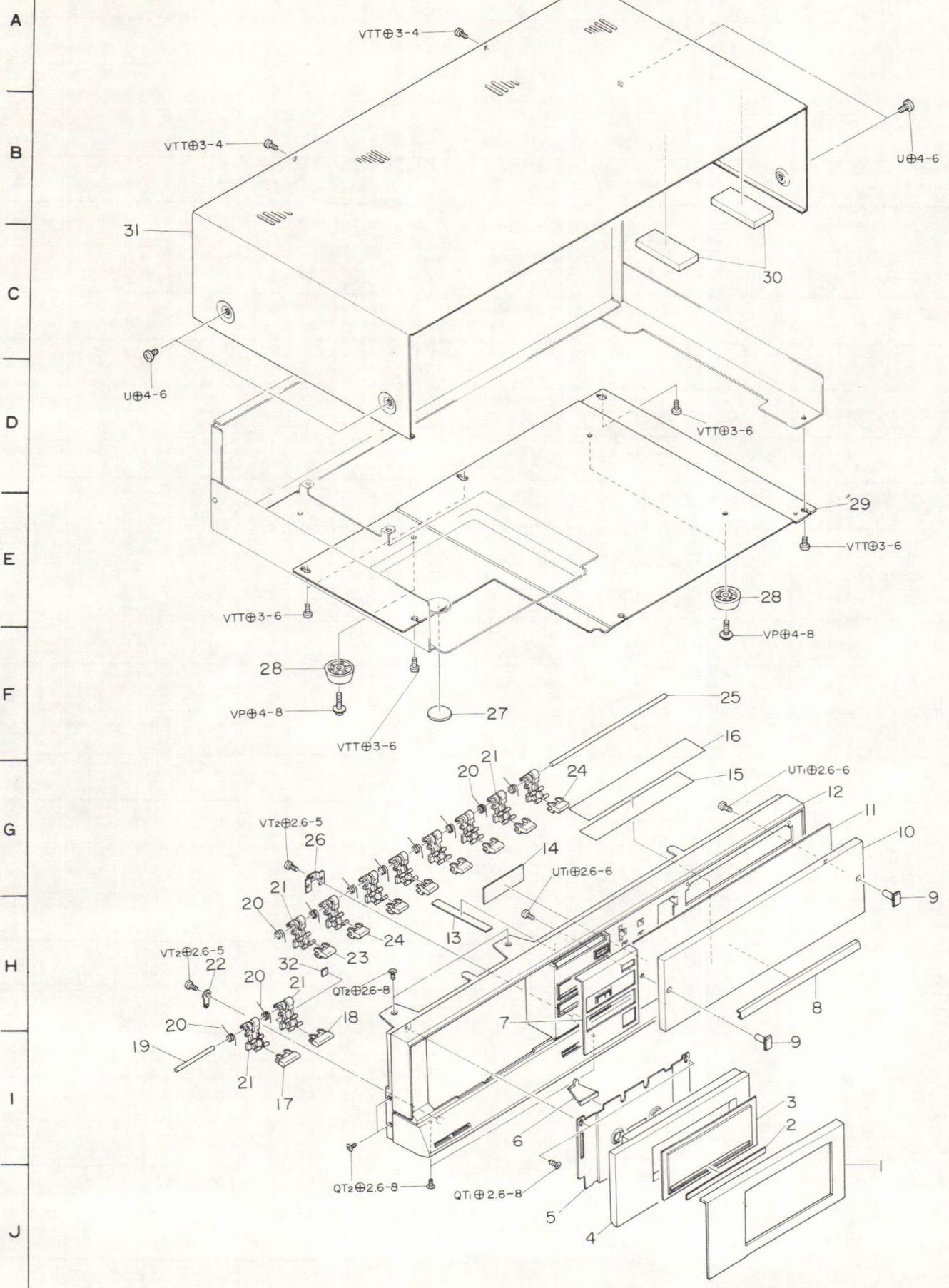


Fig. 5

EXPLODED VIEW-1

1 2 3 4 5 6 7



PARTS LIST

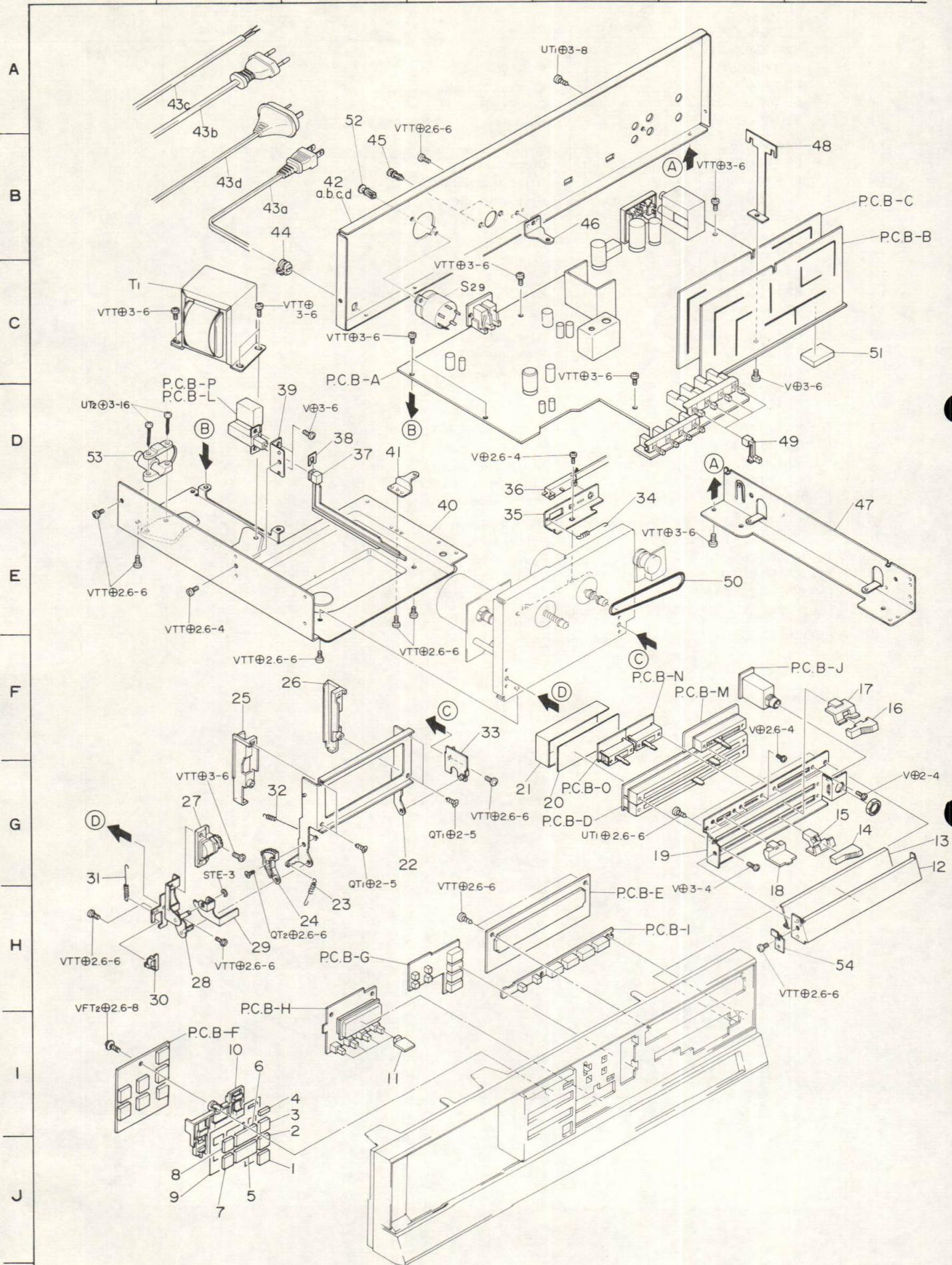
MECHANICAL PARTS

■ * mark in this part list shows exclusive part.

Ref. No.	Part No.	Part No. Changed to	Description	Common Model	Q'ty
1-1	82-179-036-01		Cassette lid	*	1
1-2	82-179-005-01		Plate, Window	*	1
1-3	82-179-006-01		Window, Cassette	*	1
1-4	82-179-034-01		Cover C, Box	*	1
1-5	82-180-009-01		Cassette plate		1
1-6	82-154-015-01		Guide, Light	AD-M700	1
1-7	82-179-046-01		Control panel	*	1
1-8	82-179-028-01		Name plate, REC	*	1
1-9	82-179-029-01		Decorative bushing	*	2
1-10	82-179-030-01		Window, Meter	*	1
1-11	82-179-026-01		Plate, Display	*	1
1-12	82-179-001-01		Cabinet, Front	*	1
1-13	82-179-246-01		Sheet B, Earth	*	1
1-14	82-179-044-01		Plate, Counter	*	1
1-15	82-179-258-01		Plate, Spacer	*	1
1-16	82-179-045-01		Plate, Cabinet	*	1
1-17	82-179-011-01		Push-button, POWER	*	1
1-18	82-179-012-01		Push-button, EJECT	*	1
1-19	82-179-212-01		Shaft, Guide lever B	*	1
1-20	82-179-234-01		T-spring, Guide lever	*	10
1-21	82-179-205-01		Guide lever, Push-button	*	10
1-22	82-179-236-01		Shaft, Metal fitting B	*	1
1-23	82-179-013-01		Push-button, ADMS	*	1
1-24	82-179-014-01		Push-button, SELECT	*	1
1-25	82-179-211-01		Shaft, Guide lever A		1
1-26	82-179-241-01		Shaft, Metal fitting A	*	1
1-27	82-168-025-01		Rubber foot	AD-3600	1
1-28	87-085-161-01		Foot		3
1-29	82-168-018-01		Cabinet, Bottom	AD-3600	1
1-30	82-179-243-01		Cushion, 20-50	*	2
1-31	82-179-002-01		Cabinet, Steel	*	1
1-32	82-179-259-01		P.V.C. sheet 4-12	*	1

EXPLODED VIEW-2

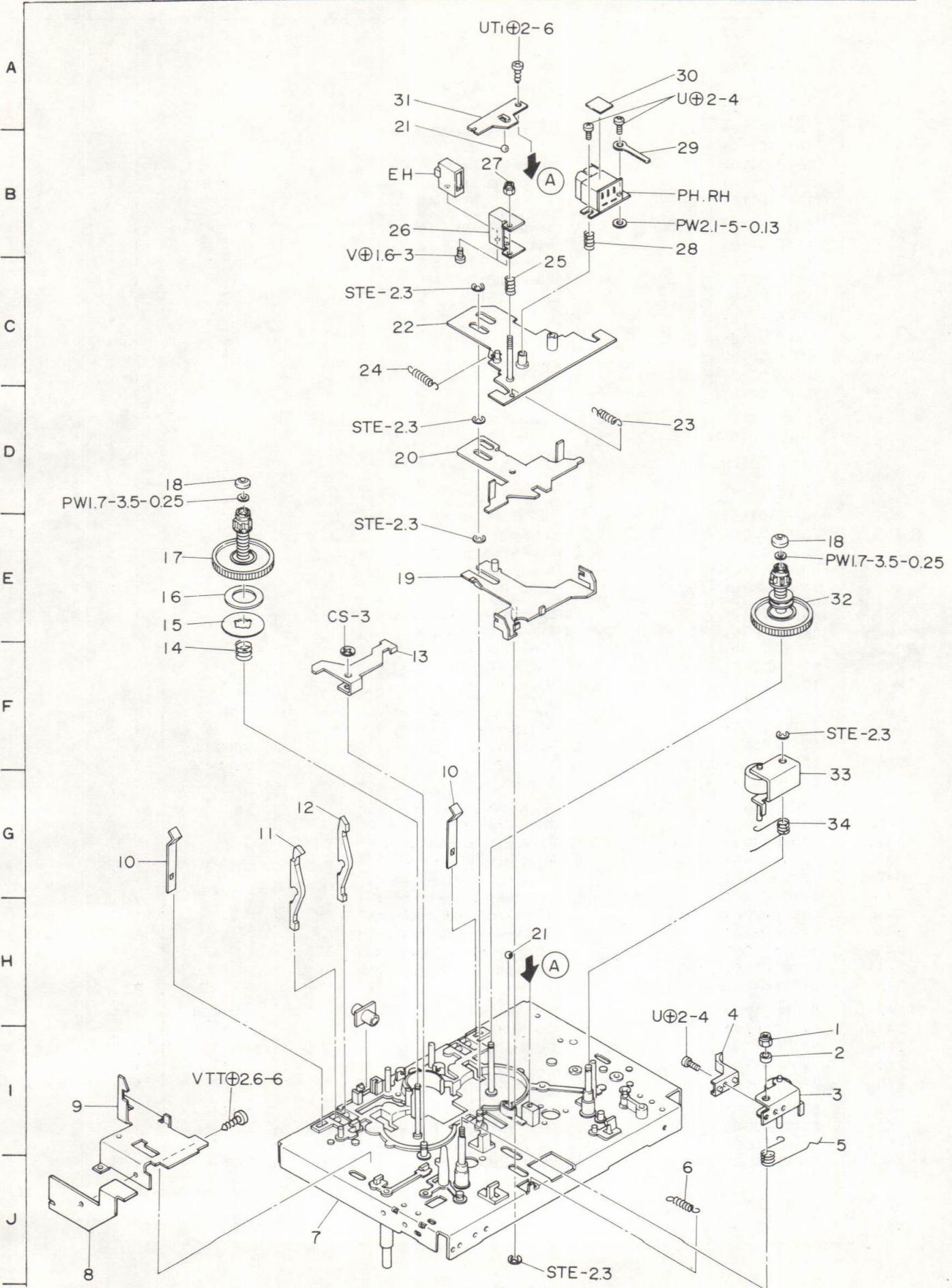
1 2 3 4 5 6 7



Ref. No.	Part No.	Part No. Changed to	Description	Common Model	Q'ty
2-1	82-179-024-01		Touch-key, MUTE	*	1
2-2	82-179-023-01		Touch-key, PAUSE	*	1
2-3	82-179-020-01		Touch-key, FF	*	1
2-4	82-179-025-01		Touch-key, COMPU	*	1
2-5	82-179-019-01		Touch-key, STOP	*	1
2-6	82-179-018-01		Touch-key, PLAY	*	1
2-7	82-179-022-01		Touch-key, REC	*	1
2-8	82-179-021-01		Touch-key, REW	*	1
2-9	82-179-242-01		Back sheet, LED	*	1
2-10	82-179-007-01		Touch-key, Light guide	*	1
2-11	82-179-010-01		Knob, Counter	*	4
2-12	82-179-027-01		REC knob plate	*	1
2-13	82-179-240-01		Plate, Auxiliary	*	1
2-14	82-179-017-01		Knob R, REC	*	1
2-15	82-179-219-01		Lever R, REC	*	1
2-16	82-179-016-01		Knob L, REC	*	1
2-17	82-179-218-01		Lever L, REC	*	1
2-18	82-179-015-01		Slide knob	*	3
2-19	82-179-203-01		Holder, Volume	*	1
2-20	82-179-248-01		Cushion, Volume	*	2
2-21	82-179-245-01		Sheet A, Earth	*	1
2-22	82-179-224-01		Cassette box ass'y	*	1
2-23	82-179-244-01		E-spring, Lid	*	1
2-24	82-179-220-01		Gear, Oil dump	*	1
2-25	82-179-032-01		Holder L, Cassette	*	1
2-26	82-179-033-01		Holder R, Cassette	*	1
2-27	82-179-228-01		Oil-dump	*	1
2-28	82-179-207-01		Cassette box holder L ass'y	*	1
2-29	82-179-204-01		Lever, EJECT	*	1
2-30	82-179-233-01		Guide, Rod	*	1
2-31	82-179-227-01		E-spring, Slide plate	*	1
2-32	82-179-249-01		E-spring, Cassette box	*	1
2-33	82-161-312-01		Cassette box holder R ass'y		1
2-34	82-179-239-01		E-spring, Remote switch	*	1
2-35	82-179-238-01		Holder, Remote switch	*	1
2-36	82-179-635-01		Wire 280, Remote switch	*	1
2-37	82-304-211-01		Rod, Selector		1
2-38	82-385-383-01		Rod, Stopper	AD-6300	1
2-39	82-160-207-01		Holder, POWER	AD-M450	1
2-40	82-179-201-01		Chassis L, Amp.	*	1
2-41	82-179-210-01		Holder circuit board B	*	1
2-42a	82-179-037-01		Panel, Rear (H model only)	*	1
2-42b	82-179-039-01		Panel, Rear (E model only)	*	1
2-42c	82-179-040-01		Panel, Rear (K model only)	*	1
2-42d	82-179-042-01		Panel, Rear (G model only)	*	1
2-43a	87-034-826-01		AC power cord (H model only)		1
2-43b	87-034-877-01		AC power cord (E model only)		1
2-43c	87-034-872-01		AC power cord (K model only)		1
2-43d	87-034-892-01		AC power cord (G model only)		1
2-44	87-085-165-01		Cord bushing (H model only)		1
2-45	87-084-078-01		Nylon rivet 3-4.5		2
2-46	82-168-213-01		Holder circuit board	AD-3600	1
2-47	82-179-202-01		Chassis R, Amp.	*	1
2-48	82-179-237-01		Holder, Dolby circuit board	*	1
2-49	82-179-213-01		Push-switch rod	*	4
2-50	82-179-256-01		Belt A, Counter	*	1
2-51	82-165-203-01		G cushion, P.C.B.	SD-L10	1
2-52	87-085-090-01		Nylon rivet 3-6.5 (H model only)		2
2-53	87-085-166-01		Holder, AC power cord (E,K,G model only)		1
2-54	82-179-265-01		Shaft A, Holder	*	1

EXPLODED VIEW-3

1 2 3 4 5 6 7



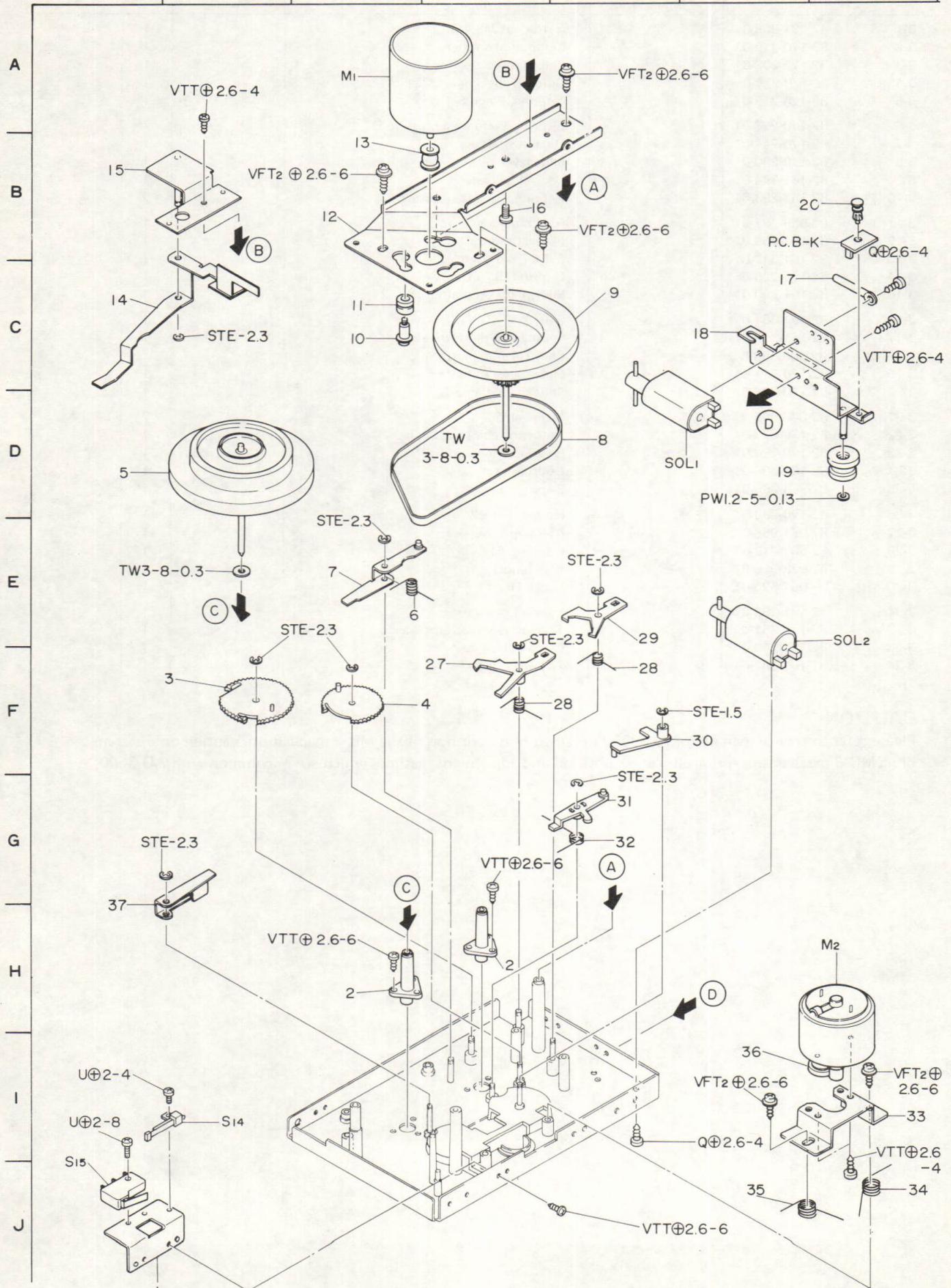
Ref. No.	Part No.	Part No. Changed to	Description	Common Model	Q'ty
3-1	87-081-969-01		Nylon nut M3-4.5		1
3-2	82-170-215-01		Collar, Pinch roller		1
3-3	82-170-208-01		Pinch lever S ass'y		1
3-4	82-170-216-01		Guide, Tape		1
3-5	82-170-218-01		T-spring, Pinch S		1
3-6	82-170-227-01		E-spring, Actuating pressure D		1
3-7	82-170-243-01		Outsert shaft ass'y D		1
3-8	82-179-230-01		Slide lever	*	1
3-9	82-161-324-01		Lock slide plate		1
3-10	82-161-293-01		P-spring, Cassette pressure		2
3-11	82-565-327-01		REC blocking lever		1
3-12	82-161-358-01		Lever, Cassette		1
3-13	82-161-347-01		EJECT blocking lever		1
3-14	82-170-225-01		C-spring (BT SD)		1
3-15	82-161-290-01		Slide plate, Actuating ass'y 2		1
3-16	82-161-351-01		Felt, 1-16-10		1
3-17	82-161-259-01		Supply reel platform ass'y		1
3-18	82-303-398-01		Cap, Take-up platform		2
3-19	82-170-231-01		Slide plate, Actuating ass'y 2		1
3-20	82-170-288-01		Slide plate, Pause 2		1
3-21	82-073-005-01		Steel ball 2φ		2
3-22	82-170-273-01		Actuating chassis ass'y 2		1
3-23	82-170-226-01		E-spring, Pinch return		1
3-24	82-161-308-01		E-spring, Actuating		1
3-25	82-565-360-01		C-spring, EH		1
3-26	82-170-283-01		Holder, EH B2		1
3-27	87-081-963-01		Nylon nut, M2-3.5		1
3-28	82-307-212-01		C-spring, EH		1
3-29	87-038-056-01		Wire binder		1
3-30	87-057-620-01		Label, Head		1
3-31	82-161-292-01		P-spring, Actuating		1
3-32	82-170-251-01		Take-up reel platform 2 ass'y		1
3-33	82-161-249-01		Pinch roller F ass'y		1
3-34	81-161-301-01		T-spring, Pinch F		1

CAUTION

Please refer to service manual for AD-3600 in regard to description of the MD-3 mechanism, caution on disassembling MD-3 mechanism, spring allocation position and adjustment method, which are in common with AD-3600.

EXPLODED VIEW-4

1 2 3 4 5 6 7



Ref. No.	Part No.	Part No. Changed to	Description	Common Model	Q'ty
4-1	82-161-234-01		Holder, REC switch		1
4-2	82-161-253-01		Shaft bearing ass'y		2
4-3	82-161-276-01		Gear, PLAY		1
4-4	82-161-277-01		Gear, PAUSE		1
4-5	82-170-228-01		Flywheel S2 ass'y		1
4-6	82-161-300-01		T-spring, Play lever		1
4-7	82-161-218-01		Play lever ass'y		1
4-8	82-170-292-01		Rubber belt, Main 2		1
4-9	81-170-219-01		Flywheel T ass'y		1
4-10	87-081-483-01		Motor screw, M2.6		3
4-11	87-087-029-01		Cushion, Rubber		3
4-12	82-161-227-01		Flywheel plate		1
4-13	82-170-276-01		Pulley, Motor		1
4-14	82-170-236-01		Lever indication ass'y		1
4-15	82-170-233-01		Holder, Indication ass'y		1
4-16	82-331-107-01		Thrust screw		2
4-17	87-038-039-01		Wire binder		1
4-18	82-179-214-01		Holder, Pulley ass'y		1
4-19	87-040-150-01		Counter pulley ass'y		1
4-20	87-084-085-01		Nylon rivet 3.5-4.5		1
4-21	82-161-269-01		Trigger lever, PLAY		1
4-22	82-170-272-01		T-spring, Trigger		2
4-23	82-161-270-01		Trigger lever, PAUSE		1
4-24	82-161-272-01		Eject lever, Brake		1
4-25	82-161-266-01		FRP lever ass'y		1
4-26	82-161-298-01		T-spring, Pause lever		1
4-27	82-170-242-01		Holder, Motor		1
4-28	82-161-295-01		T-spring, Brake L		1
4-29	82-161-296-01		T-spring, Brake R		1
4-30	82-170-248-01		Idler ass'y		1
4-31	82-179-261-01		Lever, FRP- 2	*	1

Circuit description

* Explanation of operation

1. Outline

The AD-FF8 system controller is composed of a closed loop dual capstan mechanism drive circuit, Compu-Brain (automatic recording frequency response control mechanism) and a FL (Fluorescent Lamp) electronic counter drive circuit using a 4-bit μ -computer.

2. Block diagram of controller and peripheral circuits

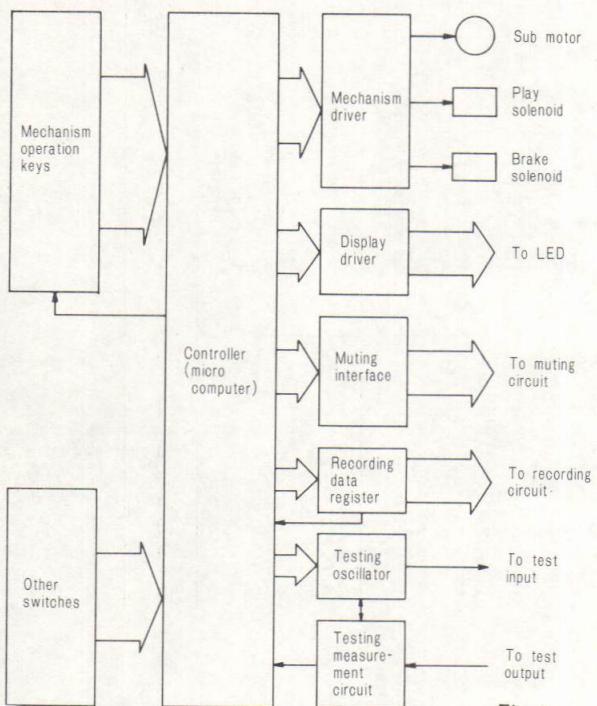


Fig. 1

3. Controller specifications

3-1. General specifications

3-1-1. It is the same as a conventional controller for STOP, PLAY, RWD, FF, REC, REC/PLAY, PLAY-PAUSE and REC/PLAY-PAUSE.

3-1-2. CUE-REV: Possible by double-pressing the PLAY and FF (or RWD) keys.

3-1-3. ONE-REC: Enters REC/PLAY-PAUSE mode only when REC key is pressed in the PAUSE mode.

3-1-4. TIMER-REC/PLAY: Same as in general specifications.

3-1-5. TIMER-PLAY: Same as in general specifications.

3-1-6. AUTO-REPEAT: Same as in general specifications.

3-1-7. MEMORY-STOP: Same as in general specifications.

3-1-8. MEMORY-PLAY: Same as in general specifications.

3-2. Additional functions

3-2-1. REC-MUT-TIMER (1): Automatically enters the REC/PLAY-PAUSE mode 4 seconds after the REC-MUT key is pressed for MS (music sensor) and released.

3-2-2. REC-MUT-TIMER (2): When this key is pressed continuously to leave a non-recorded section of 4 sec or more, the LED winds every 2 seconds after 4 sec.

3-2-3. Tape slack prevention: When the cassette is loaded, RED (120ms) — FF (120ms) operation is done to prevent the tape from becoming slack.

3-2-4. ADMS:

This is the device to demagnetize the head.

3-3. Controller timing

Control timing of the mechanism and muting timing are taken into consideration, so a peripheral time constant circuit is not required.

(See the timing chart)

4. Compu-Brain specifications

4-1. Adjustment items

4-1-1. Bias adjustment:

Adjusts bias so that the REC/PLAY sensitivity at the reference frequency (400 Hz) and the bias control Frequency (10 kHz) are the same.

4-1-2. Sensitivity adjustment: Adjusts so that the REC/PLAY sensitivity at the reference frequency is the reference value.

4-1-3. Equalization adjustment: Adjusts so that the REC/PLAY sensitivity at the equalization control frequency is the reference value.

4-2. Number of control steps

32 steps for all items

4-3. Adjustment

Sequential comparison feedback adjustment with bias current value, variable sensitivity value and variable equalization value as parameters.

Adjustment uses 5 bits ($32 = 2^5$), so adjustment is complete by comparison feedback 5 times. Adjustment is possible in 5/32 of the sequential comparison time.

4-4. Error treatment

4-4-1. When a data error (non-adjustable) occurs during adjustment, FF operation is done for 1 sec and then adjustment is repeated. When the same error occurs in the 2nd adjustment, items up to the error are displayed by LEDs, the tape is rewound and the adjustment is suspended.

4-4-2. When the tape position is changed during adjustment, adjustment is discontinued and the unit enters the STOP mode. The data is set to the reference data.

4-5. Time required

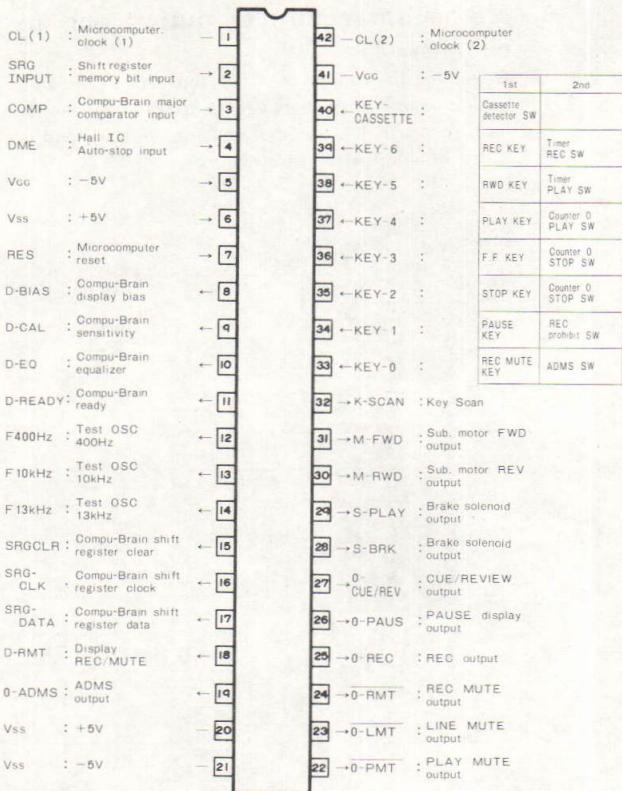
4-5-1. When an error does not occur: Approx. 16 sec

4-5-2. When an error occurs: Differs depending on the type of error.

4-6. Mechanism control key interruption

Mechanism control key operations are accepted during adjustment.

5. Terminal connection diagram



* Direction of the arrow shows the direction of signal flow.

Fig. 2

6. Description of terminals (μPD546-253)

Terminal No.	Terminal symbol	Item
1, 42	CL(1), CL(2)	μPD546 Clock oscillation terminal (400 Hz)
2	SRG INPUT	Shift register memory bit input terminal. LSB terminal of constant register (shift register) required during recording and the memory bit input. With this bit set to "1" and the Compu-Brain data set to "0", the microcomputer judges data to be reference data.
3	COMP	Detects the magnetized part of the tape during Compu-Brain adjustment (judges as magnetized when "1"). Becomes the input of the comparison result during adjustment (bias, sensitivity, equalization).
4	DME	Signal input terminal of Hall IC used for measuring the tape q'ty used during Compu-Brain operation.
5	V _{GG}	-5 V terminal (idle terminal)

Terminal No.	Terminal symbol	Item
6	V _{SS}	+5 V terminal (idle terminal)
7	RES	RESET input terminal of microcomputer at power ON/OFF operation
8	D-BIAS	Indicates bias adjustment process during Compu-Brain operation
9	D-CAL (D-SENS)	Indicates sensitivity adjustment process during Compu-Brain operation
10	D-EQ	Indicates equalization adjustment process during Compu-Brain operation
11	D-READY	Indicates completion of adjustment data setting during Compu-Brain operation
12	F400	Controls test tone frequency (400 Hz) used during Compu-Brain operation
13	F10K	Controls test tone frequency (10 kHz) used during Compu-Brain operation
14	F13K	Controls test tone frequency (13 kHz) used during Compu-Brain operation
15	SRG CLR	This bit is turned ON/OFF before outputting the reset pulse of the shift register when checking the memory bit and when checking the selection of the tape position while power is supplied.
16	SRG CLK	Sync. pulse output terminal used when transferring data inside the microcomputer to the data register (shift register).
17	SRG DATA	Terminal to output data for the shift register of the microcomputer.
18	D-RMT	REC MUTE operation indicator output.
19	0-ADMS	This bit is set to "1" during ADMS ON.
20, 21	V _{SS}	+5 V terminal (power terminal)
22	0-PMT	PLAY MUTE output. Set to ON when "0".
23	0-LMT	LINE MUTE output. Set to ON when "0".
24	0-RMT	REC MUTE output. Set to ON when "0".
25	0-REC	Output set to "1" during REC operation.
26	0-PAUS	PAUSE operation indicator output.
27	0-CUE/REV	Output set to "1" during CUE/REV operation. Controls torque MUTING, etc. of sub. motor.

Terminal No.	Terminal symbol	Item
28	S-BRK	Brake solenoid output
29	S-PLAY	Play solenoid output
30	M-RWD	Output controlling revolution direction (reverse revolution) of sub. motor
31	M-FWD	Output controlling revolution direction (normal revolution) of sub. motor
32	K-SCAN	15 key operations are input using the matrix system. This is the scan output at that time.
33 , 34 , 35 36 , 37 , 38 39 , 40	KEY-0,1,2,3,4 5,6 KEY-CASSETTE	Data input terminals for matrix key input. 1st key (mechanism control key) input is received at Low level with Key scan output at High level. With Key scan output at Low level, 2nd key (MODE key) is received at High level.
41	V _{GG}	-5 V terminal (power terminal)

Table- 1

7. KEY-SCAN circuit (15 key)

The deformed matrix input is employed as shown in figure 3, so the input levels of 1st and 2nd key inputs should satisfy the following,

V_{IH} (Input high level) > 3 V,

V_{IL} (Input low level) < 0.7 V.

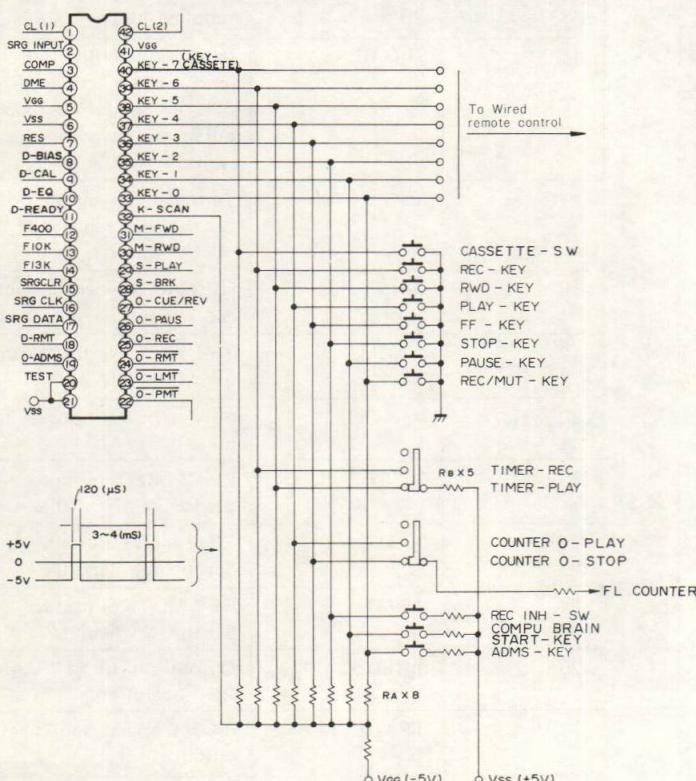


Fig. 3

8. Mechanism controller output and peripheral circuits

Refer to the timing chart in the attached diagram for the timing relationship between output terminals. The inverter used in figure 4 is an open collector output, and is composed of the open inverter or transistors.

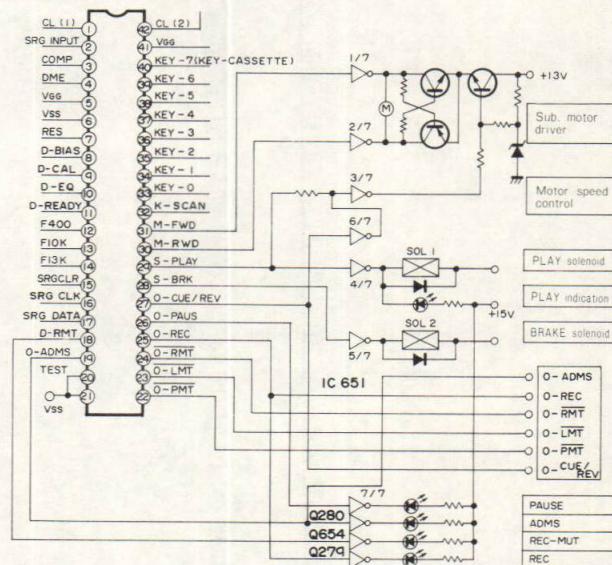
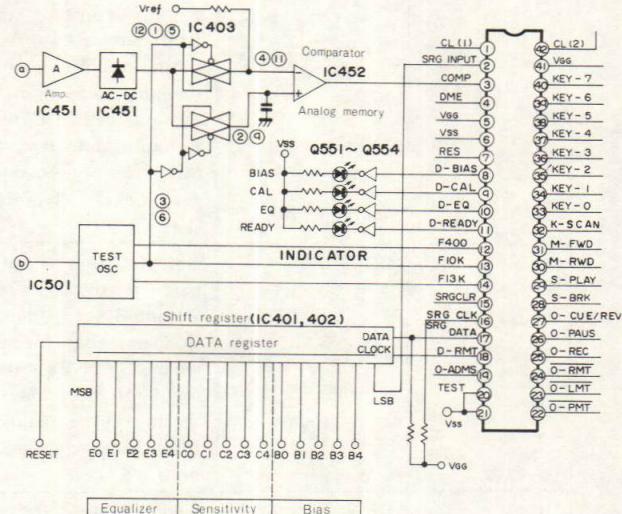


Fig. 4

9. Compu-Brain peripheral circuits

9-1. Connection diagram



- (a): Test signal (REC/PLAY output) input terminal
- (b): Test signal (REC input) output terminal

Fig. 5

9-1-1. Shift register: This is the REC circuit drive data register; data is transferred in the direction of the arrow. MSB (5th bit of equalization) is the 1st data item and LSB (MEMO) is the last data item. Bits of each item have following weight.

(B,C,E)0 : 2^0
 (B,C,E)1 : 2^1
 (B,C,E)2 : 2^2
 (B,C,E)3 : 2^3
 (B,C,E)4 : 2^4

9-1-2. TEST oscillator: Testing oscillator and frequency is set by 3 outputs shown below.

F400: Reference frequency (400 Hz ~ 1 kHz)

F10K: Bias control frequency (5 k ~ 8 kHz)

F13K: Equalizer control frequency (10 k ~ 18 kHz)

F10K output is used for the control line which switches over the comparator input to the difference between F10K (output voltage) and F400 (output voltage) and transfers it to microcomputer.

9-1-3. Amp. AC-DC: Amplifies the output signal during testing and converts it to direct current.

9-1-4. Vref: Reference voltage during sensitivity adjustment and equalization adjustment.

9-1-5. Analog memory: Memorizes output voltage of F400 during bias adjustment.

9-1-6. Comparator: Comparator used for sequential comparison feedback.

9-1-7. Item indication: Indicates items following the adjustment procedure.

9-2. Detection of magnetized section

Whether or not it is a magnetized section of tape before starting adjustment. The method is:

9-2-1. Test oscillator: F400 is set to "1".

9-2-2. Contents of shift register

Bias = 10000 (binary) center value

Sensitivity = 00000 (binary) Max. value

Equalization = 10000 (binary) center value

9-2-3. Comparator: Whether or not the recorded and played back voltage (output voltage) is larger or smaller than the reference voltage is compared and discriminated.

When the COMP signal (comparator output) is set to "0" in the above condition, it is judged to be a magnetized section and when it is set to "1", it is judged to be another condition (leader tape, tape broken, etc.).

9-3. Basic principle of sequential comparison feedback adjustment

The sequential comparison feedback adjustment is frequently used for high speed in A/D (analog-digital) conversion. In this case, the voltage and current are the analog data converted to digital data via the D/A (digital/analog) converter.

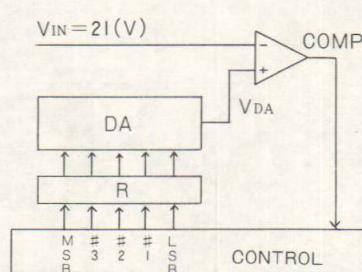


Fig. 6

V_{IN}: Input voltage to be converted
V_{DA}: Voltage with contents of R as analog value
COMP: Comparator
DA: Analog value of contents of R
R: Comparison register
CONTROL: Overall controls
 $* V_{IN} = 20 (V)$

- Range of V_{IN} is set 0 V ~ 31 V for convenience
- Number of conversion bits is set to 5 (0 ~ 2^5 , 0 ~ 31).
- DA is to convert the 5 bit digital value of R to 00000 = 0 V, 11111 = 31 V.

Resulting from the above, each bit has the following weight:

MSB = 16 V Most significant bit

#3 = 8 V

#2 = 4 V

#1 = 2 V

LST = 1 V Least significant bit

- When COMP = "0", it is left as it is, and when it "1", it is reset.

Conversion procedure

#	R	DA(V)	$V_{DA} - V_{IN}$	COMP	R	
MSB	0 0 0 0 0	16	16 - 21 < 0	" 0 "	1 0 0 0 0	Left as it is Reset
3	1 0 0 0 0	24	24 - 21 > 0	" 1 "	1 0 0 0 0	
2	1 0 1 0 0	20	20 - 21 < 0	" 0 "	1 0 1 0 0	Left as it is Reset
1	1 0 1 1 0	22	22 - 21 > 0	" 1 "	1 0 1 0 0	
LSB	1 0 1 0 1	21	21 - 21 = 0	Not fixed	1 0 1 0 X	Not fixed

Table-2

As a result, it is converted to the digital value as
 $R = 10101 = 21$ or $R = 10100 = 20$

with the error $LSB \pm 1$ (bit).

The above is the principle of A/D conversion. The block diagrams of sensitivity, equalization adjustment and bias adjustment in this controller are shown in figures 7 and 8.

9-4. Sensitivity and equalization adjustment block diagram

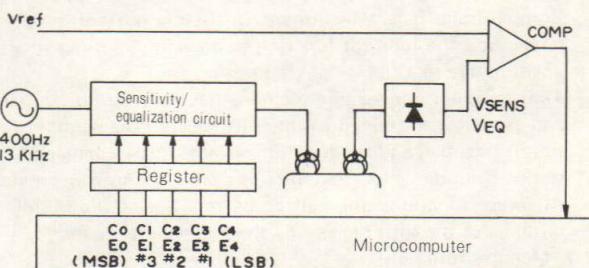


Fig. 7

9-5. Bias adjustment block diagram

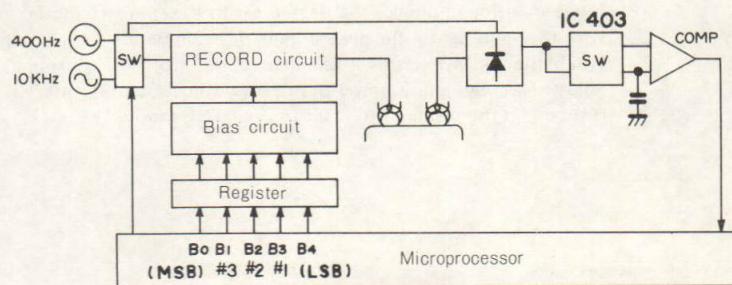


Fig. 8

9-6. Logic of each adjustment

In the adjustment (conversion) method shown above, treatment against COMP bit is considered in the following 2 ways.

9-6-1. • Resets the corresponding bit with COMP = "0".

- Resets the corresponding bit with COMP = "1".

Significance (relation between data and bias amount, sensitivity amount, equalization amount, etc.) of adjustment circuit classified by item varies.

9-6-2. Bias adjustment

- COMP = "1" (+) should be obtained when F400 (reference frequency) output < F10K (bias adjustment output)
- COMP should work towards "1" as bias data gets larger.

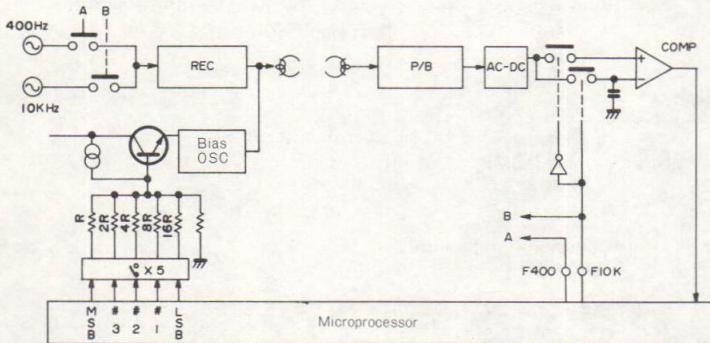


Fig. 9

a) and b) described previously are established in figure 9, so check it as reference.

9-6-3. Sensitivity, equalization adjustment

- COMP should be set to "0" with:

Vref (reference output level) < F400 (reference frequency) output,
Vref (reference output level) < F13K (equalization adjustment frequency) output.

- COMP should work toward "0" as sensitivity and equalization become larger.

(The above is the logic determined by software inside the microprocessor)

9-7. MEMO terminal of shift register

This controller is provided with the monitor function of the Compu-Brain data when there is an intermittent supply of power and the monitor function to prevent recording at wrong position due to a change of tape position.

That is, when non-volatile memory data backed up by C-MOS and capacitor is applied to the shift register, the memory function is possible, and the function automatically changing to the standard mode when the tape position is changed is provided. All these functions are realized by monitoring the MEMO bit terminal of the shift register by the controller.

9-7-1. Memory function:

When the MEMO terminal is set to "1" ("1" when Compu-Brain data is set to "1") when of power is supplied, it is assumed to be the READY indication. When data is protected as it is and when it is set to TIMER recording, it is set to TIMER recording by means of Compu-Brain data naturally.

9-7-2. Tape monitoring position:

When the MEMO terminal changes from "1" to "0" in the mode mentioned above, the deck is set to the standard mode with the value set by the general tape position data.

When the MEMO terminal changes to "0" from "1" during adjustment by the Compu-Brain, the adjustment is interrupted and the mechanism is set to the STOP mode.

Circuit explanation

10. System controller

10-1. MPU (Microprocessor Unit)

This is a 4-bit CPU which is the heart of the control unit. It works in the following sequence when power is applied.

Step 1:

Simultaneously with the power supply, the internal clock oscillator with a frequency of 400 Hz determined by the ceramic filter connected between CL1 (pin 1) and CL2 (pin 42) starts, and MPU starts operation. [the 400 Hz clock can be observed at pins (1) and (42) using an oscilloscope]

Step 2:

When the RESET terminal (pin 7) is in the RESET mode at "H" level (3 V or more), the output terminals (pins 8 ~ 32) are set to "L" level (0.7 V or less) and the MPU is kept at stop at the first step of the internal program.

Step 3:

When the RESET terminal (pin 7) is set to "L" level (0.7 V or less) several hundred seconds after power is supplied, and RESET is released, CPM starts operation following the internal program.

Step 4:

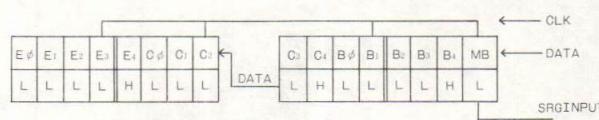
At first after RESET is released, MPU outputs "H" level to SRG CLR (shift register, CLEAR) terminal (pin 5) to check whether the contents of the shift register (IC401, IC402), which is the Compu-Brain memory, is standard data or Compu-Brain data. ("H" level is output to K-SCAN terminal (pin 32) at that time; it is output to the program only, so the key input described later is not done)

This SRG CLR output signal is inhibited by D419 when the terminal voltage of the backup capacitor C401 when the shift register power voltage is OFF is more than 3 V, but when the terminal voltage of capacitor C401 is 3 V or less, the SRG CLR output signal sets the LSB (IC401-1/2) output of the shift register to CLEAR (sets to "L" level) via D418, R417 (It is inhibited via D417 when the output of IC401 pin (5) memory bit is set to "L" level).

Step 5:

After that, the CPU inputs the LSB memory bit (IC401 pin 5) of the shift register from SRG INPUT (pin 2). When it is set to "H" level, CPU judges that the contents of the shift register are Compu-Brain data and sets the READY terminal (pin 11) of the Compu-Brain indicator to "H" level and lights the READY indicator.

When it is set to "L" level, the CPU judges that the contents of the shift register are the standard data or the terminal voltage of the back-up capacitor is 3 V or less and the contents of the shift register are not kept as it was when the power was OFF, and outputs from SRGDATA (pin 17), SRGCLK (pin 16) and set the contents of the shift register to the standard data.



* Content of shift register when the data is standard

Fig. 10

10-2-2. MUTING drive circuit

The MUTING drive circuit is composed of Q657, Q658 and Q659. When MPU is reset during power ON and OFF, MPU 0-RMT and 0-LMT and 0-PMT terminals are set to "L" level and it works as an inverter to inverse logic at that time because it is required to set the MUTING transistor to ON later. MUTING power supply is stored using D661, D658 to maintain MUTING when the power voltage drops during power OFF.

0-RMT is set to "H" level and releases MUTING of the REC amp (REC MUTE).

0-PMT is set to "H" level and releases MUTING of PLAY amp (PLAY MUTE).

0-LMT is set to "L" level during power ON, OFF and Compu-Brain operation and inhibits LINE IN input and LINE OUT output (LINE MUTE).

10-2-3. MPU RESET circuit

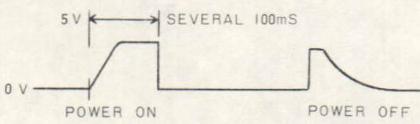


Fig. 13

MPU RESET circuit is composed of Q655 and Q656 and performs MPU RESET operation during the power ON/OFF operation.

C657 is charged via D662 or D663 by AC input simultaneously with POWER ON but as Q656 is set to ON via R658, the current flowing through R659 flows to Q656 and so Q655 is set to OFF. As a result, the "H" level is input to MPU RESET input (pin 7) via R657 and MPU is reset.

The -7.5 V power supply rises several hundred seconds after power is set to ON, so current starts flowing to zener diode D664 and the base voltage of Q656 tends to be negative. When Q656 is set to OFF, current flows to the base of Q655 via R659, so Q655 is set to ON and MPU RESET is released. The time constant of Q657, R660 is short during POWER OFF, C657 immediately discharges and the current flowing to the base of Q655 via R659 disappears, Q655 is set to OFF and MPU is reset again.

10-2-4. Mechanism display LED drive circuit

Mechanism display LED driver is composed of IC651-4/7 (PLAY ▶), IC651-7/7 (PAUSE II), Q654 (REC MUTE ●), for PLAY solenoid drive and REC LED drive Q279 is used in common for REC bias Power drive.

10-3. Compu-Brain oscillation circuit

The Compu-Brain oscillation circuit is composed of the oscillation circuit IC501-2/2 with Wynne bridge, Servo amp. IC501-1/2 and frequency select analog switch IC502.

10-3-1. Wynne bridge oscillation circuit

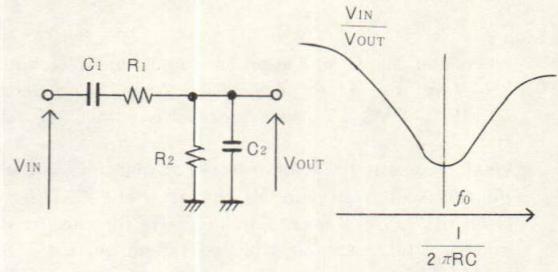
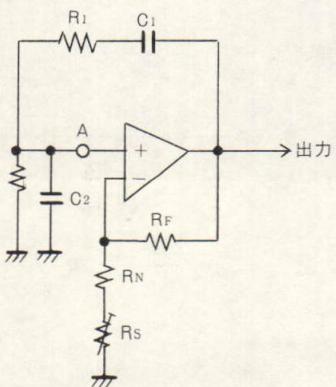


Fig. 14

Basic composition of the Wynne bridge is shown in Figure 14.

The loss of the positive feedback circuit when $R = R_1 = R_2$, $C = C_1 = C_2$, is minimum is approx. 1/3 with the frequency $f_0 = \frac{1}{2\pi RC}$. When R_S of the negative feedback circuit is varied and controlled so that the amp gain determined by $\frac{R_N + R_S}{R_N + R_S + R_F}$ is equivalent to the loss, the signal fed back from the output is amplified by attenuated component, so stable sine wave oscillation is done at a constant voltage.

10-3-2. Servo amp circuit

The servo amp IC501-1/2 performs this automatic variation of R_S and FET (Q501) is used as variable resistance element for R_S .

When the oscillation circuit output is still set to the GND potential, the (+) input of the servo amp IC501-1/2 is set to approx. +0.6 V because it is divided by R510 and R511 and connected to +7.5 V, and the output potential of the servo amp tends to be positive. The gate voltage of FET Q501 at that time is set to GND potential by R515, and the resistance R_{DS} between drain sources of FET is lowest ($R_{DS} = 500\Omega$ or less). The amp gain of the Wynne bridge oscillation circuit is 3.16 times or more at that time, so the oscillation circuit starts oscillation. When the oscillation voltage exceeds -0.6 V at its peak in the negative direction, the potential of the (+) input of the servo amp. starts to be negative, so its output amplified approx. 20 times applies reverse bias to the FET gate via R511, D503 to boost R_{DS} .

As a result, the amp. again of the oscillation circuit is decreased by boosting R_{DS} , so the oscillation output is decreased and the peak value of the negative potential is stabilized at around -0.6 V, 400 Vrms.

10-3-3. Analog switch circuit

The oscillation frequency is switched over by the analog switch IC502. IC501 terminal pins (1) ~ (2), (3) ~ (4) and (9) ~ (10) are set to ON respectively by MPU outputs F400, F10K and F13K to switch over the positive feedback time constants C1, C2, R1, R2 of the Wynne bridge oscillation circuit described previously. (R501 and R502 during F400Hz are not equal. This is because of the fact that $R501 // R507 \neq R502$)

10-3-4. Operation during adjustment

The TEST TONE 400 Hz and 10 kHz are alternately changed over and oscillate at the period of approx. 600 ms to compare the REC/PLAY levels between 400 Hz and 10 kHz during the Compu-Brain bias adjustment. When the oscillation output voltage is rapidly boosted during selection, it is required to stabilize it due to the time constant of the servo circuit, so the output voltage is clipped by D501, D502 so that it is not boosted rapidly.

The test tone frequency is set to 400 Hz during CAL adjustment, and 13 kHz during EQ adjustment.

When the oscillation circuit is oscillating during the Compu-Brain operation, MPU 0-LMT terminal (pin 23) is set to "L" level, so IC502 pin (12) is set to "H" level via the mechanism control MUTING driver Q658. As a result, pins (10) ~ (11) are set to ON and the output of the oscillation circuit is input to the Dolby encoder INPUT of the audio circuit Dolby IC HA11226 via R516, IC502 pins (10) ~ (11) and SFR501. The LINE MUTE signal is set to

"H" level at that time, and the Dolby encoder INPUT is grounded by R199 via Q153, so the output of the oscillator is attenuated by R199/(R199 + R516 + SFR501) and set to approx. 7.75 mV (-17 V when converted to Dolby input level).

10-3-5. Compu-Brain oscillation level adjustment

The output of the Compu-Brain oscillator should be adjusted to calibrate the Compu-Brain MEASURE.

Adjust it by the following procedure.

(Strictly observe the procedure)

- (1) Remove the 1P connector between MEASURE INPUT and PB Dolby OUTPUT.
- (2) Load a blank tape and turn Compu-Brain on.
- (3) Connect an oscilloscope to MEASURE COMP OUTPUT test point TP-7.
- (4) Connect the Dolby encoder OUTPUT test point TP-1 and MEASURE INPUT when the set enters the RE-WIND mode.
- (5) Adjust the Compu-Brain oscillator SFR501 so that the 400 Hz rectangular wave appears on the oscilloscope.
- (6) Disconnect TP-1 and MEASURE INPUT when adjustment is completed, and then connect MEASURE INPUT and PB Dolby OUTPUT again using the 1P connector.

The adjustment mentioned above should be done again when the Lch Dolby PC Board or IC is replaced, or the constant of the Compu-Brain oscillator or MEASURE is replaced.

10-4. Compu-Brain MEASURE unit

This circuit amplifies (IC451-2/2), rectifies (IC451-1/2, D451) and compares (IC453, IC452-1/2) the recorded and played back TEST TONE during the Compu-Brain operation and inputs it to MPU COMP terminal (pin 3). The REC/PLAY level of the Compu-Brain TEST TONE is approx. -17 VU but it is only approx. 77.5 mV at the PB Dolby OUTPUT, so this TEST TONE of this PB Dolby OUTPUT is amplified approx. 25 times by IC451-2/2. The amplification gain is determined by R462 and C455 connected to R454 in parallel. R462, C455 determine the REC/PLAY frequency response after Compu-Brain adjustment. It is designed so that 10 kHz and 13 kHz are increased by approx. +0.5 dB ~ 1.0 dB over 400 Hz and adjusted.

The signal amplified here is set to approx. 2 Vrms, and amplified by IC451-1/2, rectified by D451, applied to C453, and by applying feedback to IC451-1/2, converted to approx. 1 : 1 DC 2 V.

IC453 in the next stage works as the analog MPX; when MPU F10K terminal is set to "H" level, IC453 pins (3), (6) are set to "H" level, and pins (12), (1), (5) and pins (4), (11) are set to ON. When MPU F10K terminal is set to "L" level, pins (12), (1), (5) and pins (2), (9) are set to ON. That is, when the oscillation frequency of the Compu-Brain oscillator is set to 400 Hz or 13 kHz, and the MPU F10K terminal is set to "L" level, potential Vref (approx. 2 V) of SFR451 is connected to (+) input of the comparator IC452-1/2 in the next stage, and the potential of C453 - rectified REC/PLAY output voltage of TEST TONE - is connected to (-) input, and these two are compared. This is done during Compu-Brain and EQ adjustment; data of discrimination of level between potentials Vref and C453 done by MPU via IC452-1/2 is received via COMP terminal (pin 3) to adjust sensitivity and EQ.

When the oscillation frequency of the Compu-Brain oscillator is designated to be 10 kHz and the MPU F10K terminal is set to "H" level, pins (12), (1), (5) ~ pins (4), (11) are set to ON. The ON resistance between pins (12), (1), (5) and pins (4), (11) is only approx. 1 kΩ at that time, so the potential of SFR IC452-1/2 (+) input is set approximately equivalent to the potential of C453. This is used for Compu-Brain bias adjustment.

The Compu-Brain oscillator first oscillates at 400 Hz in the bias adjustment; this sets IC453 pins (12), (1), (5) and pins (2), (9) to ON and the terminal voltage of C453 is applied to IC452-1/2 (-) input and is applied to C454 simultaneously. Next at the instant when MPU changes over the frequency of the Compu-Brain oscillator to 10 kHz, pins (12), (1), (5) and pins (2), (9) are set to OFF, and pins (12), (1), (5) and pins (4), (11) are set to ON, so the voltage produced by rectifying the 400 Hz REC/PLAY output is applied to IC452-1/2 (-) input while it is kept as it is by C454. The voltage produced by rectifying the 10 kHz REC/PLAY output is applied to the (+) input side later, so MPU inputs the IC452-1/2 COMP output produced by comparing these two from COMP terminal (pin 3) and obtains the REC/PLAY sensitivity difference between 400 Hz and 10 kHz, and varies the bias.

10-5. Compu-Brain D/A unit

The Compu-Brain D/A unit is composed of the shift register IC401, IC402 described previously in the description of MPU, capacitor back-up voltage, monitoring comparator IC452-2/2, D/A transistors Q401 ~ Q425.

10-5-1. Shift register

IC401, IC402 HD14015BPs incorporate 2 x 4 stage serial INPUT parallel OUTPUT shift registers.

By cascade-connecting IC401 and IC402, they compose a synchronized 16-bit serial INPUT parallel OUTPUT shift register.

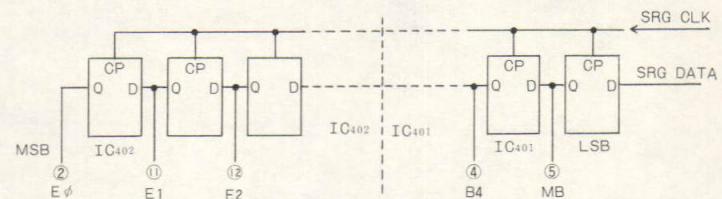


Fig. 15

The shift register is composed of the D-flip-flop as shown in Figure 15, and the D-flip-flop latches the data (D output) to the output (Q output) at the rise of the clock (CP input) signal. As a result, data shifts by one to the left; as the contents of SRG DATA shown in Figure 14 shift to MB (MEMORY BIT) by 1 clock pulse (SRG CLK), and the contents of MB shift to B4.

When MPU reloads the contents of the shift register, MPU outputs 16 pulses to the SRG CLK terminal and outputs SRG DATA following the data set in sequence starting at the MSB side (Eφ side) in synchronization with the pulses; in this way, MPU reloads the shift register.

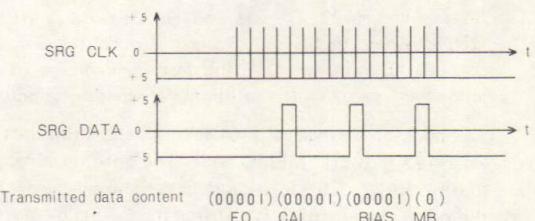


Fig. 16

This shift register is provided with the serial/parallel conversion function which converts the REC bias, sensitivity, EQ and MB data transmitted via 2 lines — SRG CLOCK and SRG DATA — from MPU to the digital/analog converging 16-bit parallel data through the circuit shown in Figure 17, and functions as the data register (memory) which stores these data during the power ON/OFF operation.

10-5-2. D/A (Digital/Analog) conversion circuit

The parallel output of the shift register is converted to analog values used for Bias, Cal and EQ adjustment via this circuit. The D/A conversion is done by switching each bit of the resistor block's 5-bits (R425, 427, 429) using transistors. The D/A conversion principle is: The value of R_X shown in Figure 17 is changed to $3.9 \text{ k} \sim \infty$ by the transistor switched by the 5-bit resistor block.

For example, resistance of the resistor block corresponding to each bit has approximately double the weight of the data of the shift register output $B_4 \sim B_0$. e_{out}/e_{in} attenuation amount is changed as shown in Figure 16 by the data (0 ~ 31) of the BCD code of $B_4 \sim B_0$ to perform D/A conversion.

R_A here corresponds to the bias circuit R283 in the bias adjustment, the REC amp. R205 in the CAL adjustment and the REC amp C199 \times R257 in the EQ adjustment.

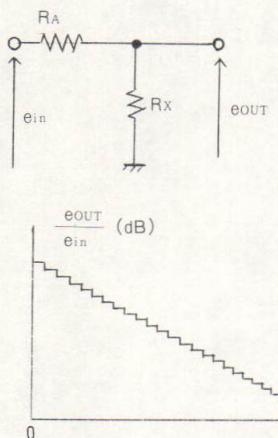


Fig. 17

10-5-3.

IC452-2/2 controls another function of the shift register as the data register (memory). C401 0.022F (scheduled to be changed to $3300\mu\text{F}/16\text{V}$) guarantees non-volatility of the shift register during power OFF.

IC452-2/2 works as a comparator. The voltages at both terminals of R420 are set to approx. 3.3 V by R421, so when the C401 voltage plus C420 voltage (0.4 V) is 3.3 V or more, the output of IC452-2/2 is set to "L" level and inhibits the SRG CLR signal output from MPU during power ON by means of D419.

(See Explanation of microcomputer).

C401 0.022F is charged with the time constant of approx. 30 sec via R422, 5.6 k Ω and R423, 6.8 k Ω after power ON, so when the SRG CLR signal is output several hundred seconds after power ON, the terminal voltage of C401 is almost the same as the terminal voltage during power OFF.

The back-up voltage of C401 is supplied to the shift register via R422, 5.6 k Ω (MEMO Vss). The both terminal voltages of this R422, 5.6 k Ω should be as shown below to keep the contents of the shift register for 24 hrs or more during power OFF:

5 mV or less when C401 = 0.022F

1 mV or less when C401 = $3300\mu\text{F}$.

MEMO Vss advances toward the tape selector switch. This switch turns ON instantaneously when the tape selector is switched over, and MEMO Vss passes through C420, 0.0047 μF , differentiated and clears the shift register which stores MB in the 16-bit shift register.

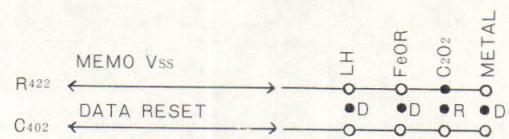


Fig. 18

This MB is set to "H" level when the CPU starts the Compu-Brain operation, and is kept at "H" level during the Compu-Brain operation or when the Compu-Brain data is stored in the shift register.

It is set to "L" level when the standard data is in the shift register. MPU always monitors this MB via the SRG INP terminal; when it is set to "L" level during power ON or when it changes to "L" level from "H" level, MPU immediately sets the shift register to the standard data by the procedure shown in Figure 16.

When the MPU starts the Compu-Brain operation, this MB is set to "H" level. When it is not set to "H" level for some reason, the Compu-Brain operation is interrupted.

- (1) D419 is open and SRG CLR signal is not inhibited.
- (2) IC452-2/2 output is set to "H" level and SRG CLR signal is not inhibited.
- (3) Power to the shift register changes when the output of IC401 or IC402 shift register is short-circuited or D421 is open.
- (4) When a mechanism control key or RM key is pressed continuously.

The shift register operation can be checked by the fact that the pulse is output when Compu-Brain operation starts; it is seen when monitoring IC402 pin (2), E_ϕ output using an oscilloscope. Be sure to use the specified diode MA150 for D420, D421, D416, D417, D401 ~ D415 because the capacitor back-up time is shortened when the counter leak current is too high.

When MB is set to "L" level, the SRG CLR signal is inhibited by D417. This diode inhibits the SRG CLR signal passing through C402 when the tape selector is changed over during standard data operation. MB is originally set to "L" level, so it does not change when the shift register is cleared and set to "L" level, so MPU cannot detect that the shift register is cleared.

10-6. FL (Fluorescent Lamp) Drive unit

The FL DRIVE unit is composed of the AC CLOCK shaper Q704, FL filament power supply D704, FL counter UP/DOWN driver Q702, D702 and MEMORY REWIND circuit IC701, Q701, D702.

10-6-1. Explanation of FL electronic counter unit terminals

Terminal No.	Terminal symbol	Item
1	60/50	Output pulse only during power ON. AC CLOCK is judged as 50 Hz with this terminal connected to GND, and 60 Hz with this terminal open.
2	STA/STP	Receives START/STOP instruction of TAPE TIME function. TAPE TIME starts at "H" level.
3	WR	Set to "H" level with MEMORY REWIND SW set to ON, and the internal counter LSI memorizes the counter data at that time.
4	V _{SS}	Power GND input terminal. Connect to +5 V.
5	V _{DD}	Counter LSI power supply. Connect to -5 V.

Terminal No.	Terminal symbol	Item
6	Vdis	FL cathode power supply. Connect to -13 V.
7	UP/DOWN	Addition/subtraction instruction input of the counter. Set to addition at "H" level, and to subtraction, at "L" level.
8	C-CLK	Counter clock input. Add or subtract 1 per pulse according to the UP/DOWN input.
9	T-CLK	TAPE TIME clock. Divides according to the pin (1) input 60/50 terminal with AC 50 Hz or 60 Hz clock input, and counts 1 per sec.
10	A, D	"H" level is output when the counter content is set to "0000".
11	M, D	"H" level is output when the counter content matches the number memorized by WR.
12	F	FL cathode electrode filament power supply. Supplies power (effective value; approx. 1.8 V) between Vdis and F.

10-6-2. AC CLOCK shaper

This produces the reference clock of the TAPE TIME function of the FL electronic counter. Q704 is set to ON in the positive half period (+1.8 V or more) of the secondary side of the power transformer, and OFF in the negative side half period (+1.8 V or less) and produces the 50 Hz or 60 Hz rectangular wave and inputs it to the FL electronic counter T-CLK terminal as CLOCK.

10-6-3. FL electronic counter UP/DOWN driver

This instructs the addition mode or subtraction mode of the electronic counter. It is in the addition mode when the sub. motor of the mechanism is rotating in the positive direction, and in the subtraction mode when it is rotating in reverse. The mechanism does not stop immediately; it is designed so that addition is kept in positive rotation → STOP, and subtraction is kept in reverse rotation → STOP. This is done by charging C703 from the MPU M-FWD terminal ("H" level during sub. motor positive rotation) via D701, and by setting Q702 by means of the MPU M-RWD terminal ("H" level during sub. motor reverse rotation) and discharging C703 during the reverse rotation.

10-6-4. MEMORY REWIND circuit

This circuit receives the MEMORY REWIND switch instruction inside the FL electronic counter and operates the MEMORY REWIND function ON/OFF. When the MEMORY REWIND function is set to ON, LSI inside the FL electronic counter memorizes the counter's content. The "H" level is output to the FL electronic counter FL terminal at that time, so the toggle flip-flop composed of IC701-1/4, -2/4, -3/4 is set. IC701-1/4 pin (3) is set to "H" level at that time and the MEMORY REWIND LED indicator is lit via Q703. S-PLAY terminal is set to "H" level when MPU is in the PLAY mode, so both IC701-4/4 pins (12), (13) are set to "H" level and the pin (11) level is set to "L" level. (The REC input is set to "L" level in the REC mode, so the pin (13) "H" level is inhibited via D703 and the operation thereafter is not done)

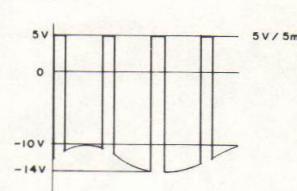
When the content of the FL electronic counter matches the number memorized in the LSI inside the counter, "H" level is output to the FL MD terminal, Q701 is set to ON and the REWIND instruction is given to MPU via D702.

Note 1.

The FL electronic counter unit is very vulnerable to static electricity because an LSI is used, so be careful in handling it with the connector removed.

10-6-5. Waveform of IC (HD38701) used for electronic counter

① ② ⑦ ⑧ D0 ~ D3



Phases of D0, D1, D2, D3 drift by approx. 1.7ms each

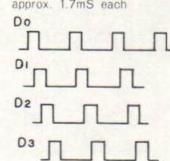
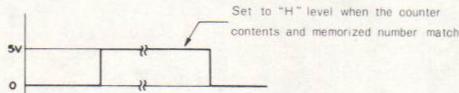


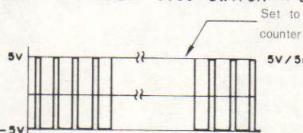
Fig. 19

③ MD



Set to "H" level when the counter contents and memorized number match

④ ZD (COUNTER "0000" SWITCH → STOP)



Set to "H" level constant when the counter is set to "0 0 0".

Fig. 20

⑤ S-CLK (With 50Hz power supply frequency)

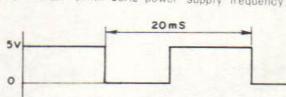
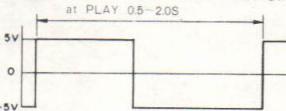


Fig. 21

⑥ C-CLK Set to "H" level during RESET SWITCH ON at PLAY 0.5~2.0S



⑦ UP/DOWN

at PLAY: FF : 4.5V

at REW : 0V

⑧ RST

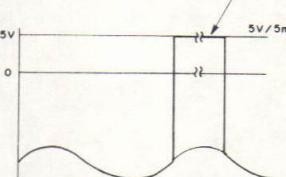


Fig. 22

⑨ Vdis (With 50Hz power supply frequency)

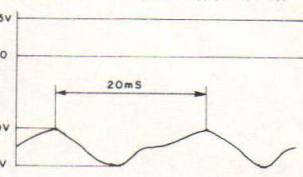


Fig. 23

⑩ PW-RST (POWER ON)

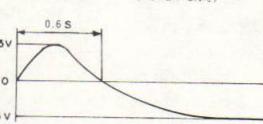


Fig. 24

(11) V_{DD} - 5V Const

(12) (14) 5V Const

(13) OSC

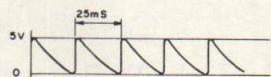


Fig. 27

(15) WR

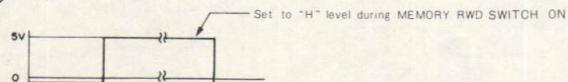


Fig. 28

(16) 50/60 (During POWER ON)

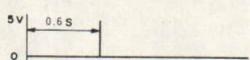


Fig. 29

(17) W/C During WATCH display : "H" level +5V

During COUNTER display : Same as "L" level ⑨ Vdis.

(18) START/STOP During PLAY : "H" level +5V

During STOP, FF, REW, PAUSE : "L" level 0V

(19) MR Power frequency select switch 50Hz : GND level

Power frequency select switch 60Hz : Same as ⑨ 50/60

⑩ ⑪ ⑫ ⑬ ⑭ ⑮ ⑯ ⑰ ⑱ ⑲ ⑳ a~g

Duty of a ~ g changes 0 ~ 100% depending on numerals displayed.

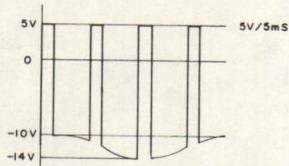


Fig. 30

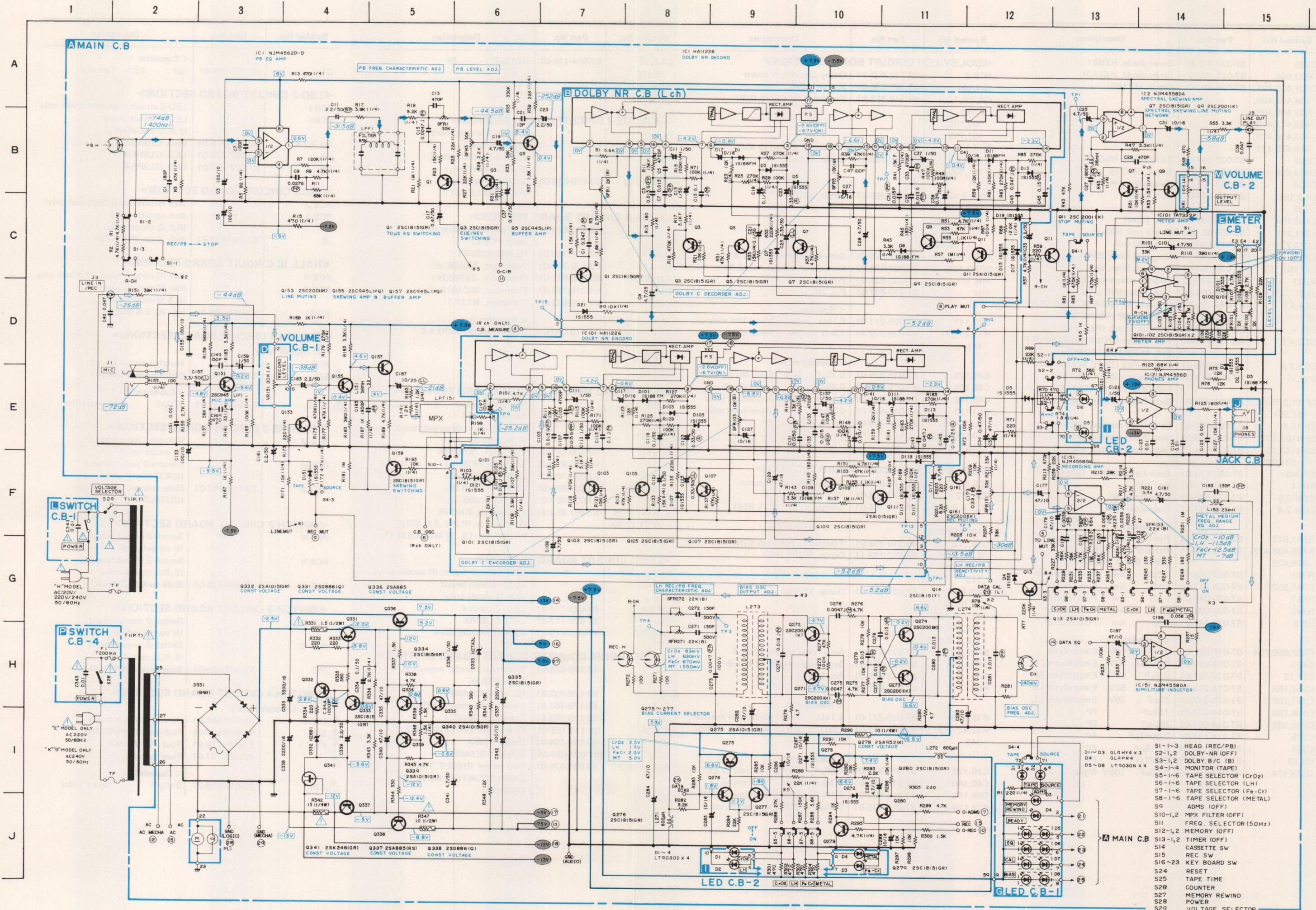
ACCESSORIES/PACKAGE

Ref. No.	Part No.	Part No. Changed to	Description	Common Model	Q'ty
1	82-179-856-01		Printed indiv., Packing	*	1
2	82-179-852-01		Cushion L, Printed indiv.	*	1
3	82-179-853-01		Cushion R, Printed indiv.	*	1
4	87-056-607-01		Poly-vinyl sack		1
5	87-051-135-11		Poly-vinyl sack (E,K,G model only)		1
6	87-051-131-11		Poly-vinyl sack (H model only)		1
7a	82-179-906-01		Instructions booklet(H model only)	*	1
7b	82-179-904-01		Instructions booklet(E model only)	*	1
7c	82-179-905-01		Instructions booklet(K model only)	*	1
7d	82-179-907-01		Instructions booklet(G model only)	*	1
8	87-056-009-41		Distributors list		1
9	87-056-008-01		Label AC power cord (K model only)		1
10	87-056-059-01		Guarantee card (G model only)		1
11	87-051-171-11		Poly-Vinyl sack		1
12	86-944-012-01		Connection cord, CW-129 BSK		2
13	87-032-845-01		Siemens plug (H model only)		1

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SCHEMATIC DIAGRAM-1

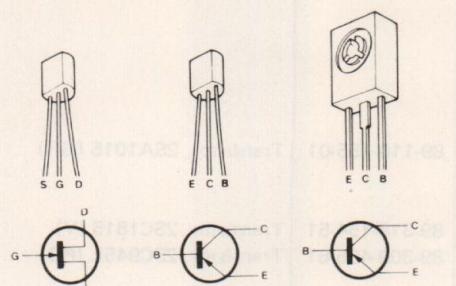


NOTES:

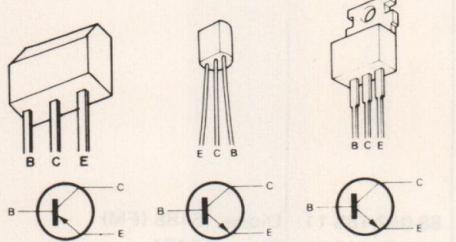
- 1) B (+) power supply B (-) power supply
- 2) → Signal path
→ Rec path
- 3) The voltage is the reference value measured with a tester (20 k-ohms/V DC) when there are no signals.
But () is with
An asterisk (*) indicates that the value was measured with a vacuum-tube voltmeter during recording.
- 4) Resistors with no designation have a rated power of 1/4W and a tolerance of $\pm 5\%$.
- 5) Capacitors with no designation have a dielectric strength of less than 50WV.
- 6) The only capacitor tolerance indicated are $\pm 5\%$ (J) and $\pm 10\%$ (K).
- 7) Ceramic capacitor symbols:
—II— High dielectric constant system (YY)
—II— High dielectric constant system (YW, YP, YZ)
- 8) Explanation of symbols
 - (M) Mylar capacitor
 - (A) Aluminum solid capacitor
 - (PP) Polypropylene film capacitor
 - (BP) Bi-polarized capacitor
 - (LL) Low-leakage capacitor
 - (T) Tantalum capacitor
 - (WR) Fuse resistor

 Safety component symbol
This symbol is given to important parts which serve to maintain the safety of the product, and which are made to conform to special safety specifications. Therefore, when replacing a component with this symbol, make absolutely sure that you use a designated part.

- The ICs on the electrical parts which are indicated by an **C** MOS IC symbol mark (④).
- This schematic diagram is subject to change without notice in the interests of improved performance.



2SK246 2SA945 2SA885
2SA1015
2SB598

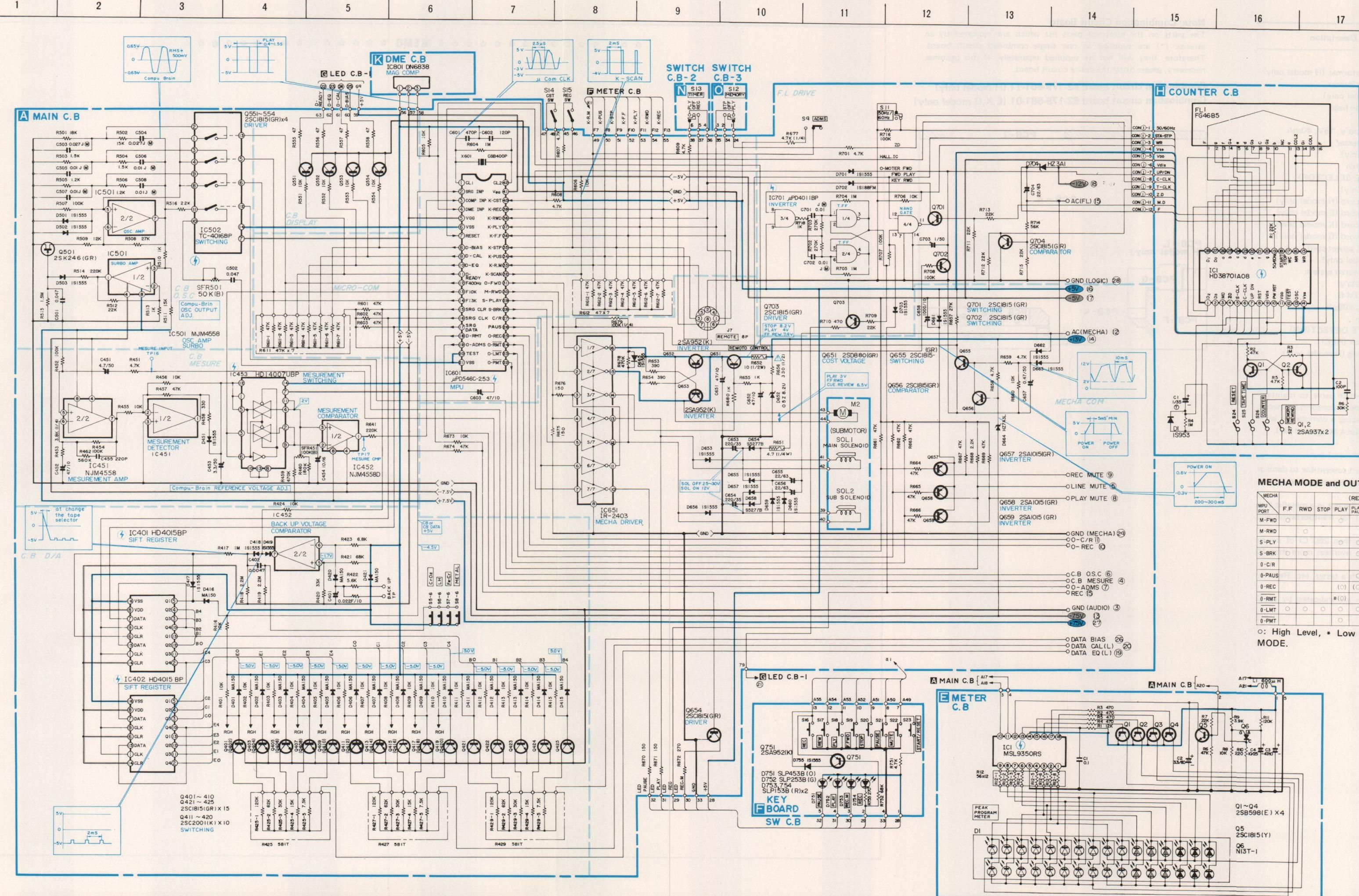


2SA937 2SC945 2SD880
2SC1815 2SD886
2SC2001

ELECTRICAL MAIN PARTS LIST

Symbol No.	Part No.	Description	Symbol No.	Part No.	Description	Symbol No.	Part No.	Description	Symbol No.	Part No.	Description	Symbol No.	Part No.	Description	
MAIN CIRCUIT BOARD SECTION»															
PCB-A	*	Main circuit board (H model only)	D332	87-027-475-01	Zener diode, HZ6B1	PCB-B	82-175-622-21	Dolby-Lch circuit board	C4,8,32,	87-014-118-01	0.015μF PP	C1	82-179-705-01	<Capacitor>	
PCB-A	*	Main circuit board (E,K,G model only)	D333,664	87-027-399-01	Zener diode, HZ7A3L	IC1,101	87-027-738-01	IC, HA11226	36,104,			1μF 35V Tantalum			
IC1	87-027-814-01	IC, NJM4562D-D	D401,402,403,	87-027-219-01	Diode, MA150	Q1,3,5,7,	89-318-155-01	Transistor, 2SC1815 (GR)	108,132,						
IC2,151,	87-027-371-01	IC, NJM4558DA	404,405,406,			9,101,			136						
152			407,408,409,			103,105,									
IC101	87-027-726-01	IC, TA7332P	410,411,412,			107,109									
IC121	87-027-739-01	IC, NJM4556D	413,414,415,												
④ IC401,402	87-027-799-01	IC, HD14015BP	416,420,421												
IC451,452,	87-027-235-01	IC, NJM4558	D652	87-027-244-01	Zener diode, 05Z8.2U	Q11,111	89-110-155-01	Transistor, 2SA1015 (GR)	PCB-D	*	Volume-1 circuit board	LED-2 CIRCUIT BOARD SECTION»			
501			D654,658	87-027-365-01	Diode, S5277B	D19,11,	88-052-188-11	Diode, 1S188 (FM)	PCB-D	*	Volume-1 circuit board	PCB-I	*	LED-2 circuit board (H model only)	
④ IC453	87-027-800-01	IC, HD14007UBP	D704	87-027-301-01	Zener diode, HZ3A	101,109,			VR151,152	82-179-618-01	Slide volume, 10kΩ-A (RECORD LEVEL)	PCB-I	*	LED-2 circuit board (E,K,G model only)	
④ IC502	87-027-429-01	IC, TC4016BP	L1,2,151,	87-005-147-01	Coil, 36mH	111						D1,2,3,4	87-027-775-01	LED, LT9030DI	
④ IC601	82-179-626-01	IC, μPD546C-253	L153,154	87-005-148-01	Coil, 23mH	D3,5,7,13,	87-027-097-01	Diode, 1S1555	PCB-D	*	Volume-1 circuit board	D5	87-027-773-01	LED, GL9NG4	
IC651	87-027-426-01	IC, IR-2403	L271,272	82-401-661-01	Choke coil, 600μH	15,17,19,			VR151,152	82-179-618-01	Slide volume, 10kΩ-A (RECORD LEVEL)	D6	87-027-772-01	LED, GL9PR4	
④ IC701	87-027-706-01	IC, μPD-4011BP	L273,274	82-179-633-01	Bias OSC coil	21,103,105,									
Q1,2,3,4,	89-318-155-01	Transistor, 2SC1815 (GR)	LPF1	87-008-243-01	Low-pass filter, 85K x 2	107,113,115,									
7,8,101,			LPF151,152	87-030-061-01	Low-pass filter, 85K	117,119,121									
102,159,160,			X601	87-008-236-01	Ceramic resonator CSB400P	SFR1,101	87-021-626-01	Semi-fixed resistor, 2kΩ-B	IC1	87-027-725-01	LED display module ass'y (with/PCB-E)				
276,277,279,			J1,2	82-168-634-01	Jack, 6.3φ (MIC L,R)	SFR3,103	87-021-634-01	Semi-fixed resistor, 10kΩ-B	Q1,2,3,4	82-179-708-01	IC, MSL9350RS	J8	82-168-633-01	Jack, 6.3φ (PHONES)	
280,333,334,			J3,4,5,6	87-049-055-01	Pin jack, 4P (LINEIN, LINE OUT)	PIN	87-032-635-01	Pin, 5P	(Q1,2,3,4)	(89-109-521-01)	Transistor, 2SB598 (E)				
335,401,402,			J7	87-032-985-01	DIN jack, 8P (REMOTE)	PIN	87-032-637-01	Pin, 7P	Q5	89-318-154-51	Transistor, 2SC1815 (Y)				
403,404,405,			S1	82-179-628-01	Remote switch (REC/PB)	R17,117	87-025-271-01	5.1kΩ 1/4W Metal film resistor	Q6	82-179-673-01	Transistor, N13T-1				
406,407,408,			S2,3,4,9	82-179-620-01	Push-switch (DOLBY-NR ON/OFF, B/C, MONITOR, ADMS)	R11,41,111	87-025-272-01	13kΩ 1/4W Metal film resistor	R12-1,12-2,	82-179-709-01	Resistor block, 560Ω x 8				
409,410,421,			S5,6,7,8	82-179-619-01	Push-switch (TAPE SELECTOR)	C25,125	87-015-329-01	<Capacitors>	12-3,12-4,						
422,423,424,			S10,11	87-031-650-01	Slide switch (MPX FILTER, FREQUENCY SELECTOR)	C39,139	87-015-895-01	0.33μF 50V Electrolytic LL	12-5,12-6,						
425,551,552,			SFR1,2,151,	87-021-624-01	Semi-fixed resistor, 50kΩ-B	C45,145	87-015-427-01	0.15μF 25V Aluminum solid	12-7,12-8						
553,554,654,			SFR3,4	87-021-687-01	Semi-fixed resistor, 30kΩ-B	C23,123	87-015-429-01	0.33μF 25V Aluminum solid							
655,656,701,			SFR101,102	87-021-688-01	Semi-fixed resistor, 2kΩ-B	C3,7,31,35,	87-014-118-01	0.015μF PP							
703,704			SFR153,154	87-021-614-01	Semi-fixed resistor, 22kΩ-B	Q751	89-109-521-01	Key-board switch circuit board (H model only)							
Q5,6,151,	89-309-456-01	Transistor, 2SC945L (P)	271,272			D751	89-109-521-01	Key-board switch circuit board (E,K,G model only)							
152			SFR451	87-021-570-01	Semi-fixed resistor, 100kΩ-B	D752	87-027-810-01	Transistor, 2SA952K							
Q9,10,11,12,	89-320-011-01	Transistor, 2SC2001 (K)	PIN-1	87-032-912-01	Pin, 12P	PCB-C	82-175-622-21	Dolby-Rch circuit board	PCB-M	*	Volume-2 circuit board (H model only)				
153,154,161,			CON-3,5	87-032-575-01	Connector, 5P	IC2,102	87-027-738-01	IC, HA11226	PCB-M	*	Volume-2 circuit board (E,K,G model only)				
162,271,272,			CON-2,4	87-032-577-01	Connector, 7P	Q2,4,6,8,	89-318-155-01	Transistor, 2SC1815 (GR)	PCB-M	*	Volume-2 circuit board (E,K,G model only)				
273,274,411,			R611,612	82-179-631-01	<Resistors>	10,102,104,			VR1,2	82-179-617-01	Slide volume, 30kΩ-A (OUTPUT LEVEL)				
412,413,414,			R425,426,427,	82-179-632-01	Resistor block 47kΩ x 7	106,108,110									
415,416,417,			428,429		Resistor block 7.5kΩ, 15kΩ, 30kΩ, 62kΩ, 120kΩ	Q12,112	89-110-155-01	Transistor, 2SA1015 (GR)							
418,419,420,			R331	87-029-066-01	1.5Ω 1/4W Fuse resistor	D2,12,10,	88-052-188-11	Diode, 1S188 (FM)							
Q13,275,332,	89-110-155-01	Transistor, 2SA1015 (GR)	R347,652	87-029-117-01	10Ω 1/4W Fuse resistor	102,110,									
339,340,657,			R651	87-029-089-01	4.7Ω 1/4W Fuse resistor	112									
658,659			R342	87-029-094-01	15Ω 1/4W Fuse resistor	D4,6,8,14,	87-027-097-01	Diode, 1S1555							
Q14,702	89-318-154-51	Transistor, 2SC1815 (Y)	R5,6	87-025-274-01	82Ω 1/4W Fuse resistor	16,18,20,									
Q155,156,157,	89-309-455-61	Transistor, 2SC945L (PQ)	C655,656,704	87-015-885-01	<Capacitors>	22,104,106,									
158			C401	87-015-919-01	22μF 63V Electrolytic	108,114,116,									
Q278,652,653	89-109-521-01	Transistor, 2SA952K	C11,12	87-015-387-01	0.022μF 10V Electrolytic	118,120,122									
Q331,651	89-408-862-01	Transistor, 2SD886 (Q)	C157,158	87-015-243-01	2.2μF 50V Electrolytic BP	SFR2,102	87-021-626-01	Semi-fixed resistor, 2kΩ-B	PCB-G	*	LED-1 circuit board (H model only)				
Q336,337	89-108-854-51	Transistor, 2SA885R (S)	C167,168												

SCHEMATIC DIAGRAM-2

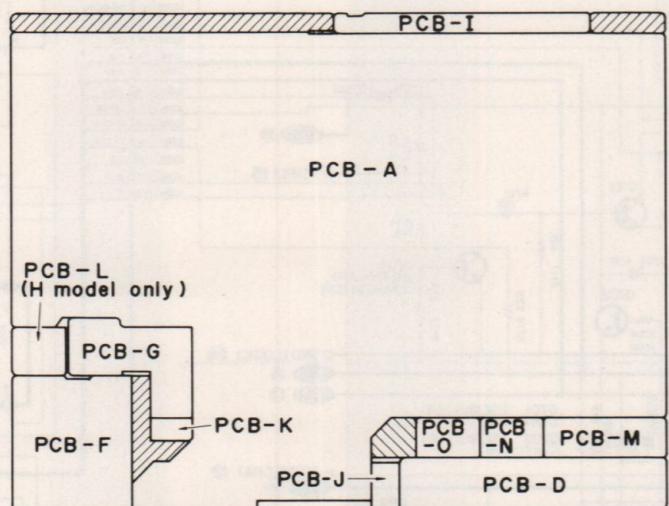


Symbol No.	Part No.	Description
<<Miscellaneous>>		
 T1	82-179-615-01	Power transformer (H model only)
 T1	82-179-614-01	Power transformer (E,K,G model only)
PH,EH	87-046-194-01	Combination head
EH	87-046-192-01	Erase head
PL1	82-179-623-01	Pilot lamp ass'y, 15V, 40mA
	87-033-140-01	Splice connector (H model only)
 S29	87-031-586-01	Rotary switch (VOLTAGE SELECTOR) (H model only)
	87-034-826-01	AC power cord (H model only)
	87-034-877-01	AC power cord (E model only)
	87-034-872-01	AC power cord (K model only)
	87-034-892-01	AC power cord (G model only)
	87-085-166-01	Holder, AC power cord (E,K,G model only)
M1	87-045-175-01	DC motor, servo system
M2	87-045-164-11	DC motor ass'y
SOL1,2	82-179-630-01	Solenoid, DM-6
L1	82-401-661-01	Choke coil, 600 μ H
S14	82-283-631-01	Leaf switch (CASSETTE DETECTION)
S15	87-031-610-01	Micro switch (REC)
	87-085-165-01	Cord bushing (H model only)

Note; Combination Circuit Board

The parts on the electrical parts list which are indicated by an asterisk (*) are supplied as one single combined circuit board. Therefore, they will not be supplied separately. If this becomes necessary, please order the entire circuit board.

Combination circuit board 82-179-601-11 (H model only)
Combination circuit board 82-179-681-01 (E.K.G model only)



 Safety component symbol

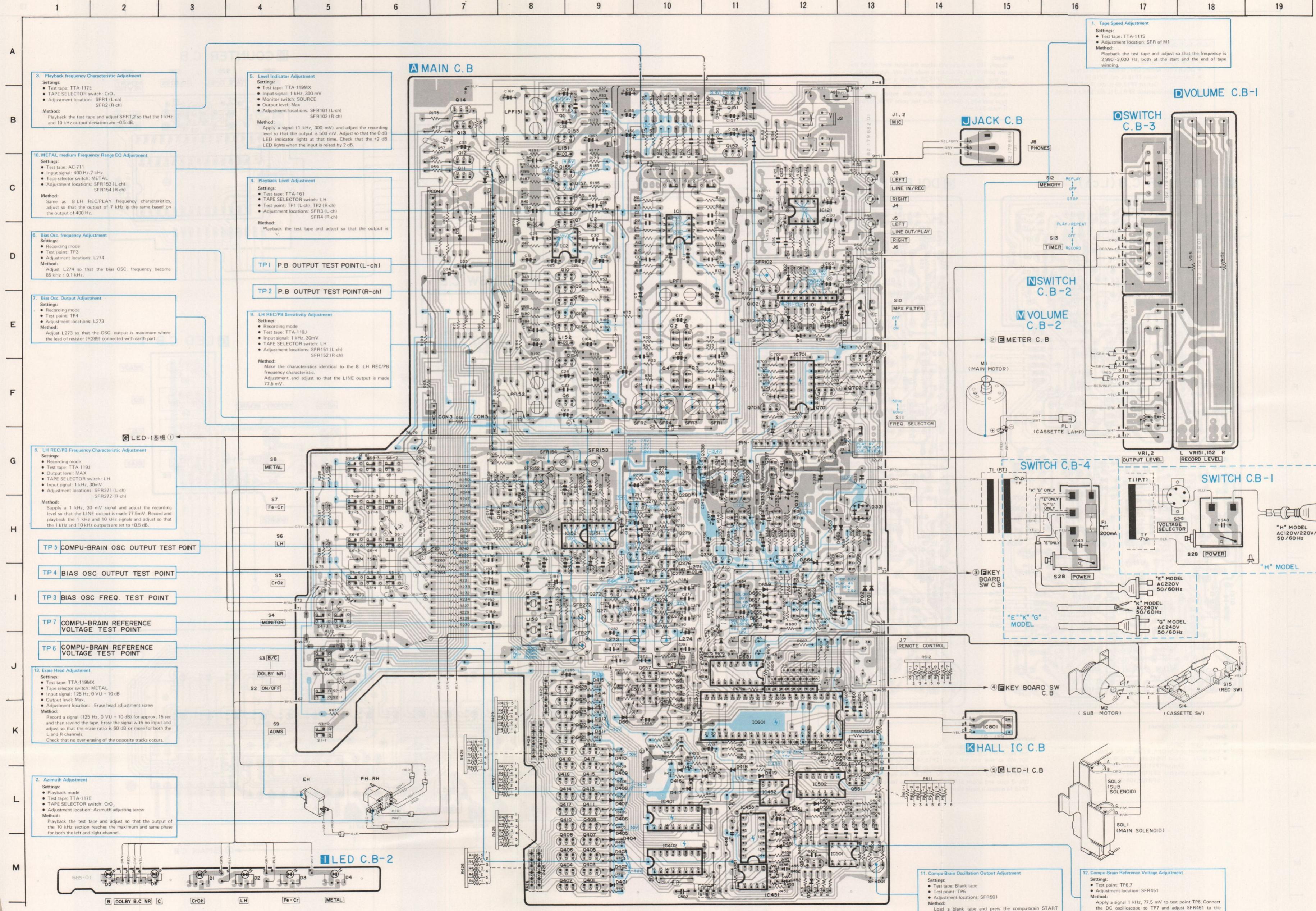
This symbol is given to important parts which serve to maintain the safety of the product, and which are made to conform to special safety specifications. Therefore, when replacing a component with this symbol, make absolutely sure that you use a designated part.

C-MOS IC handling precaution

The C-MOS IC's construction makes this part susceptible to damage by static electricity and so take sufficient care in regard to following articles.

1. Need to be put on conductive sheet, to be put in a metallic box and to be wrapped by aluminium foil for transportation and deposit.
2. To use solder iron less than 40W (less than 260°C) of power consumption for soldering. But do not overheat more than 10 second.
3. Do not perform a conductivity test with a tester, etc. Refer to the circuit voltages of each part.
4. The ICs on the electrical parts which are indicated by an C-MOS IC symbol mark ().

WIRING-1



WIRING-2

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19

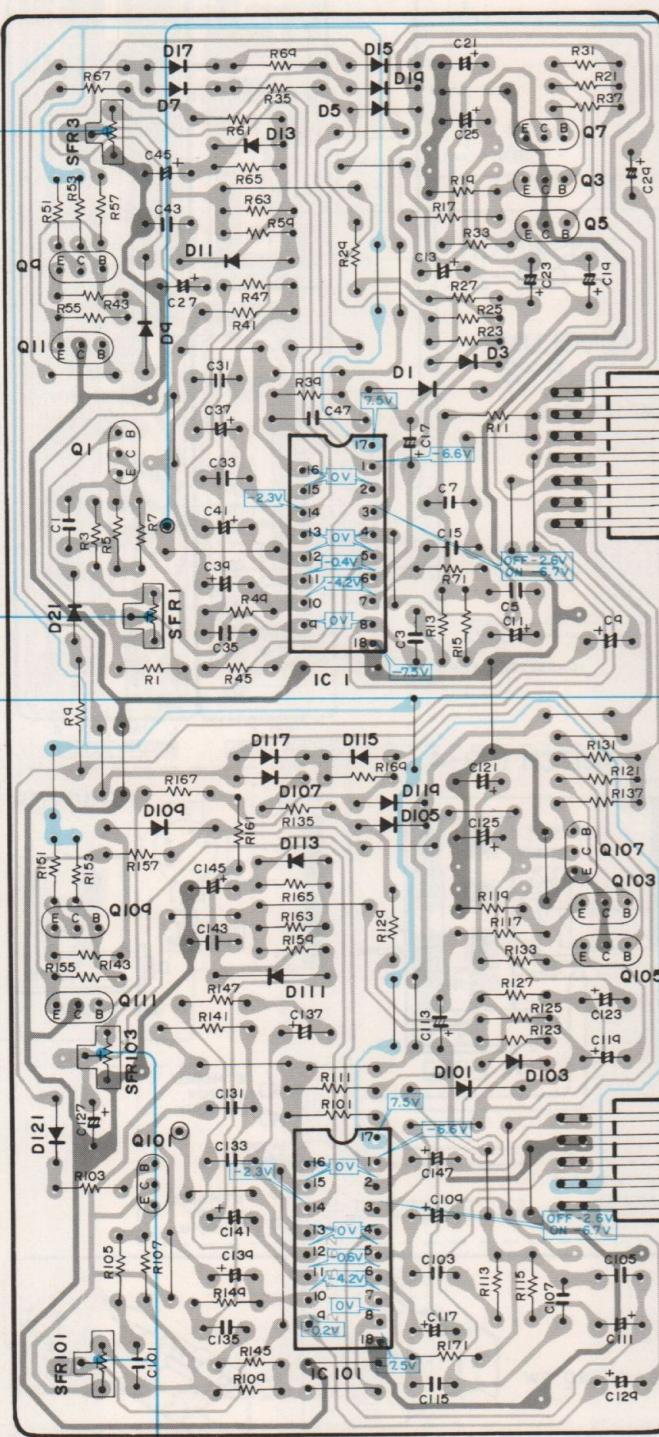
A

15. Dolby C Decoder Adjustment

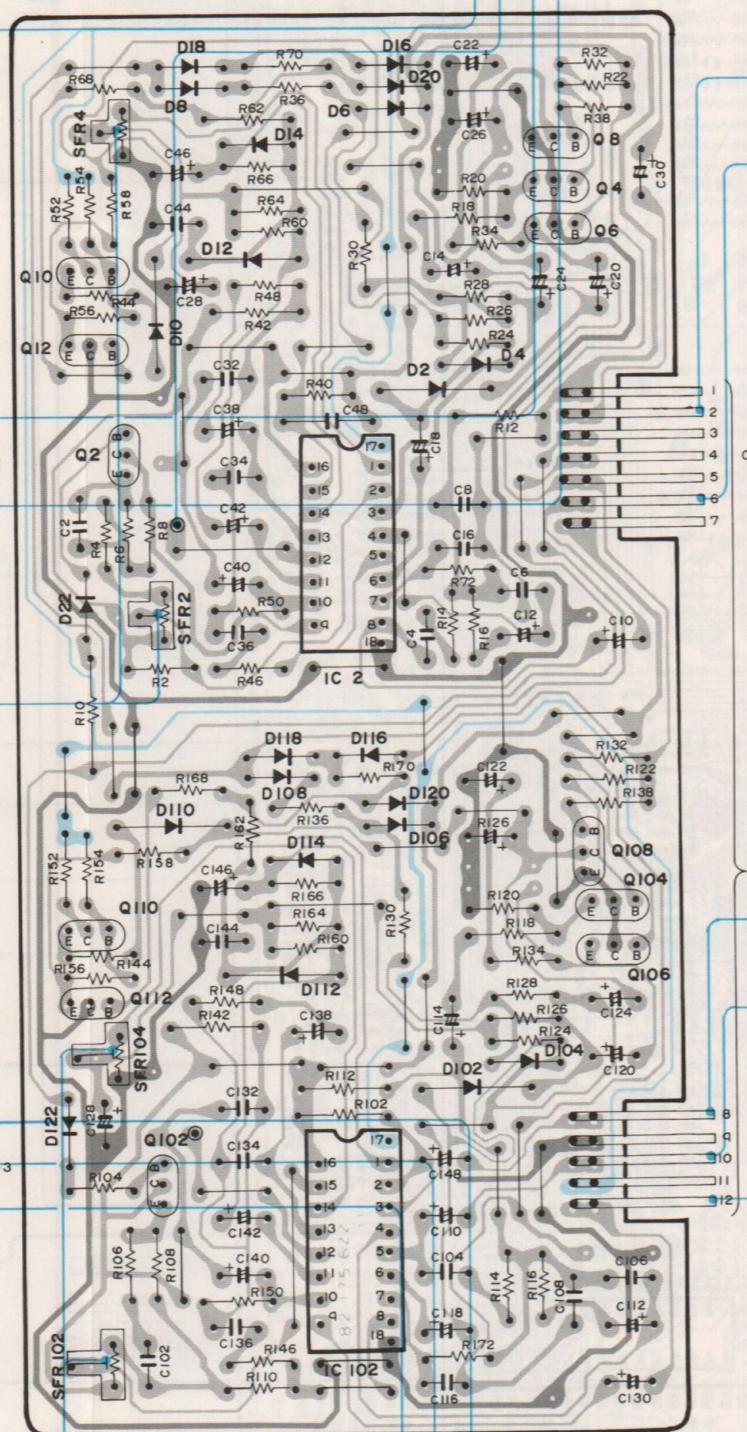
Settings:
 • Input signal: 700 Hz
 • DOLBY-NR switch: OFF, B type → ON, C type
 • Test point: Input TP15 (L-ch), TP16 (R-ch)
 • Output TP17,19 (L-ch), TP18,20 (R-ch)
 • Adjustment locations: SFR1,3 (L-ch), SFR2,4 (R-ch)

Method:
 Supply 700 Hz signal and adjust the input level so that the test point TP17,18 output is made 775 mV. Adjust SFR1,3 so that the test point TP19,20 output is made 775 mV. Next adjust the input level so that the point TP19,20 output is made 83 mV. DOLBY-NR switch to ON, C type and adjust SFR2,4 so that test point TP19,20 output is made 23.5 mV.

B DOLBY NR C.B (Lch)



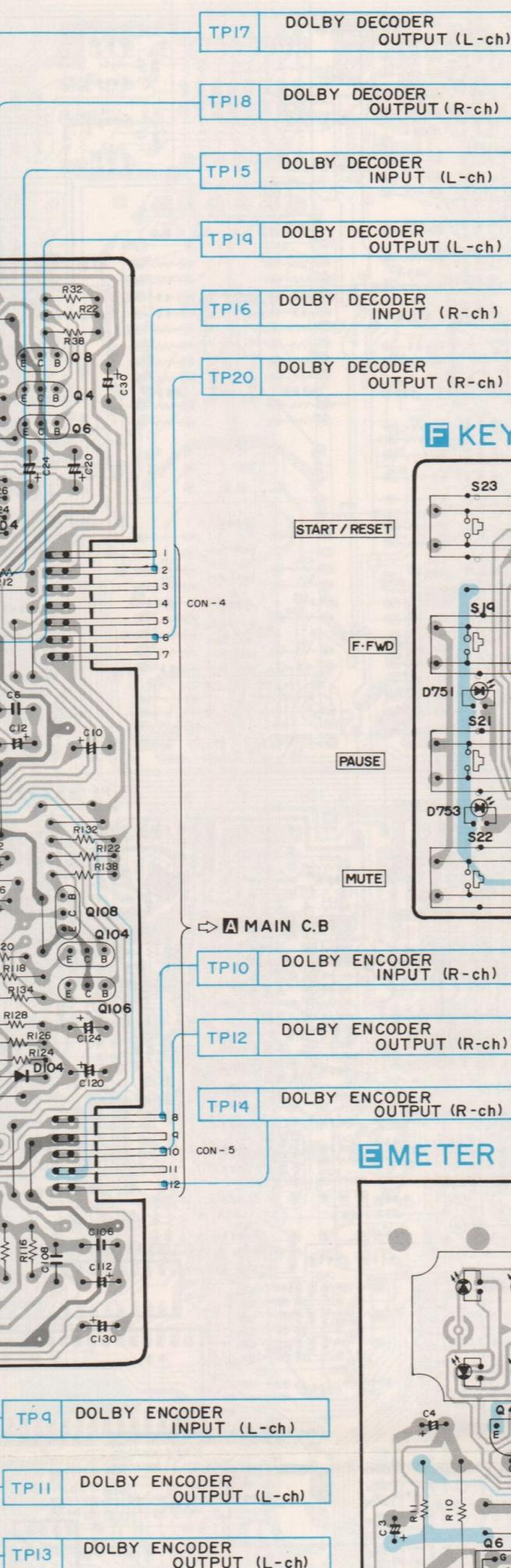
C DOLBY NR C.B (Rch)



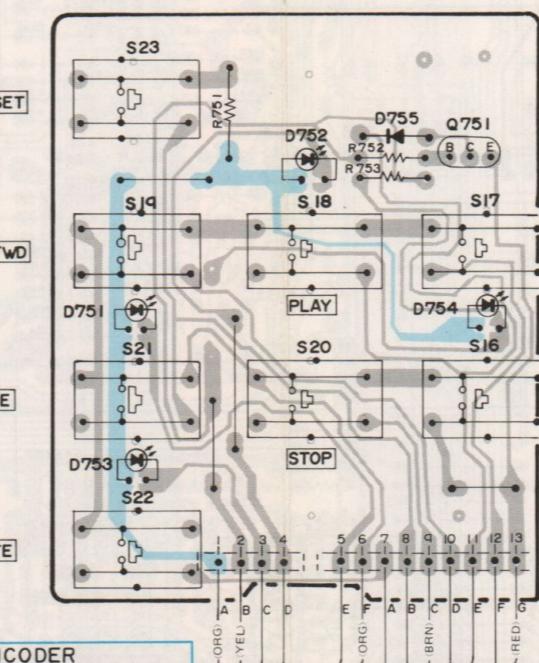
14. Dolby C Encoder Adjustment

Settings:
 • Input signal: 700 Hz
 • DOLBY-NR switch: OFF, B type → ON, C type
 • Test point: Input TP9 (L-ch), TP10 (R-ch)
 • Output TP11,13 (L-ch), TP12,14 (R-ch)
 • Adjustment locations: SFR101,103 (L-ch), SFR102,104 (R-ch)

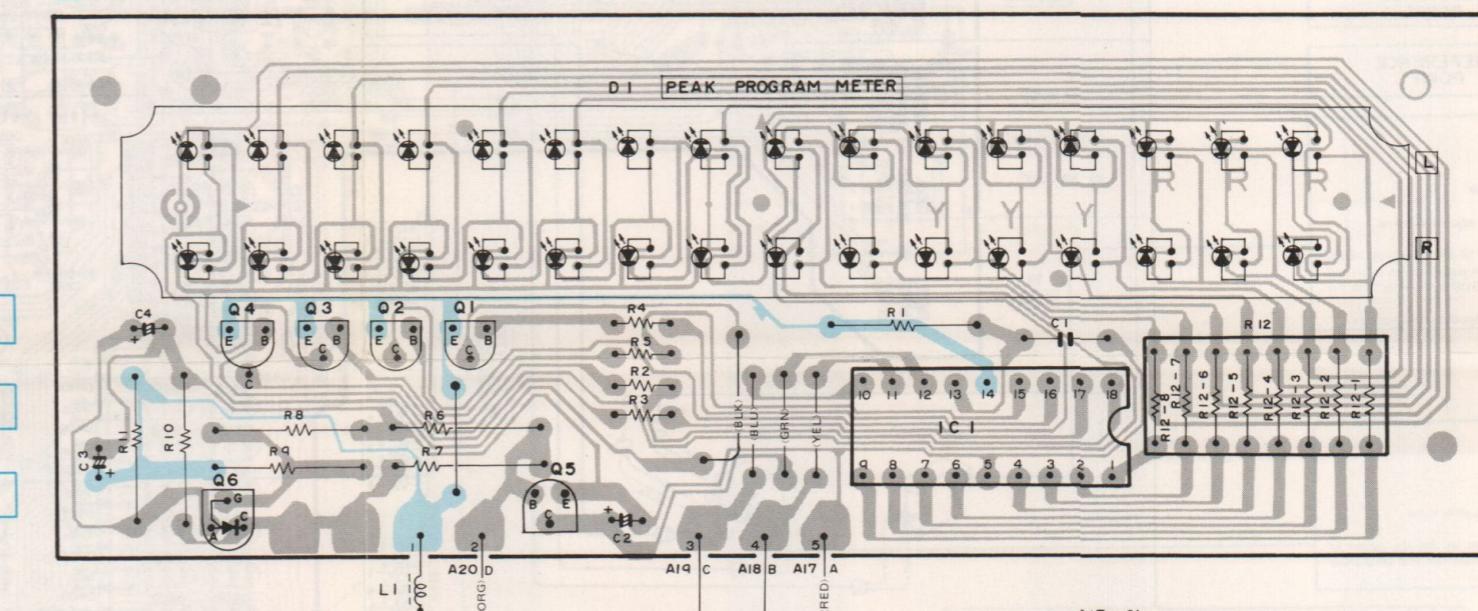
Method:
 Supply a 700 Hz signal and adjust the input level so that the test point TP11,12 output is made 775 mV. Adjust SFR102 so that the test point TP13,14 output is made 775 mV. Next adjust the input level so that the test point TP13,14 output is made 23.5 mV. DOLBY-NR switch to ON, C type and adjust SFR103,104 so that the test point TP13,14 output is made 83 mV.



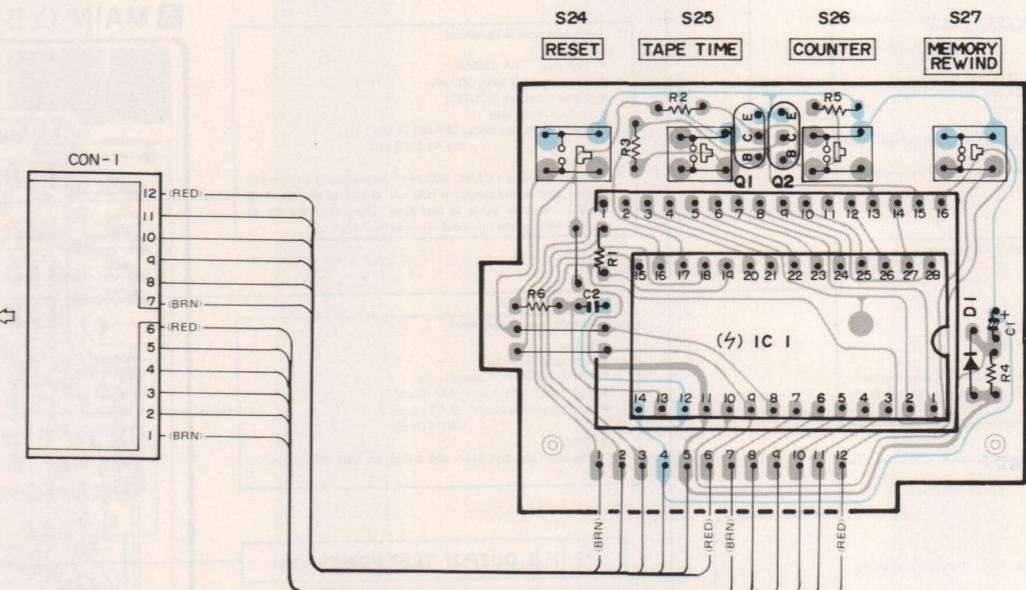
F KEY BOARD SW C.B



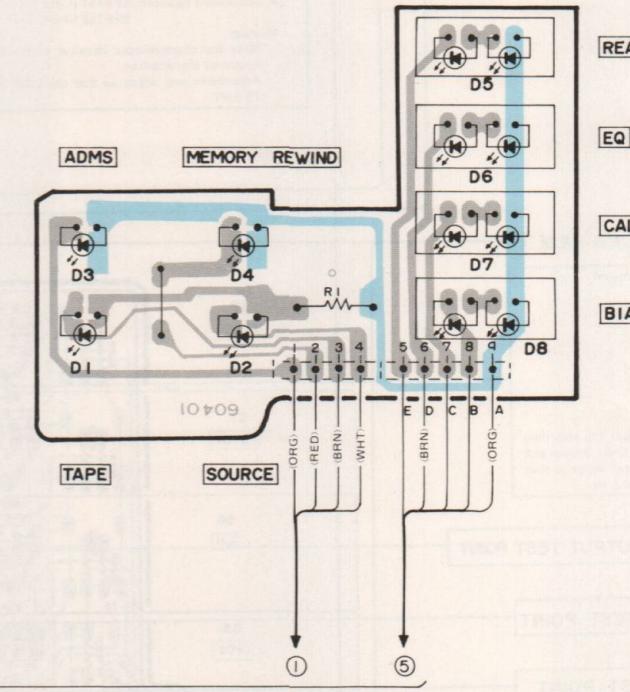
E METER C.B



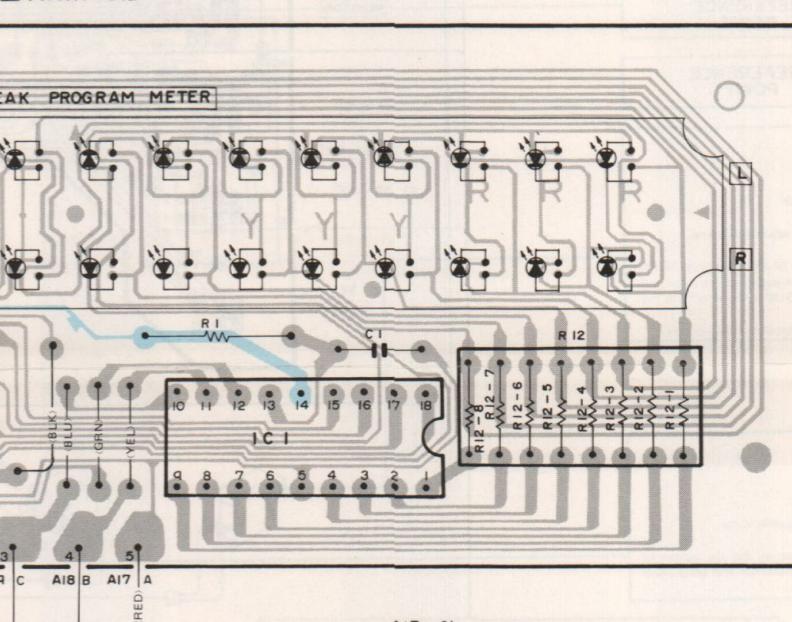
H COUNTER C.B



G LED C.B-1



A MAIN C.B



11. Timing charts

11-1. Bias adjustment

• BIAS ADJUSTMENT

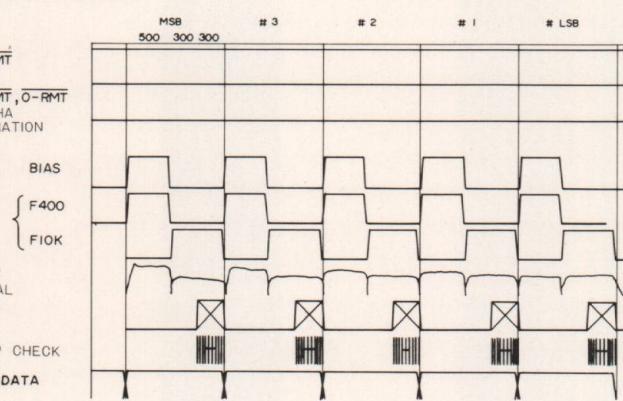


Fig. 31

11-2. Transfer from STOP mode

• STOP → PLAY or (REC/PLAY) KEY=PLAY or REC/PLAY

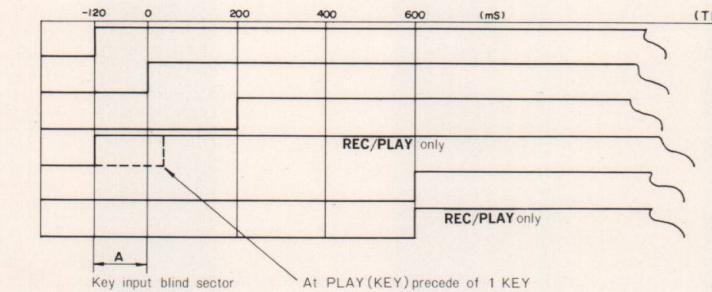


Fig. 32

• STOP → RWD KEY=RWD

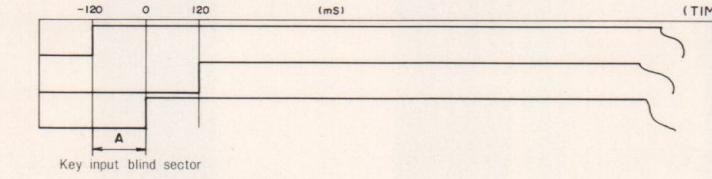


Fig. 33

• STOP → FF KEY=FF

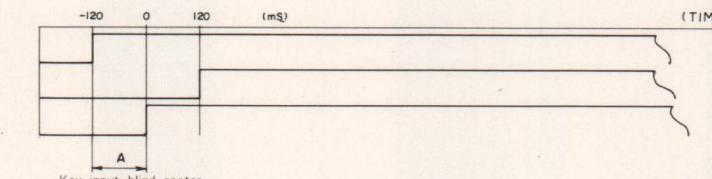


Fig. 34

• STOP → REC KEY=REC

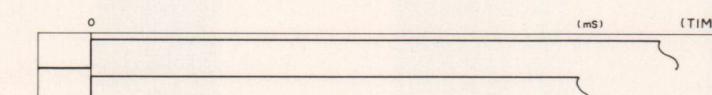


Fig. 35

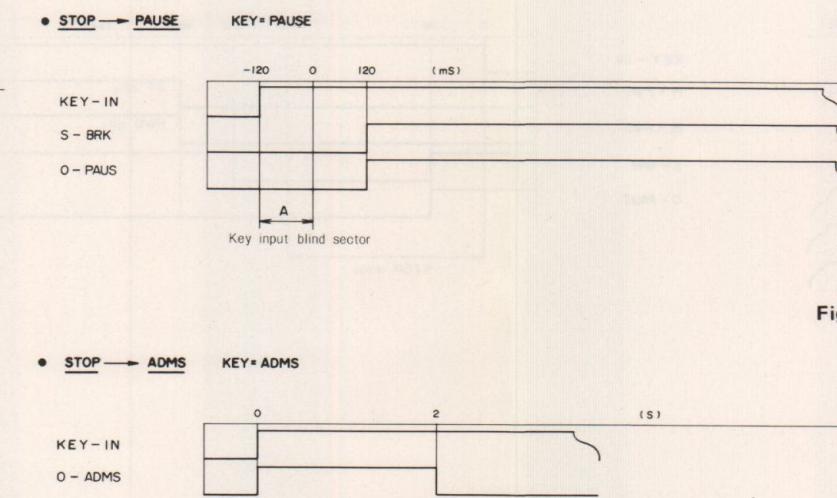


Fig. 36

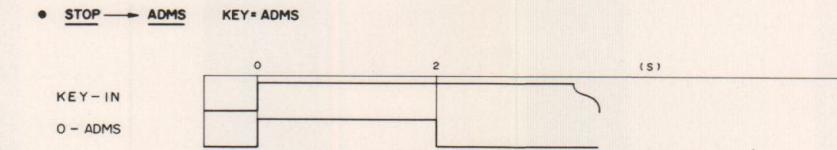


Fig. 37

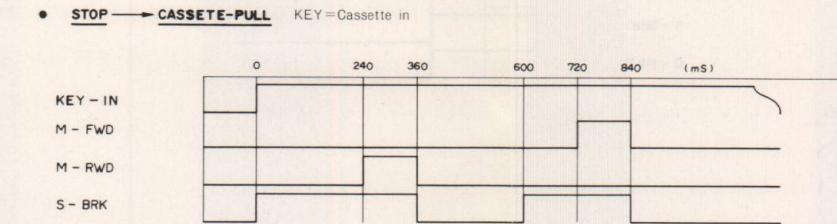


Fig. 38

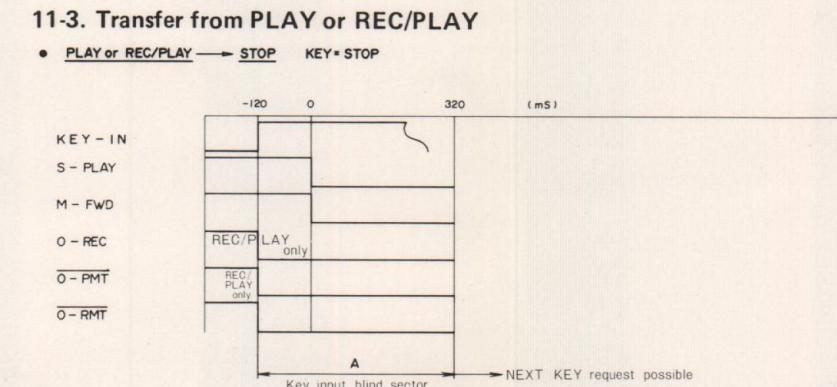


Fig. 39

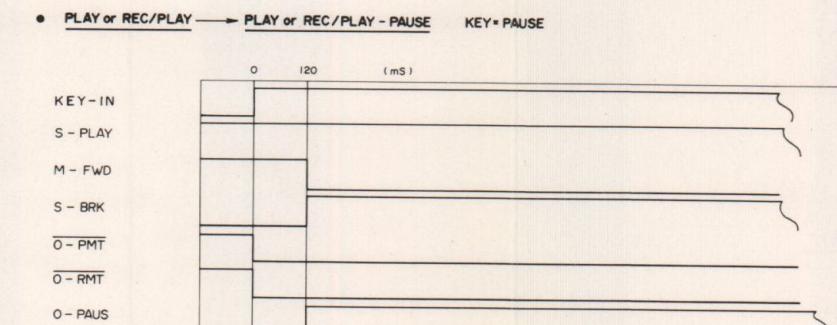


Fig. 40

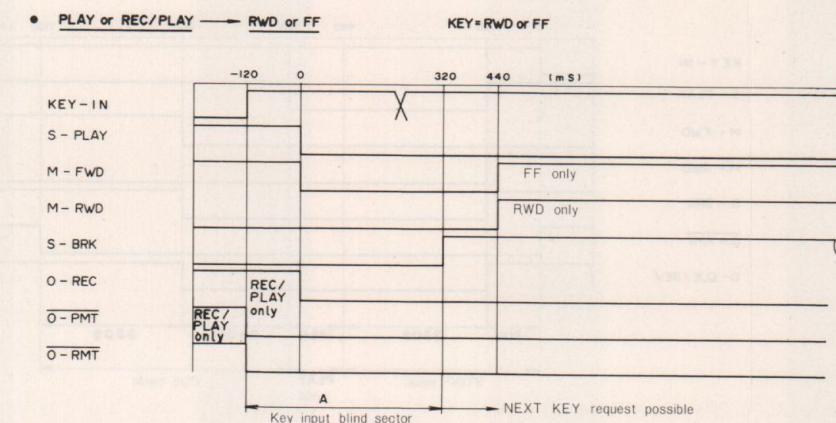


Fig. 41

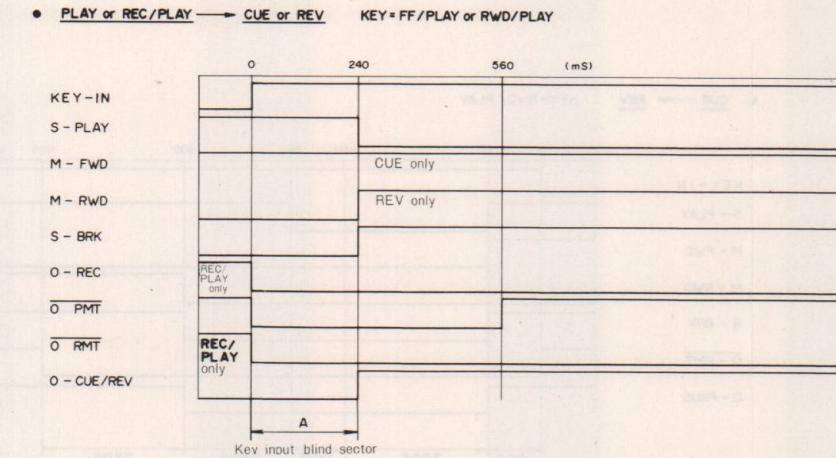


Fig. 42

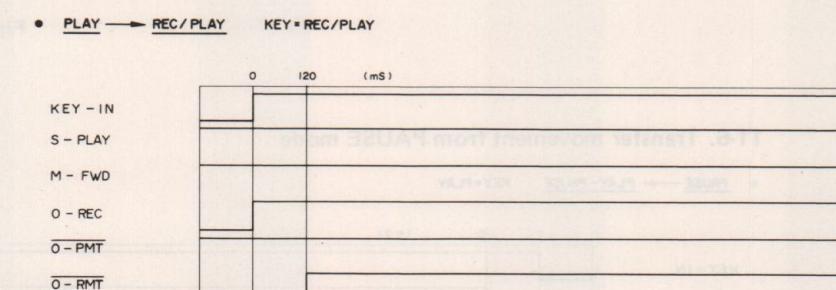


Fig. 43

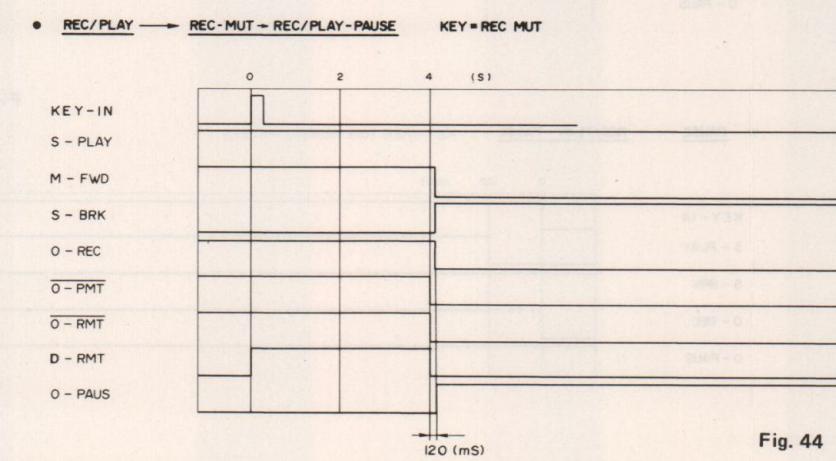


Fig. 44

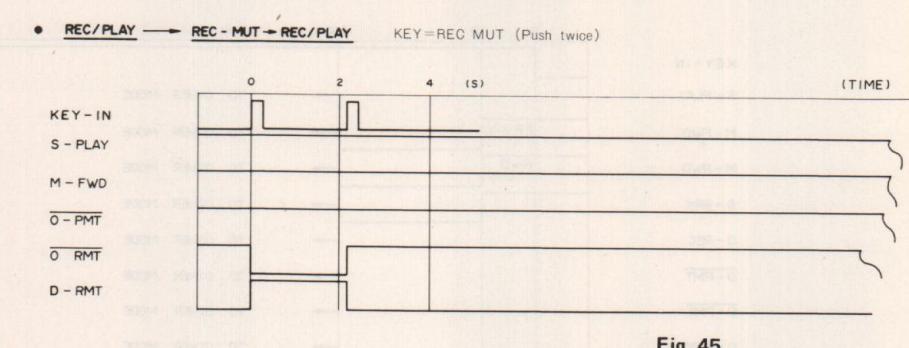


Fig. 45

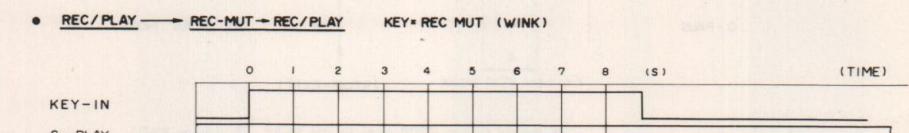


Fig. 46

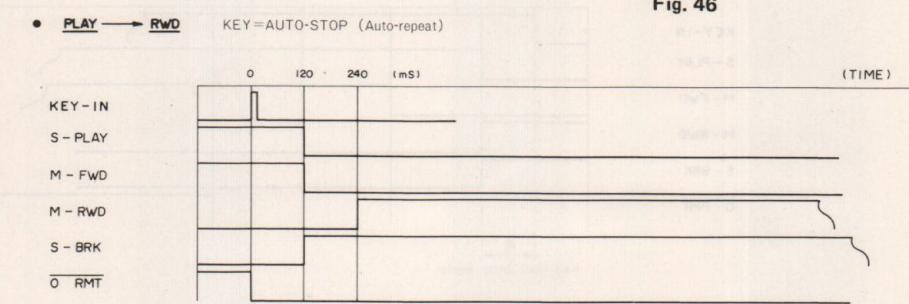


Fig. 47

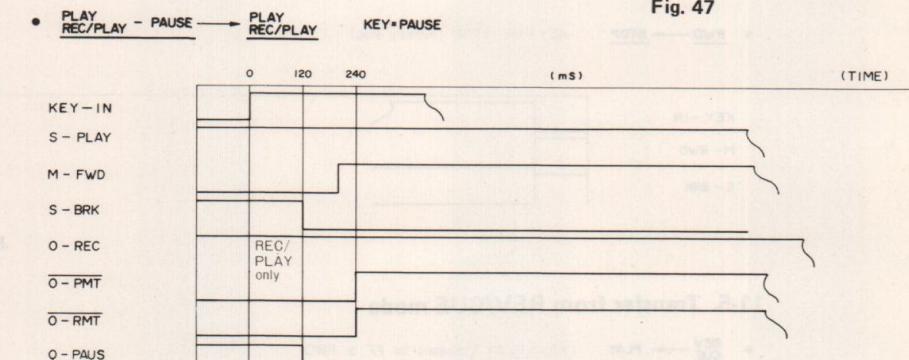


Fig. 48

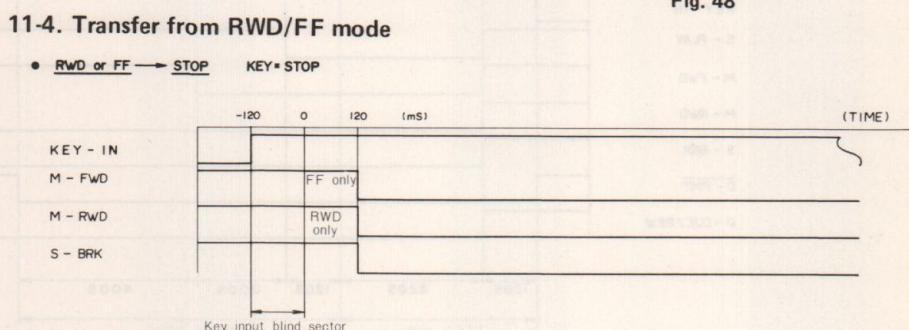
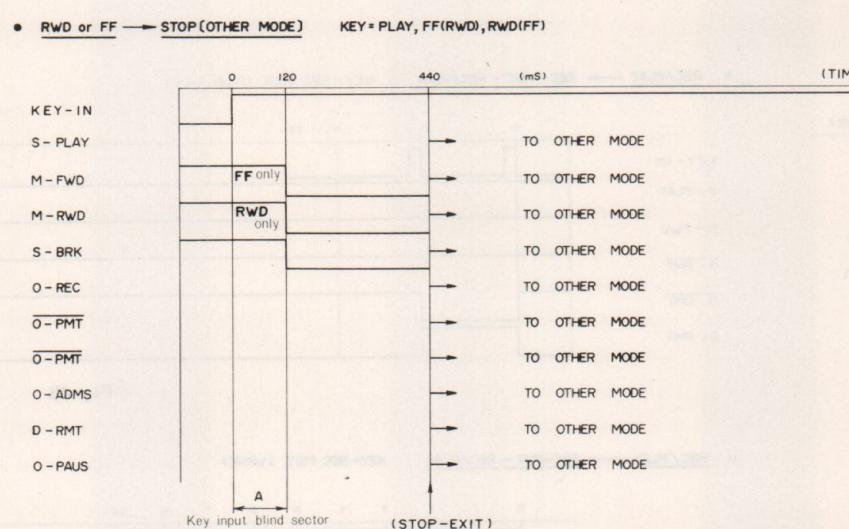


Fig. 49



• Passes through STOP mode for the PLAY, FF (during RWD), RWD (during FF) mode.

Fig. 50

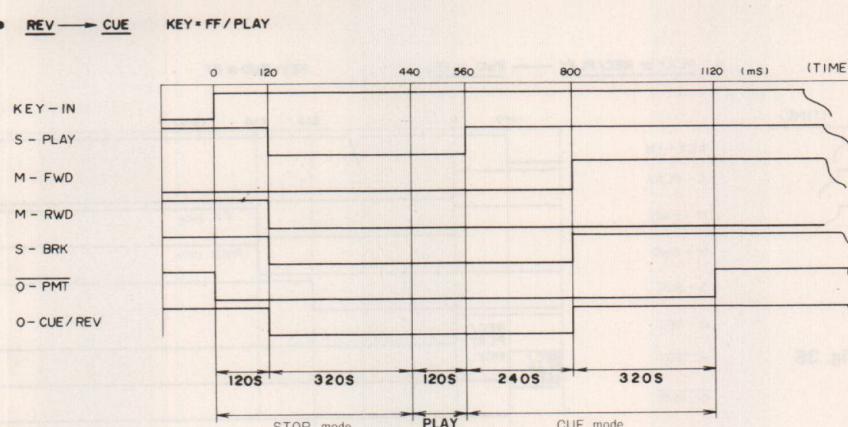


Fig. 54

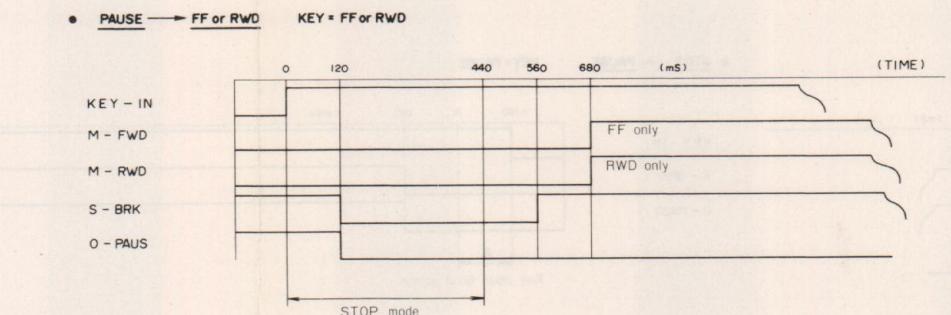


Fig. 58

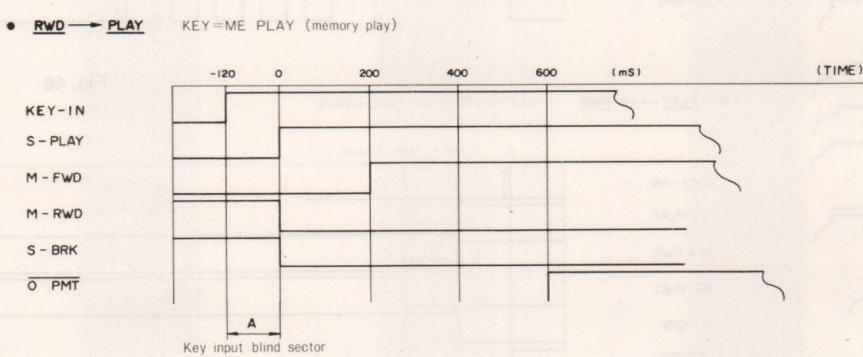


Fig. 51

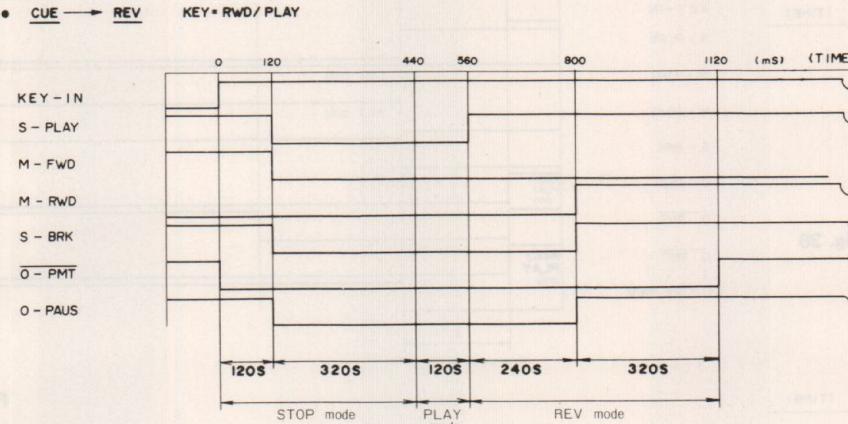


Fig. 55

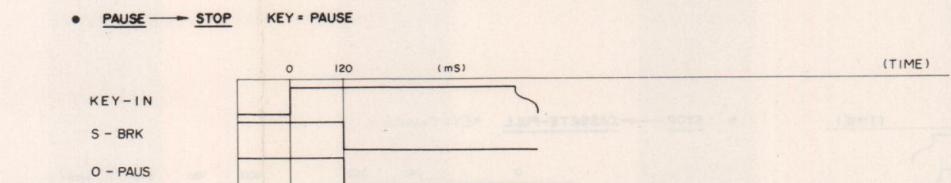


Fig. 59

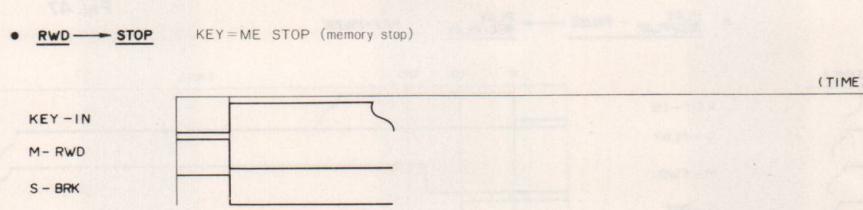


Fig. 52

11-5. Transfer from REV/CUE mode

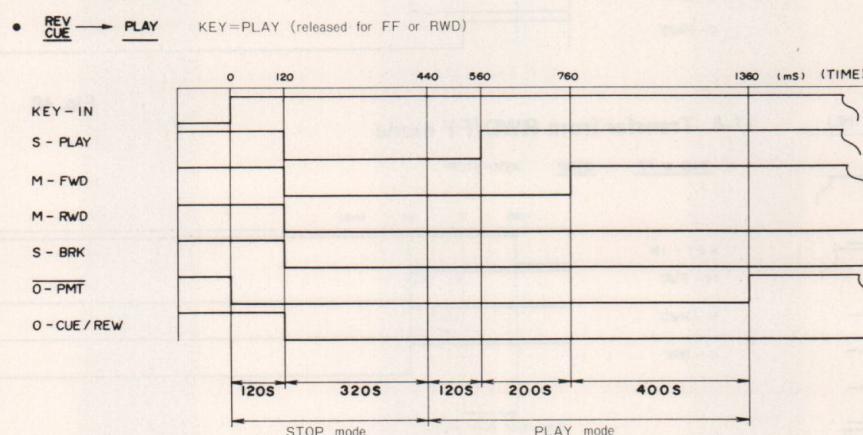


Fig. 53

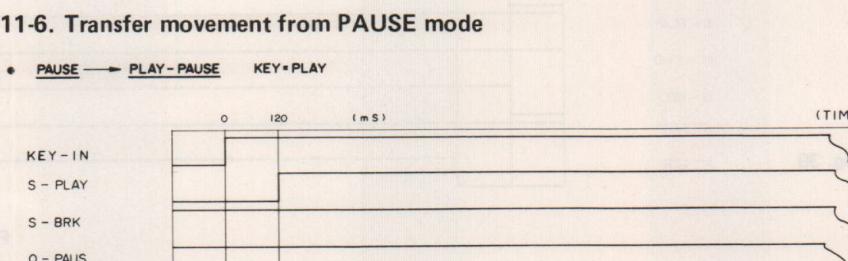


Fig. 56

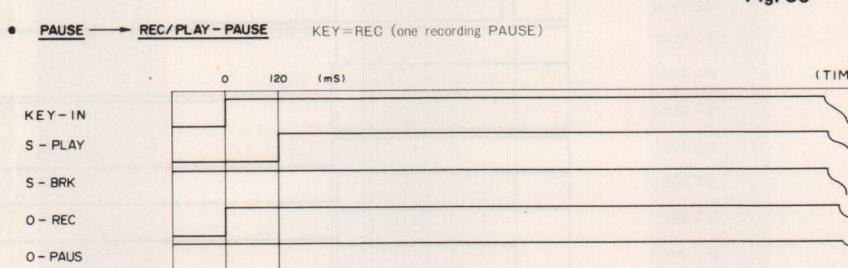


Fig. 58