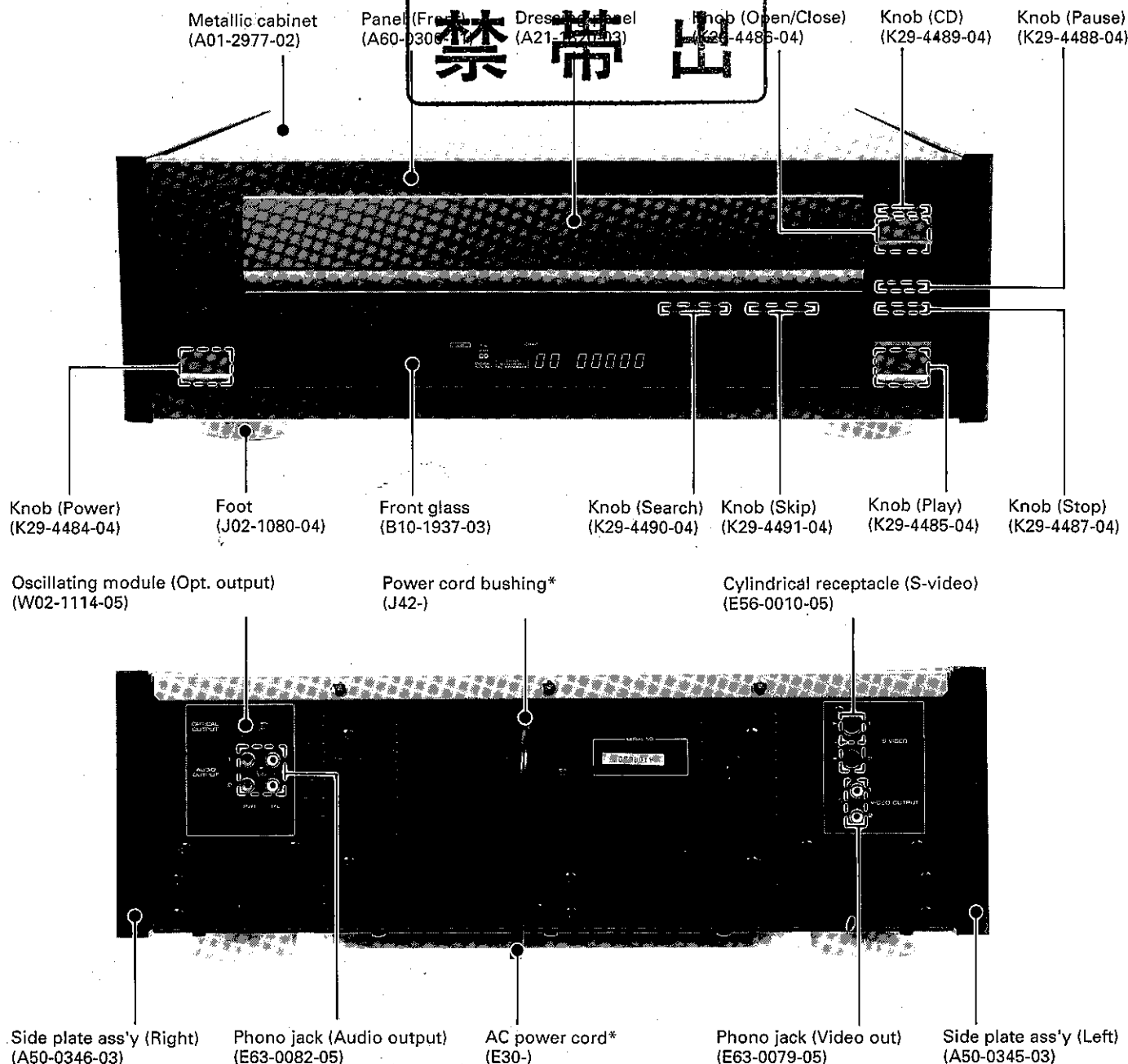


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DANGER: Laser radiation when open and interlock defeated. AVOID DIRECT EXPOSURE TO BEAM.

***Refer to parts list on page 119.**

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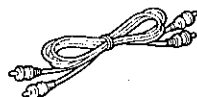
NOTE : Refer to the following service manual, if need description about item of table.

Unit	Ref No.	Parts No.	Function name	Reference service manual	Reference page
X29-2380	IC7	TC5081AP	Phase comparator	LVD-300/700 CIRCUIT DESCRIPTION	P.128
	IC8	HD49403NT	Disc servo	LVD-310/V7	P.31
	IC10	PD0011A	24-bit data decoder	LVD-310/V7	P.35
	IC20	HA11529	Servo IC	LVD-320	P.22
X32-2350	IC3	CA0002AM	Analog audio signal processor	LVD-320	P.24
	IC4	CXD2500BQ	Digital signal processor	LVD-320	P.25
	IC10	SM5813APT	Digital filter	LVD-300/700 CIRCUIT DESCRIPTION	P.103
	IC3	YM3558	Video FM signal demodulation	LVD-320	P.30
X35-2100	IC4	HA11528	Video signal processor	LVD-310/V7	P.28
	IC6	LVA519S	SYNC SEP	LVD-300/700 CIRCUIT DESCRIPTION	P.89
	IC21	M50554-270SP	Display IC	LVD-310/V7	P.32
	IC5, IC6	CXK1206M	Memory IC	LVD-300/700 CIRCUIT DESCRIPTION	P.67
X35-2110	IC7, IC8	MN4760S	Memory IC	LVD-300/700 CIRCUIT DESCRIPTION	P.91

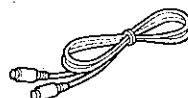
Service Manual parts No. : LVD-300/700 CIRCUIT DESCRIPTION (B51-4163-00), LVD-310/V7 (B51-4409-00), LVD-320 (B51-4629-00)

ACCESSORIES

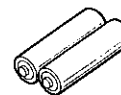
• Audio cord 1
(E30-2600-05)



• Video cord 1
(E30-2725-05)



• Battery ("R03" or "AAA") 2
(-)



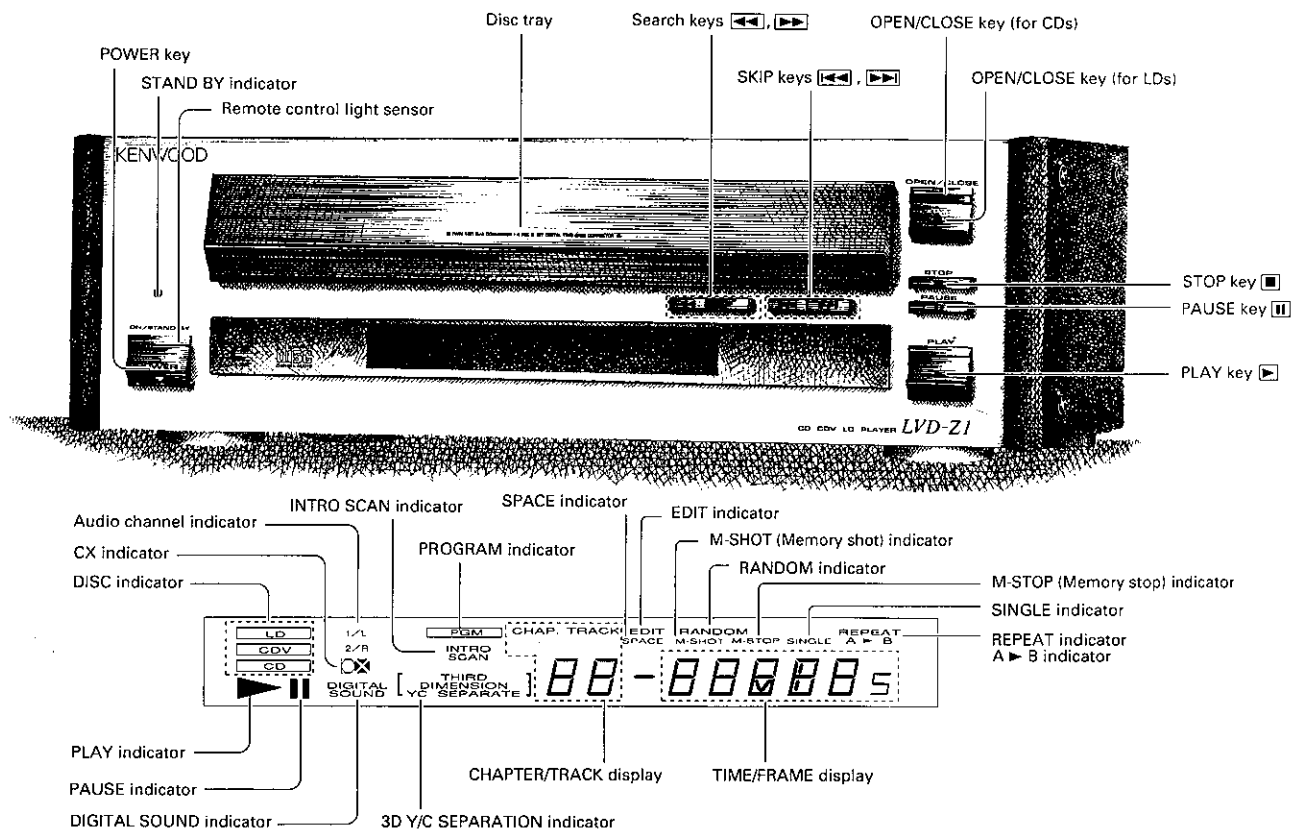
• Remote control unit 1
(A70-0914-05)
• Battery cover (A09-0144-08)



CONTROL

Stand by mode of POWER switch

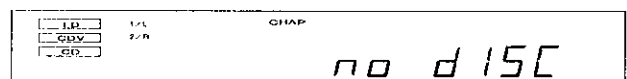
When the power cord of this system is plugged into an AC outlet, the STAND BY indicator lights up regardless of the ON/OFF setting of the POWER switch. This indicates that a small amount of current is being supplied to the unit to back up the memory contents. This mode is referred to as the Stand By mode. While the STAND BY indicator is lit, the power of the system can be switched ON/OFF from the remote control unit.



• Precautions when shipping or moving

When shipping or moving the LVD-Z1, please take the following precautionary procedure:

1. Make sure that no discs are inside the machine, then press the **POWER** key to turn on the power.
2. Confirm the display shows the following message.
3. Press the **POWER** key to turn off the power.



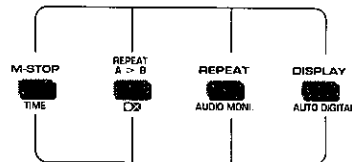
REMOTE CONTROL OPERATION



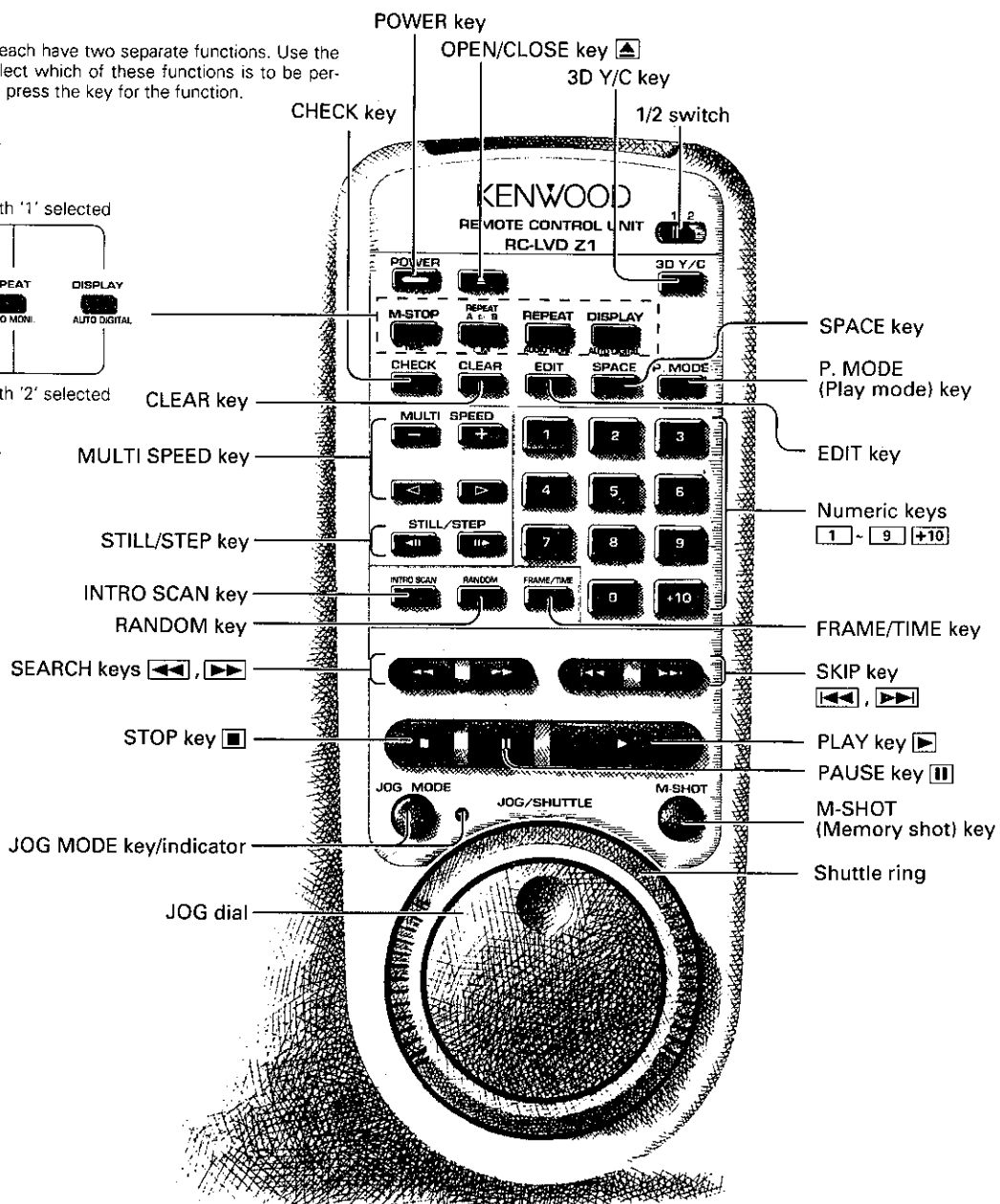
These four keys each have two separate functions. Use the 1/2 switch to select which of these functions is to be performed, and then press the key for the function.



Functions available with '1' selected



Functions available with '2' selected

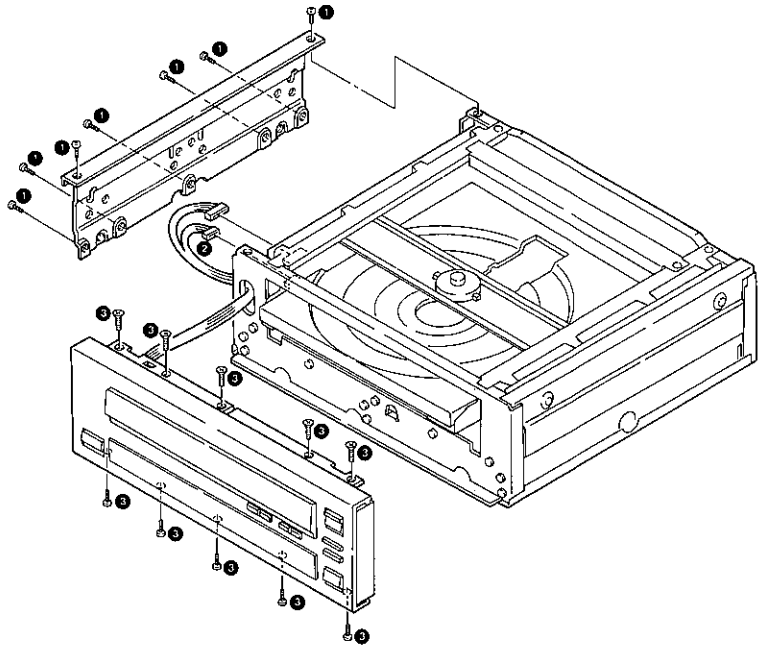


Model name: RC-LVDZ1 (infrared signaling)

DISASSEMBLY FOR REPAIR

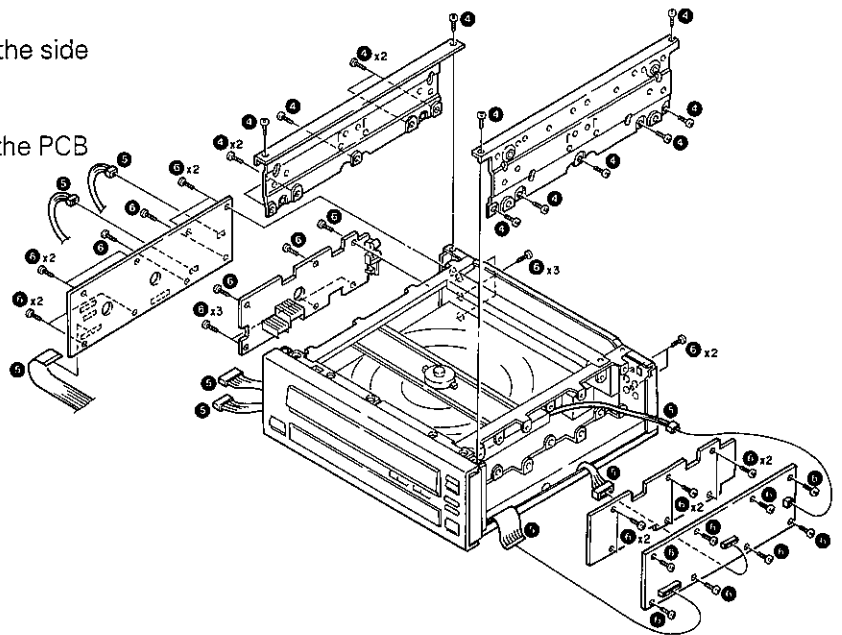
1. Removing the Front Panel

1. Remove the 7 screws (1), then remove the side panel.
2. Disconnect the 2 connectors (2).
3. Remove the 10 screws (3), then remove the front panel.



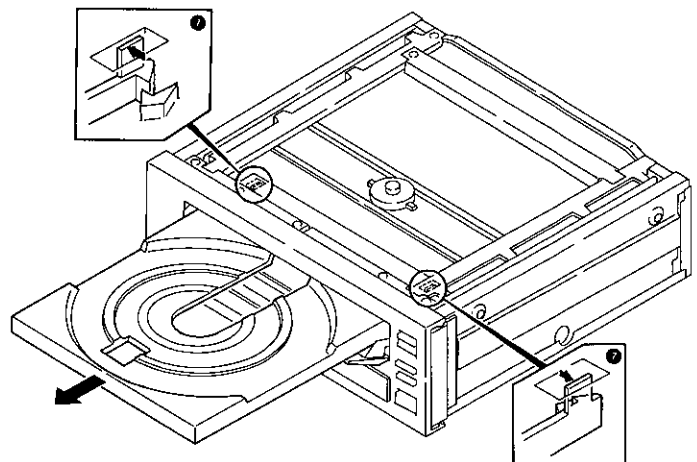
2. Removing the PCB Unit

1. Remove the 14 screws (4), then remove the side panel.
2. Disconnect the 8 connectors (5).
3. Remove the 33 screws (6), then remove the PCB unit.



3. Removing the Tray

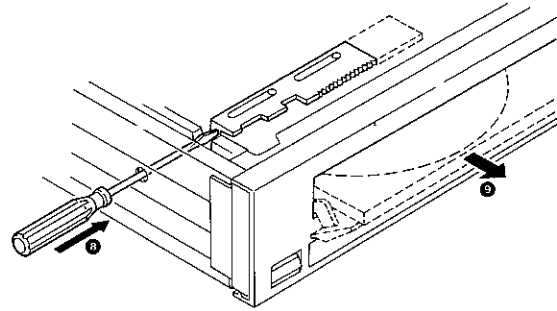
Removing the 2 hook of tray (7), then remove the tray.



DISASSEMBLY FOR REPAIR

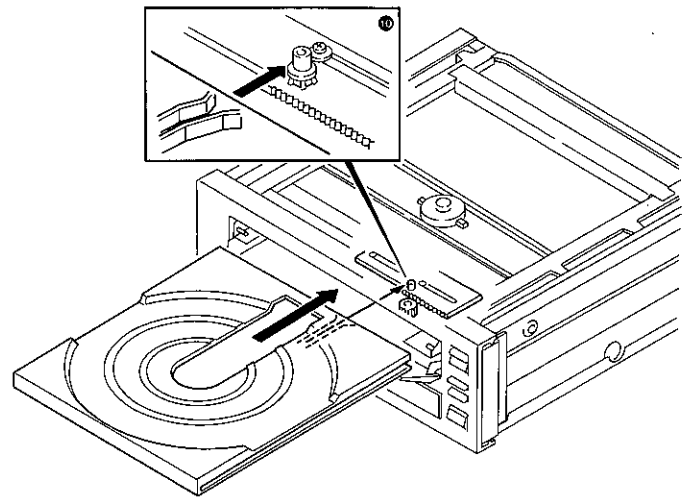
4. How to Pull Tray Out by Hands

1. Insert the screw driver into left side slit of mechanism ass'y (8).
2. Pull out the tray front-wards by hand (9).



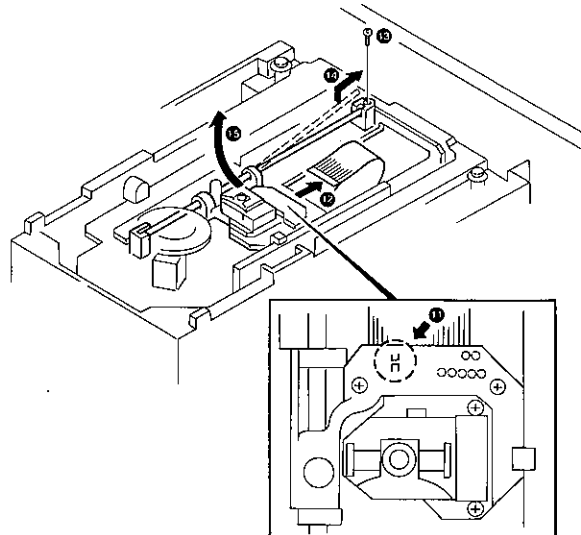
5. How to Mount Tray

Meet the slider boss with the groove of the tray (10).



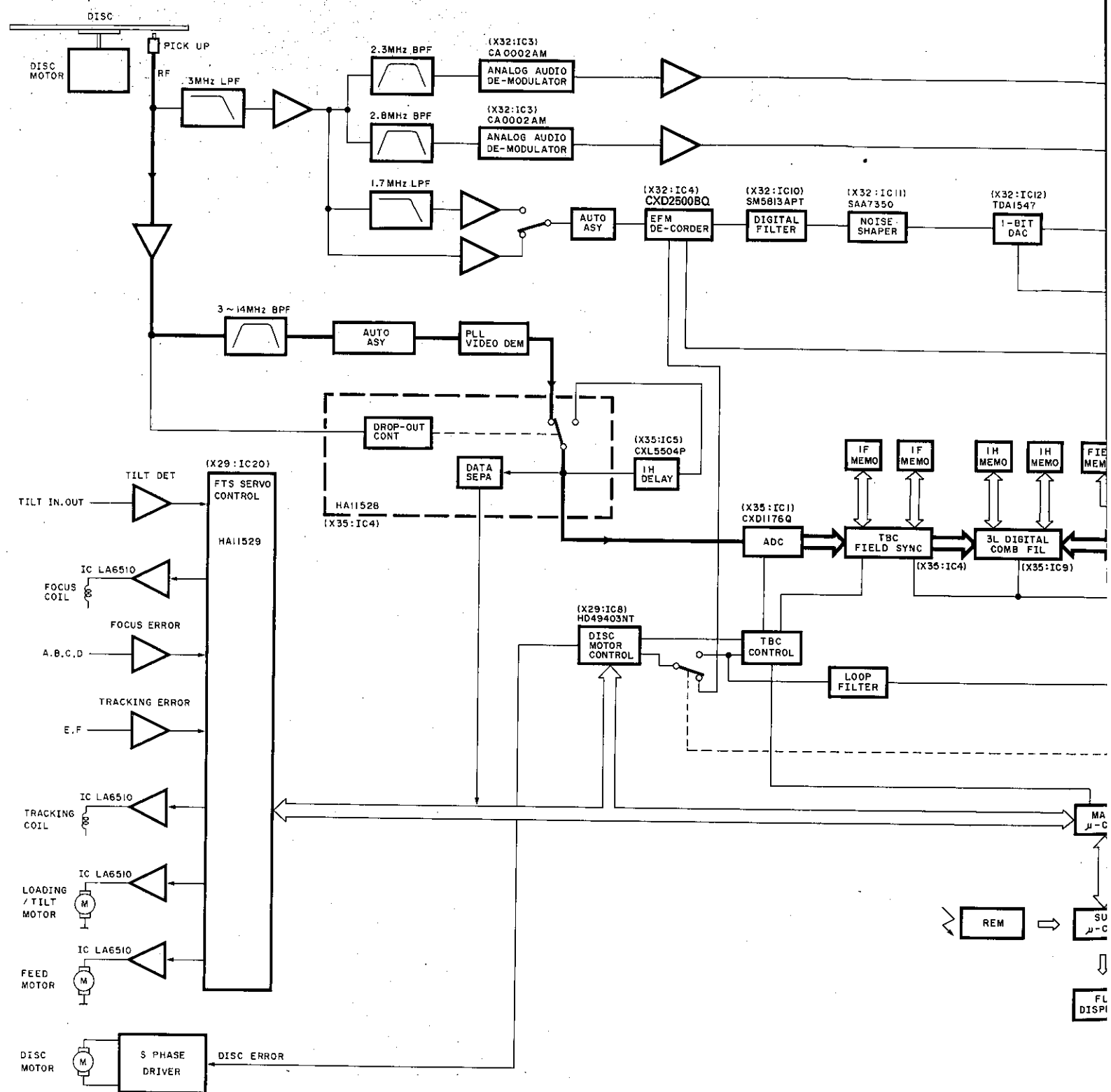
6. How to Disassemble Pickup

1. Short the short land (11).
2. Disconnect the 1 connector (12).
3. Remove the 1 screw (13).
4. Remove the lod of pickup (14).
5. Remove the pickup (15).



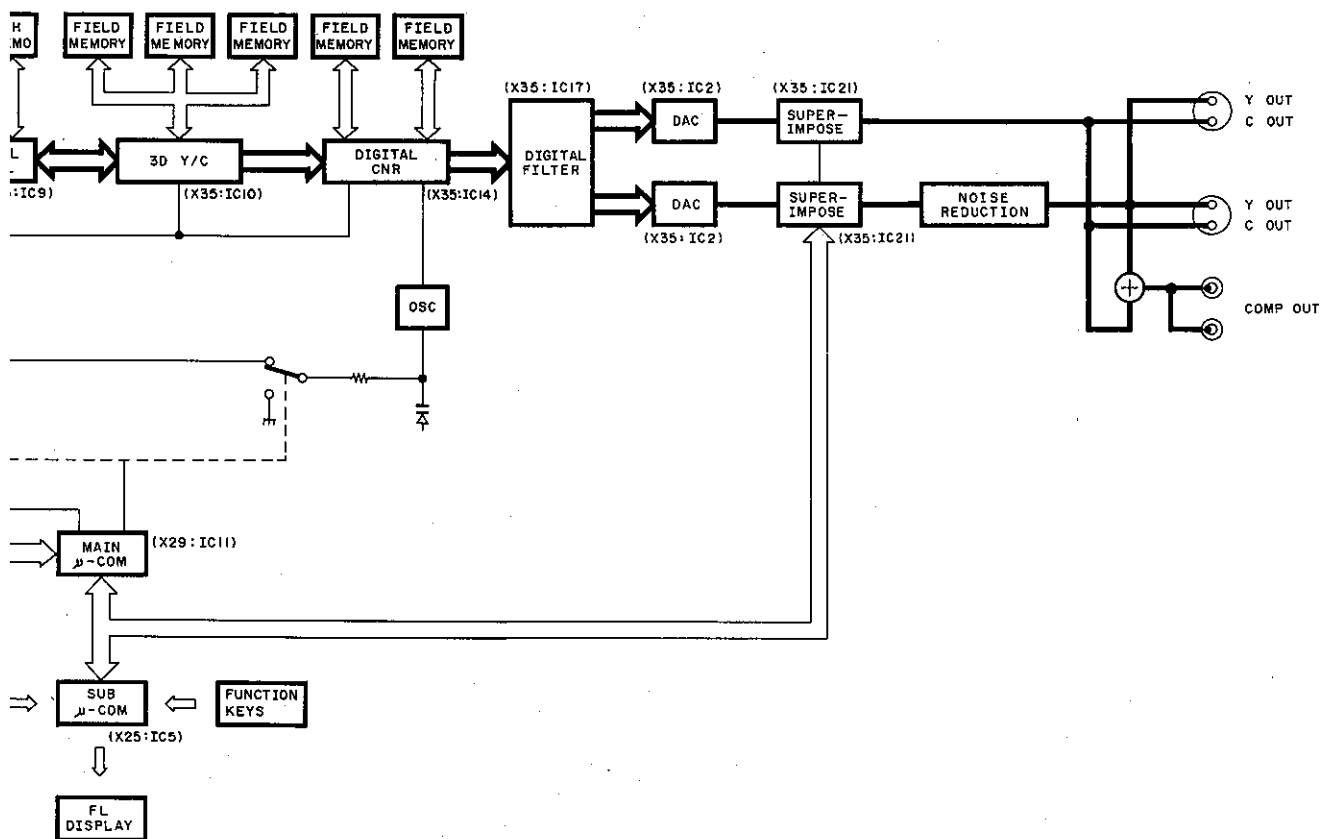
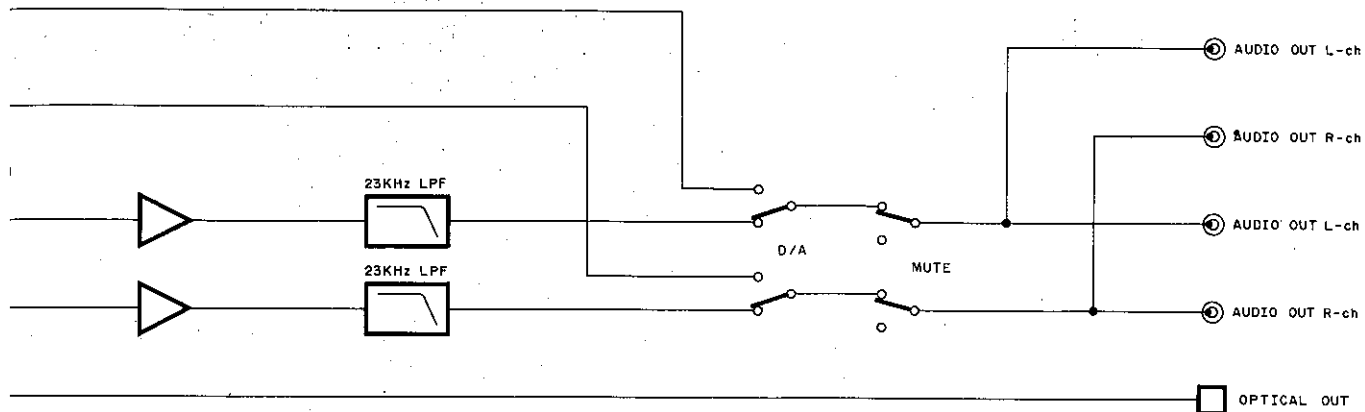
LVD-Z1 L

BLOCK DIAG



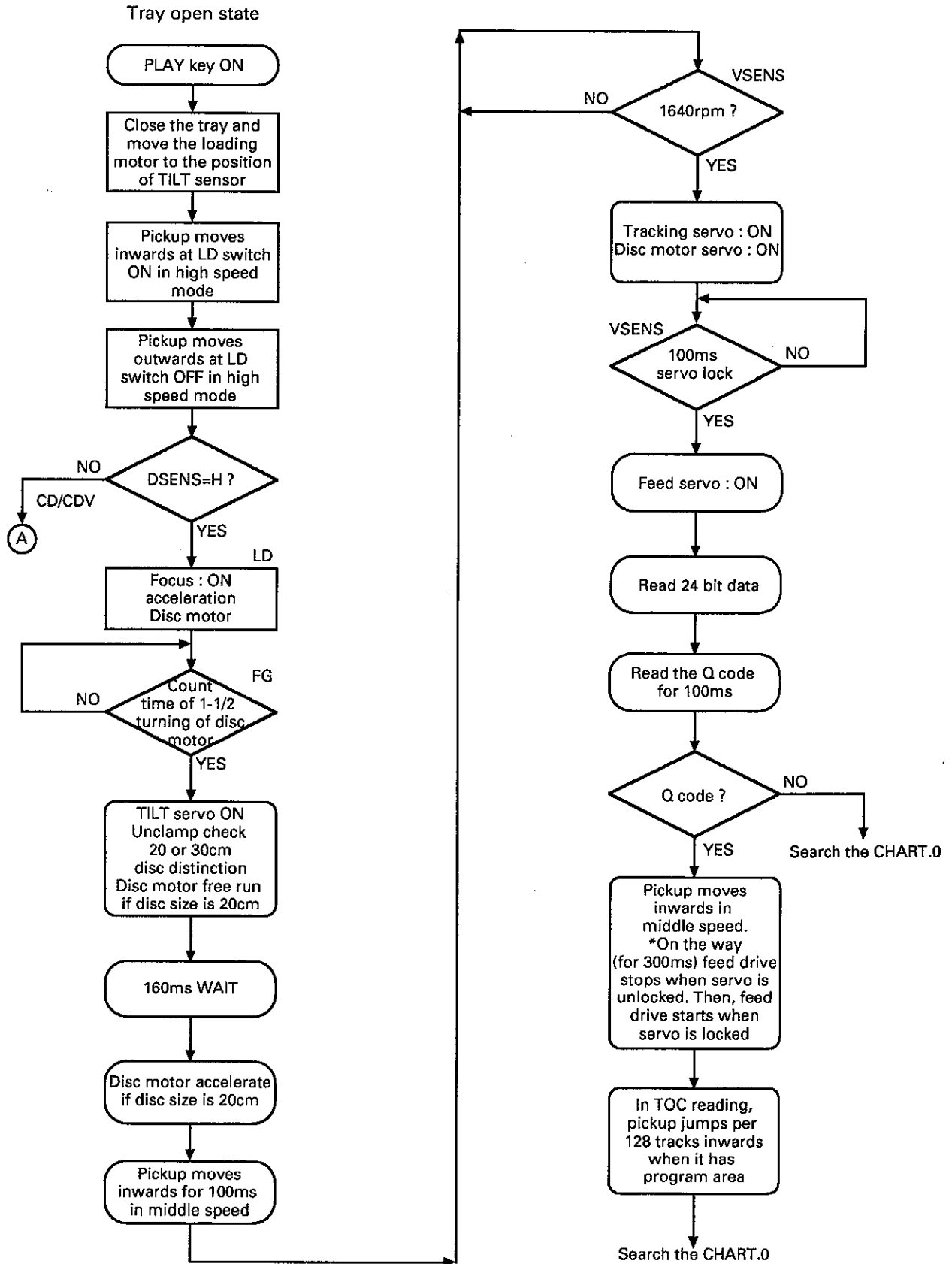
LVD-Z1

IAGRAM



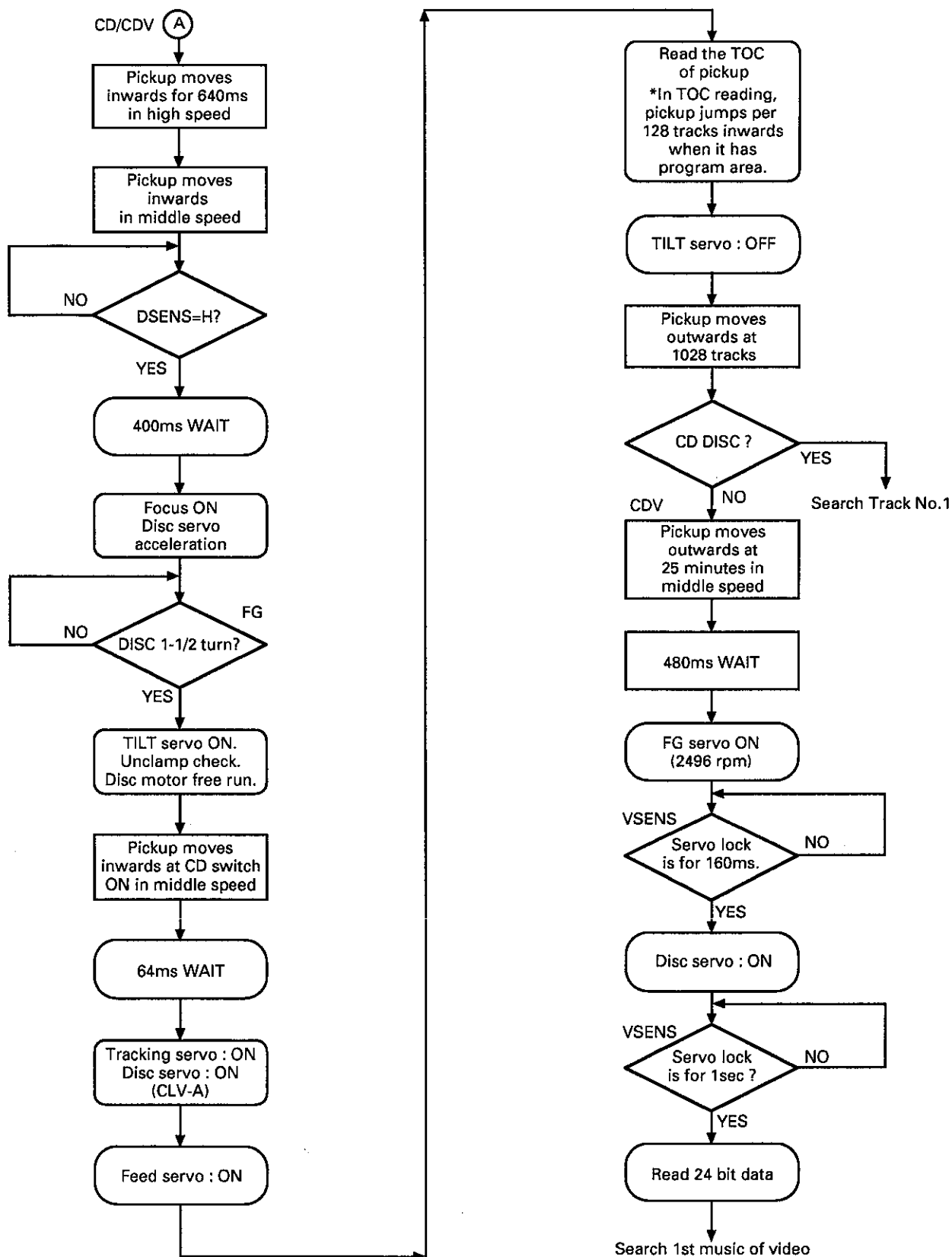
LVD-Z1

FLOW CHART F0



LVD-Z1

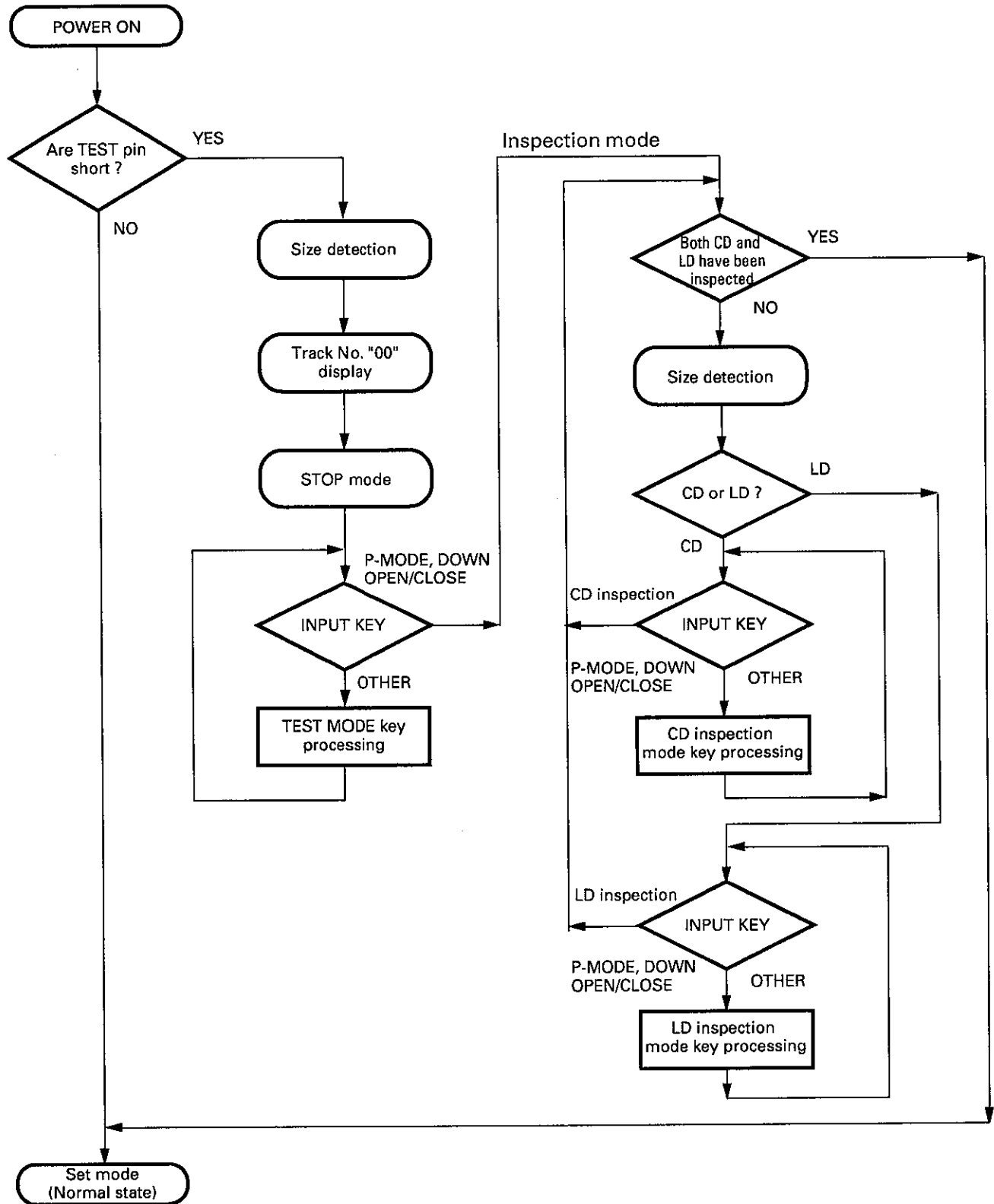
DISC STARTING



TEST MODE

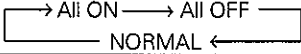
1. Setting the Test Mode

This microprocessor built in this unit can be put to TEST MODE by the just short-circuiting the test pins 3 and 4 on X35-210 (B/2).



TEST MODE

2. Keys and Functions Valid in Test Mode

KEY Name	Description	Track No.
PLAY	Focus servo ON Tracking servo ON Feed servo ON	 Lights
PAUSE	Focus servo ON Tracking servo OFF Feed servo OFF	 Lights
STOP	Enters the STOP mode with the disc clamp.	
SKIP UP	FL 	Video mute is OFF when FL is OFF.
SKIP DOWN or P-MODE	Changes the mode (identification) and not open or close the tray. CD : TNo.=7 ~ play back LD : CHAPTER=27 ~ play back	
Manual FWD 	Feed the pickup outwards	
Manual RVS 	Feed the pickup inwards	
OPEN / CLOSE	OPEN or CLOSE the tray. Change to inspection mode,	
SPACE or RANDOM CD OPEN / CLOSE	Change TILT to ON / OFF (ON : SPACE)	
+10 key or EDIT	Open the tray without changing the mode.	

Inspection mode

OPEN / CLOSE	OPEN or CLOSE the tray. After CD and LD inspection mode, change normal mode if press Open key.	
1 KEY	Still forward	
2 KEY	Still reverse	
3 KEY	Multi-speed forward	
4 KEY	Multi-speed reverse	
5KEY or FRAME / TIME	In the playback mode, turn to still image (Frame No.10900).	

- In the test mode, CHAP. and TNo. go ON.
- In inspection mode, CHAP. and TNo. go OFF.
- In inspection mode, mute output of serial data as follows.
MUTE ON BUSY, DATA : High
MUTE OFF BUSY, DATA : Low
- In inspection mode, the keys except the above table works normally.

CIRCUIT DESCRIPTION

1. Description of Components

1-1. ELECTRIC UNIT (X25-5080-11)

Ref No.	Semi. name	Use and Function	Operation
IC1	μPC78L05J	3-terminal regulator	+5V power supply control for sub μ-com.
IC2	TA78DL05S	3-terminal regulator	+5V power supply control for main μ-com.
IC3	μPC2405HF	3-terminal regulator	+5V power supply control for video (digital).
IC4	PST529C	Reset IC	Generate the reset signal of sub μ-com.
IC5	μPD75216ACW-W44	Sub μ-com	Communicates with main μ-com and receives various keys and remote control signals, drives FL.
Q1	2SA992 (F, E)	Driver	-30V power supply for sub μ-com.
Q2, Q3	DTC124ES, DTA124ES	Switch driver	Turns ON/OFF Q4 and Q5 with power signals.
Q4, Q5	2SD1302 (S, T)	Switch driver	Switch for FL heater. Turned OFF when power is turned OFF.
Q6	2SC3246	Relay driver	Turns ON/OFF relay with power signal.
Q11, Q12	2SC3311A (Q, R)	FL grid current driver	Driver to supply current to grid of FL.
Q13	DTC124ES	Change of LED brightness	Changes brightness of D25 with power signals.
D1	RD30ES (B2)	30V zener diode	Reference of -30V power supply for sub μ-com.
D2	RD5.1ES (B2)	5.1V zener diode	Reference of -24V for sub μ-com.
D3	D3SBA20F03	Rectification diode	Rectification of ±16V power supply for disc motor drive.
D4	D3SBA20F03	Rectification diode	Rectification of +5V power supply for video (Digital).
D5 ~ D8	S5688B	Rectification diode	Rectification of -30V power supply for sub μ-com.
D9 ~ D12	S5688B	Rectification diode	Rectification of +5V power supply for sub μ-com.
D13 ~ D16	S5688B	Rectification diode	Rectification of +5V power supply for main μ-com.
D17	1SS133	For protection from inverse voltage	Prevention of inverse voltage in relay control signal.
D18, D19	1SS133	Countermeasure against line noise	Connected to chassis when GND of disc motor reaches ±0.6V.
D21	RD8.2ES (B2)	8.2V zener diode	Generate the constant VPRE voltage.
D22 ~ D24	1SS133	For protection from inverse current	Prevention of inverse current in control signal of sub μ-com.
D25	B30-1290-05	LED	POWER ON / STAND BY indicator.
D26	1SS133	For prevention of malfunction	Prevention of malfunction at change of V LOCK MODE.

1-2. ELECTRIC UNIT (X25-5120-10)

Ref No.	Semi. name	Use and Function	Operation
IC1 (2/2)	BA10393	FG comparator	Shape wave form of FG signal.
IC2 (1/4)	NJM2058D	TILT comparator	Generates TILT signal by comparing TILT PD IN and OUT.
IC2 (2/4)	NJM2058D	DSSENS comparator	Generates D SENS signal from TILT PD OUT signal.
IC2 (3/4)	NJM2058D	TILT PD OUT amplifier	Amplification of TILT PD OUT signal.
IC2 (4/4)	NJM2058D	TILT PD IN amplifier	Amplification of TILT PD IN signal.
IC3 (1/4)	NJM2058D	FE amplifier	Calculates and amplifies (B+D) - (A+C) and generates FE signal.
IC3 (2/4)	NJM2058D	4D amplifier	Calculates and amplifies A+B+C+D and generates 4D signal.
IC3 (3/4)	NJM2058D	TE amplifier	Calculates and amplifies F-E and generates TE signal.
IC3 (4/4)	NJM2058D	TCONT comparator	Compares level of TE and generates T count signal.
IC4 (1/3, X)	XRU4053B	Change-over of FE balance	Changes CD and LD to each other for FE balance adjustment according to A/V signals.
IC4 (3/3, Z)	XRU4053B	Change-over of APC LD	Turn ON/OFF laser diode with LD ON signal.
IC5 (2/2)	NJM4565D	APC	Control light emission of laser diode.

CIRCUIT DESCRIPTION

1-3. CONTROL CIRCUIT UNIT (X29-2380-00)

Ref No.	Semi. name	Use and Function	Operation
IC1	STA303A	Disc motor (3-phase) driver	3-phase switching operation for NPN Darlington transistor array.
IC2	STA302A		3-phase switching operation for PNP Darlington transistor array.
IC3 (1/2)	NJM4560D-N	Disc motor current sensing amplifier	Differential amplification of voltage at both ends of current sensing resistance (R1).
IC3 (2/2)	NJM4560D-N		Compares output voltage of IC3 (1/2) to see if it is over limit value or not. Uses triangular wave (15kHz) as comparison voltage.
IC4	TA8413P	3-phase motor control	Detects position with hole element in disc motor to control motor drivers in order. Also controls direction of rotation with F/R signal of IC8.
IC5	XRU4053B	Video VCXO control sw	Accurate LD reference master clock.
		Change-over switch for disc motor error	Selects control of disc motor with digital sound system or control with video system according to control lines LOCKMUTE and $\overline{AV}$ of μ -com. Also generates control signals to change reference clock of video to VCXO while motor is turning in digital sound system and to fixed oscillation while motor is turning in video system.
IC6 (1/2)	NJM4565D	Disc motor phase compensation AMP	Special phase compensation amplifier used when motor is controlled by video system.
IC6 (2/2)	NJM4565D	Phase compensation amplifier for VIDEO VCXO	Used when motor is controlled by digital sound system.
IC7	TC5081AP	Phase comparator	Phase comparator for control of disc motor used motor is controlled by video system. Compares phases of Ref. H sync and Playback H sync.
IC8	HD49403NT	Disc servo control	Phase compensation amplifier of disc servo system · PWM conversion Accelerator and brake control · FC servo · Frequency division of clock for FTS.
IC9 (1/2)	NJM4565D	Buffer amplifier	Buffer amplifier of disc servo system.
IC9 (2/2)	NJM4565D	Buffer amplifier	Lowers impedance of 2.5V reference voltage for disc servo.
IC10	PD0011A	24-bit data decoder	Reads 24-bit data.
IC11	M37451M8-134SP	Main μ -com	Controls main functions of mechanical control etc.
IC12	TA7805S	3-terminal regulator	Stabilized power supply for control of +5V disc motor.
IC13 (1/2)	NJM4565D	+5V stabilized power supply	For FTS control.
IC13 (2/2)	NJM4565D	-5V power supply control	For FTS control.
IC14 (1/2)	TA8410AK	Tracking actuator driver	Voltage amplification for tracking actuator.
IC14 (2/2)	TA8410AK	Feed motor driver	Voltage amplification for feed.
IC15 (1/2)	TA7272P	Loading motor driver	Voltage amplification for loading and tilting.
IC15 (2/2)	TA7272P	Focus actuator driver	Voltage amplification for focus actuator.
IC16 (1/2)	NJM4565D	Buffer amplifier	Buffer for pulse output of track jump and scan brake.
IC16 (2/2)	NJM4565D	Subtractor	Subtracts track jump and scan brake pulse from actuator displacement sensing wave form.
IC17 (1/2)	NJM4565D	Buffer amplifier	Buffer for focus error.
IC17 (2/2)	NJM4565D	Buffer amplifier	Buffer for tracking error.
IC18	NJM4565D	Window comparator	Converts output of IC16 (1/2). (Displacement of actuator, Jump pulse/Brake pulse) into pulse wave form.
IC19 (1/2)	NJM4565D	Positive phase amplifier	For defect sensing.
IC19 (2/2)	NJM4565D	Phase compensation amplifier	Amplification and phase compensation of 4D signal.
IC20	HA11529	FTS servo control	For servo control of focus, tracking, slider, and tilting.
Q1	2SC3311A (Q, R)	Voltage conversion	Converts PWM wave form for disc motor control from +5.0V into $\pm 16V$.
Q2, Q3, Q4	2SA1309A (Q, R)	Voltage shift	For control of disc motor driver. Converts +5V into +16V to switch driver on minus side.
Q5	2SA1309A (Q, R)	Voltage conversion	Converts PWM wave form for disc motor control from +5.0V into $\pm 16V$.
Q6	2SC4064	Switch	Switches drive voltage of disc motor with PWM.
Q7	2SC3311A (Q, R)	Voltage conversion	Converts PWM wave form for disc motor control from +5.0V into $\pm 16V$.
Q8	2SA1309A (Q, R)	Muting	Prevents disc motor from running away when power is turned ON/OFF.
Q9	DTC124ES	Muting	Fixes motor return error to 2.5V and stops denying motor return error when CD is played.
Q10	2SC3311A (Q, R)	Inverter	Inverts clock for transfer of system data.

CIRCUIT DESCRIPTION

Ref No.	Semi. name	Use and Function	Operation
Q11	2SC3311A (Q, R)	Clamper	DC clamp of triangular wave for PWM conversion.
Q12	DTC124ES	Muting	Fixes motor error signal for LD to 2.5V when CD is played.
Q13	DTC124ES	Disc servo phase compensation change-over switch	Changes phase compensation constant in CDV mode.
Q14	2SA1309A (Q, R)	Buffer	Buffer for generation of triangular wave for PWM conversion from reference horizontal synchronizing signal.
Q15	2SC3311A (Q, R)	Switch	Switch to lower disc servo gain when CD is played.
Q20	DTC124ES	Inverter	Inverts played horizontal synchronizing signal for IC10.
Q21	DTC124ES	Inverter	Inversion of relay control signal for audio muting.
Q22	DTA124ES	Buffer	Buffer of relay control signal for audio muting.
Q23	DTA124ES	Buffer	Buffer of control signal for FM sound muting.
Q24	2SK163 (L, M)	Switch	Fixes video system disc motor error signal to 2.5V when disc motor is controlled by digital sound system.
Q25	DTA124ES	Inverter and voltage shift	Inversion of photo sensor output for TILT position sensing and voltage conversion into +5V.
Q30	2SD882	Voltage control	Voltage control of +5V stabilized power supply for FTS.
Q31	2SB772	Voltage control	Voltage control of -15V stabilized power supply for actuator driver.
Q32	2SB772	Voltage control	Voltage control of -5V stabilized power supply for FTS.
Q33	2SD882	Voltage control	Voltage control of +15V stabilized power supply for actuator driver.
Q40	DTA124ES	Switch	Turned ON when tray is closed to apply negative voltage to loading motor.
Q41	DTC124ES	Inverter	Inverts output of CD OPEN SW.
Q42	DTC124ES	Switch	Turned ON when tray is opened to apply positive voltage to loading motor.
Q43	DTA124ES	Inverter	Inversion of tray open control signal.
Q44	2SK163 (L, M)	Switch	Turned ON/OFF with reset signals to prevent actuator from operating abnormally and limit focus actuator drive voltage.
Q45	DTC124ES	Switch	Turned OFF when switch to turn ON/OFF Q44 is reset.
Q47	DTA124ES	Switch	Switch to turn ON/OFF Q48, voltage shift.
Q48	2SK163 (L, M)	Switch	Switch for feed servo gain change-over. Turned ON with inside CD SW to lower servo gain.
Q49	DTA124ES	Switch	Switch to turn ON/OFF Q50, turned ON when tray is projected from CD OPEN SW.
Q50	2SK163 (L, M)	Switch	Turned ON when tray is projected from CD OPEN SW to give time constant to loading motor drive voltage. Effective only when tray is closed.
Q51, Q52	2SC3940A (R, S)	Two-way switch	Turned OFF when tray is projected to end to open loading motor.
Q53	DTA124ES	Switch	Switch to turn ON/OFF Q51 and Q52, voltage shift.
Q54	DTC124ES	Inverter	Inverter to operate Q53.
Q59	DTA124ES	Switch	Turned ON when LD is played to keep defect circuit turned OFF.
Q60	2SK163 (L, M)	Sample hold	For defect circuit, turned OFF at position of flaw to hold tracking error.
Q61	DTC124ES	Muting	Keeps stopper mode (search) turned OFF when CD is played.
Q62	DTC124ES	Muting	Keeps focus gain control circuit turned OFF when CD or LD is played (Turned on at this time).
Q64	2SK163 (L, M)	Switch	Turned ON/OFF with reset signal when power is applied to prevent actuator from operating abnormally and limit tracking actuator drive voltage.
D1 ~ D3	RK36	Protection from inverse electromotive force of motor	Protection of drive transistor from inverse electromotive force of motor.
D4	RK36	Regeneration of inverse electromotive force	Flywheel diode to send back power generated by motor and inverse electromotive force of L1 to power supply when Q6 is turned OFF.
D5	1SS133	Switch	Turned ON when current of disc motor reaches 2A to turn OFF Q6 to protect devices from over-current.
D6	RD5.6ES (B2)	Voltage shift	Shifts +16V source voltage when power supply is turned OFF.

CIRCUIT DESCRIPTION

Ref No.	Semi. name	Use and Function	Operation
D7, D8	1SS133	Clamp	Clamps motor return error voltage to $-0.6V$ when it drops below $-0.6V$, and to $5.6V$ when it exceeds $+5.6V$.
D9	1SS133	Switch	Turned ON while tray is opening to prevent switch of Q50 from working.
D10	1SS133	Switch	Turned ON when power supply is turned OFF to turn ON Q8 to mute motor control.
D11	1SS133	Switch	Turned ON when power supply is turned ON to turn ON Q8 to mute motor control.
D12	1SS133	Switch	Turned ON when Vsync comes near before TBC and Vsync after TBC to turn OFF disc servo.
D13	1SS133	Voltage shift	For clamp voltage adjustment of triangular wave for PWM.
D14	1SS133	Rectification	When triangular wave for PWM is generated from reference horizontal synchronizing signal, this element is turned ON, positive side in CD mode to change inclination of triangular wave.
D15, D16	1SS133	For protection from static electricity and line noise	Either is turned ON to release noise when potential difference between GND and chassis of μ -com exceeds $0.6V$.
D17	RD5.1ES (B2)	Generation of reference voltage	For $-5V$ stabilized power supply of disc motor system.
D18	RD15ES (B2)	Generation of reference voltage	For $-15V$ stabilized power supply for actuator drive.
D19	RD15ES (B2)	Generation of reference voltage	For $+15V$ stabilized power supply for actuator drive.
D20	RD5.1ES (B2)	Generation of reference voltage	Generation of reference voltage of $\pm 5V$ tracking stabilized power supply for FTS.
D21	RD5.6ES (B2)	Voltage shift	Control transistor and base voltage shift of $-5V$ stabilized power supply for FTS.
D22	RD5.6ES (B2)	Voltage shift	Control transistor and base voltage shift of $+5V$ stabilized power supply for FTS.
D23 ~ D26	S5688B	Rectification	For $\pm 5V$ power supply for FTS.
D31	1SS133	Switch	Turned on when tray is closed from a point exceeding CD OPEN SW to give time constant to motor drive voltage.
D32, D33	1SS133	OR circuit	Logic circuit to detect time when tray is fully pulled out.
D35	1SS133	Switch	Turned ON when pickup is out of CD SW to turn off Q48.
D36	1SS133	Switch	Turned ON when tray is opened exceeding CD OPEN SW and it is not being closed to turn OFF Q50.
D37	1SS133	Rectification	Rectification of 4D signal.

1-4. Signal processor unit (X32-2350-00)

Ref No.	Semi. name	Use and Function	Operation
IC1	TC74HC00AP	Asymmetry, change and shaping of wave form of RF signals of LD to CD	Shapes and asymmetries digital sound wave form. Changes RF signals of LD and CD (1/5, 2/5, 3/5) according to command ($\overline{A\overline{V}}$) of μ -com. Transfers signals (4/5) only when focus is locked by command of μ -com ($\overline{FOK}$).
IC2	NJM4565D	DC detecting amplifier	Controls DC elements. Takes difference between input and output of IC1 (4/5). (Works as difference amplifier)
IC3	CA0002AM	FM audio demodulation	• Limiting amplifier, • Detector (Phase delay type), • Mute • Drop-out detection and correction, • CX-NR decoding, • Change-over of L/R
IC4	CXD2500BQ	Digital signal processing	• Replay of bit clock, • Demodulation of EFM data • Protection of EFM frame and sync signals, • Demodulation of sub code • Error correction, • Control of disc and servo
IC5 (1/2)	NJM4565D	Buffer	For servo control signal of CD disc motor.
IC5 (2/2)	NJM4565D	Phase compensation and amplification	Phase compensation and amplification of servo control signal of LD disc motor.
IC6	NJM4565D	FM audio amplifier (L, R)	Amplifies output of IC3 (Analog sound).
IC7, IC9	NJM4565L	Error amplifier of stabilized power supply	1/2 is for $+5V$, and 2/2 for $-5V$.
IC8	NJM4565L		1/2 is for $+8V$, and 2/2 for $-8V$.
IC10	SM5813APT	Digital filter	8-time over sampling.
IC11	SAA7350	Bit-stream D/A converter	Converts multi-bit input data from digital filter into PDM signal with tertiary noise shaper.
IC12	TDA1547	Switched capacitor D/A converter	Converts PDM signal into analog signal.
IC13 (1/2)	NJM5532D	Lch difference amplifier	Filtrates and replay positive and negative phase outputs of IC12 through differential circuit.
IC13 (2/2)	NJM5532D	Lch buffer	Output buffer.

CIRCUIT DESCRIPTION

Ref No.	Semi. name	Use and Function	Operation
IC14 (1/2)	NJM5532D	Rch difference amplifier	Filtrates and replay positive and negative phase outputs of IC12 through differential circuit.
IC14 (2/2)	NJM5532D	Rch buffer	Output buffer.
IC15	NJM5532D	Lch LPF	Filtrates replayed audio signals, tertiary LPF.
IC16	NJM5532D	Rch LPF	Filtrates replayed audio signals, tertiary LPF.
Q1	2SC3311A (Q, R)	Buffer	Buffer before RF amplifier.
Q2	2SC1923 (R, O)	For RP signal amplification	Amplifies LD-RF sound signal passed through filter.
Q3	2SC3311A (Q, R)	Buffer	Lowers output impedance of RF amplifier.
Q4	2SC3311A (Q, R)	For muting LD-RF signal	Cuts LD-RF in CD mode.
Q5 ~Q7	2SC3311A (Q, R)	Phase compensation and amplification of LD-RF signal	Phase compensation and amplification of LD-RF signal.
Q8 ~Q10	2SA1309A (Q, R) 2SC3311A (Q, R)	Phase compensation and amplification of CD-RF signal	Phase compensation and amplification of CD-RF signal.
Q13	DTA124ES	For muting LD-RF signal	Cuts LD-RF in CD mode.
Q14	DTC124ES	For change of RF signals	Inverter for change-over between LD-RF and CD-RF.
Q15	DTC124ES	For muting RF signal	Cuts RF signal when not focused.
Q16	DTA124ES	CLOCK switch	Change-over SQCK input of signal processing IC according to command of μ -com (CLKSW).
Q17	DTA124ES	Inverter for EMPH	Inverts EMPH signal (61 pin of IC4).
Q20	2SA1535A	Control transistor	Controls stabilization of voltage of -5V power supply.
Q21	2SC3944A	Control transistor	Controls stabilization of voltage of +5V power supply.
Q22	2SA1535A	Control transistor	Controls stabilization of voltage of -8V power supply.
Q23	2SC3944A	Control transistor	Controls stabilization of voltage of +8V power supply.
Q24	2SA954 (L, K)	Control transistor	Controls stabilization of voltage of -5V power supply.
Q25	2SC2003 (L, K)	Control transistor	Controls stabilization of voltage of +5V power supply.
Q26, Q31	2SK709 (BL, V)	FET for oscillation	Q26 is for VCXO, and Q31 for fixed oscillation.
Q28, Q29	2SK709 (BL, V)	Buffer for oscillation	Q28 is for VCXO, and Q29 for fixed oscillation.
Q32	2SA1309A (Q, R)	Switch for changing oscillation	For turning ON/OFF VCXO.
Q33	2SA1309A (Q, R)	Switch and inverter for changing oscillation	For turning ON/OFF fixed oscillation.
Q34	DTC124ES		
Q36	2SC3311A (Q, R)	Switch	Change-over switch for relay K1.
Q37	2SK163 (N)	Constant current	Stabilizes current flowing in K1.
Q38	2SC3311A (Q, R)	Switch and inverter	Change-over switch and inverter for relay K2.
Q39	2SK163 (N)	Constant current	Stabilizes current flowing in K2.
Q40	2SC3311A (Q, R)	Switch	Change-over switch and inverter for relay K3.
Q41	2SK163 (N)	Constant current	Stabilizes current flowing in K3.
Q42, Q43	DTC124ES, DTA124ES	Switch and inverter	Change-over switch and inverter for relay K2.
Q44, Q45	DTC124ES, DTA124ES	Switch and inverter	Switch to cut input RF signal of IC for FM demodulation and VCO error signal in digital mode.
Q46	2SA1309A (Q, R)	Switch and inverter	Cuts power for IC3 in digital mode to turn OFF analog circuit.
Q47	DTA124ES		Q46 is for +5V, and Q48 is for -5V to invert D/A signal of Q47.
Q48	2SC3311A (Q, R)		All of Q46, Q47, and Q48 are turned OFF in digital mode.
D1 ~ D8	ERA081-004	Rectification diode	D1 ~ D4 are bridge rectification of AC voltage for $\pm 8V$ power supply. D5 ~ D8 are bridge rectification of AC voltage for $\pm 5V$ power supply.
D10	RD5.1JS (B2)	Reference voltage	Zener diode to control stabilization of power supply. D10 and D16 are for -5V, and D13 for -8V.
D13, D16	RD8.2JS (B2)		
D11, D12	RD5.1JS (B2)	Voltage shift	Shifts output voltage of error amplifier of $\pm 5V$ power supply.
D14, D15	RD8.2JS (B2)	Voltage shift	Shifts output voltage of error amplifier of $\pm 8V$ power supply.
D17, D18	RD5.1JS (B2)	Voltage shift	Shifts output voltage of error amplifier of $\pm 5V$ power supply.
D22 ~D24	1SS133	For protection of transistor	Prevents overcurrent from flowing in transistor because of inverse electromotive force when K1 ~ K3 are turned OFF.
D27	1SV147	For changing frequency	Variable capacity diode to change frequency of VCXO with error voltage.
D28 ~ D30	1SS133	For isolation of power supply	Separates power supply of μ -com from power supply of IC3.
D31	1SS133	Switch	Isolates VCOE signal from digital replay mode.
D32	1SS133	Switch	Prevent RF signal from being input to FM demodulation IC in digital replay mode.
D33, D34	1SS133	For changing oscillation	Eliminates effects of side turned OFF when in VCXO and fixed oscillation modes.

CIRCUIT DESCRIPTION

1-5. Video circuit unit (X35-2100-00)

Ref No.	Semi. name	Use and Function	Operation
IC1	TC74HCU04AP	HEX inverter	Amplification of RF signal.
IC2 (1/2)	NJM4565D	Difference amplifier	Shaping of RF signal wave form
IC2 (2/2)	NJM4565D	Not use	
IC3	YM3558	Demodulator	Demodulation of video signal.
IC4	HA11528	Drop-out compensation	Drop-out sensing and compensation switch. Separation of synchronous DATA.
IC5	CXL5504P	1H delay	For drop-out compensation. 1H delay of video signal.
IC6	LVA519S	Separation of synchronization	Separation of synchronization for TBC.
IC7	TC74HCU04AP	HEX inverter	VCO
IC8	TC74HCU04AP	HEX inverter	Buffer for LOCK1 and LOCK2 signal. OR operation.
IC10	XRU4053B	Analog switch	Digital TBC. Comparison of burst phase. Sensing of burst signal.
IC11 (1/2)	NJM4565D	Subtraction amplifier	Subtraction amplifier of burst phase comparison output.
IC11 (2/2)	NJM4565D	Buffer amplifier	Compensation of burst error, holding, buffer, and phase
IC12	XRU4053B	Analog switch	H, burst, change-over switch, burst error sampling pulse.
IC13 (1/2)	NJM4565D	Buffer amplifier	Buffer for sensing burst and amplitude.
IC13 (2/2)	NJM4565D	Buffer amplifier	Buffer for holding burst and amplitude.
IC14 (1/2)	NJM4565D	Subtraction amplifier	Subtraction amplifier of H phase comparison output.
IC14 (2/2)	NJM4565D	Buffer amplifier	Buffer amplifier for burst and signal.
IC15 (1/2)	NJM4565D	Addition amplifier	Addition of burst, H, and error signal
IC15 (2/2)	Not use		
IC16	TC74HC123AP	Dual mono-multi vibrator	Generates pulses to detect burst and phase shift.
IC17	TC74HC74AP	F.F	Detects burst and phase shift.
IC21	M50554-270SP	Superimpose	Gray pack. Generation of characters. Y signal superimpose.
IC22	MM1108XS	Separation of synchronization	Separation of synchronization for superimpose.
IC23	XRU4053B	Analog switch	C signal mute and superimpose.
IC24 (1/2)	NJM4565D	Inverting amplifier	Noise canceller. Noise limit voltage output (-).
IC24 (2/2)	NJM4565D	Buffer amplifier	Noise canceller. Noise limit voltage output (+).
IC25	TC74HC123AP	Dual mono-multi vibrator	Inverts H and V signals. Remove V signal noise.
IC26 (1/2)	NJM4565D	Inverting amplifier	Power supply control (-).
IC26 (2/2)	NJM4565D	Inverting amplifier	Power supply control (+).
Q1 ~ Q3	2SC1923 (R, O) 2SC3311A (Q, R)	Difference amplifier	RF signal amplifier
Q4	2SA1309A (Q, R)	Constant voltage power supply	For IC3.
Q5	2SC3311A (Q, R)	Buffer amplifier	Buffer amplifier for LPF.
Q6	2SC3311A (Q, R)	Buffer amplifier	Buffer amplifier of video amplitude adjustment circuit.
Q7	2SC3311A (Q, R)	Buffer amplifier	Buffer amplifier for de-emphasis.
Q8	DTC124ES	Switch	Changes RF amplifier equalizer.
Q9	2SC3311A (Q, R)	Constant voltage power supply	For clamping video signals.
Q10 ~ Q12	2SC1923 (R, O) 2SC3311A (Q, R)	Difference amplifier	Video amplifier.
Q13	2SC3311A (Q, R)	Inverting amplifier	Inverting amplifier for 1H delay signal.
Q14	2SC3311A (Q, R)	Buffer amplifier	Buffer amplifier for LPF.
Q15, Q16	2SC1923 (R, O)	Limiter amplifier	Amplification of 3.58MHz signal.
Q17, Q18	2SC1923 (R, O)	Limiter amplifier	Amplification of RF signal.
Q19	2SA1309A (Q, R)	Buffer amplifier	For 3.58MHz signal.
Q20, Q21	2SC3311A (Q, R)	Buffer amplifier	For 3.58MHz signal.
Q22	2SC3311A (Q, R)	Buffer amplifier	For RF signal.
Q23	2SA1309A (Q, R)	Filter	For video signal.
Q25	2SC3311A (Q, R)	Switch	Change-over of TBC error signal.
Q31	2SC3311A (Q, R)	Buffer amplifier	For Y signal.

CIRCUIT DESCRIPTION

Ref No.	Semi. name	Use and Function	Operation
Q32	2SA1309A (Q, R)	Buffer amplifier	For Y signal.
Q33	2SA1309A (Q, R)	Buffer amplifier	For C signal.
Q34	DTC124ES	Switch	Y signal mute.
Q35	2SC3311A (Q, R)	Buffer amplifier	For Y signal.
Q36	2SC3311A (Q, R)	Buffer amplifier	For LPF.
Q37, Q38	2SC1923 (R, O)	Limiter amplifier	Noise canceller and noise amplifier.
Q39	2SC1923 (R, O)	Addition amplifier	Inversion of noise canceller and addition of noise.
Q40	2SC3311A (Q, R)	Filter	LPF for noise canceller.
Q41	2SC3311A (Q, R)	Buffer	For Y and C addition.
Q43	2SC1923 (R, O)	Positive phase amplifier	For C signal.
Q44	2SC3311A (Q, R)	Filter	LPF for C signal.
Q45	2SC1923 (R, O)	Addition amplifier	For Y and C addition.
Q46	2SA1309A (Q, R)	Buffer amplifier	Composite signal output buffer.
Q47	2SC3311A (Q, R)	Buffer amplifier	Composite signal output buffer.
Q48	2SC3311A (Q, R)	Buffer amplifier	C signal output buffer.
Q49	2SA1309A (Q, R)	Buffer amplifier	Y signal output buffer.
Q50	2SC3311A (Q, R)	Buffer amplifier	Y signal output buffer.
Q51	DTC124ES	Switch	Change of noise cancel level.
Q52	2SD2012	Buffer amplifier	+5V power supply.
Q53	2SB1375	Buffer amplifier	-5V power supply.
Q54	2SK163 (L, M)	Constant current power supply	Bias current supply for Q52.

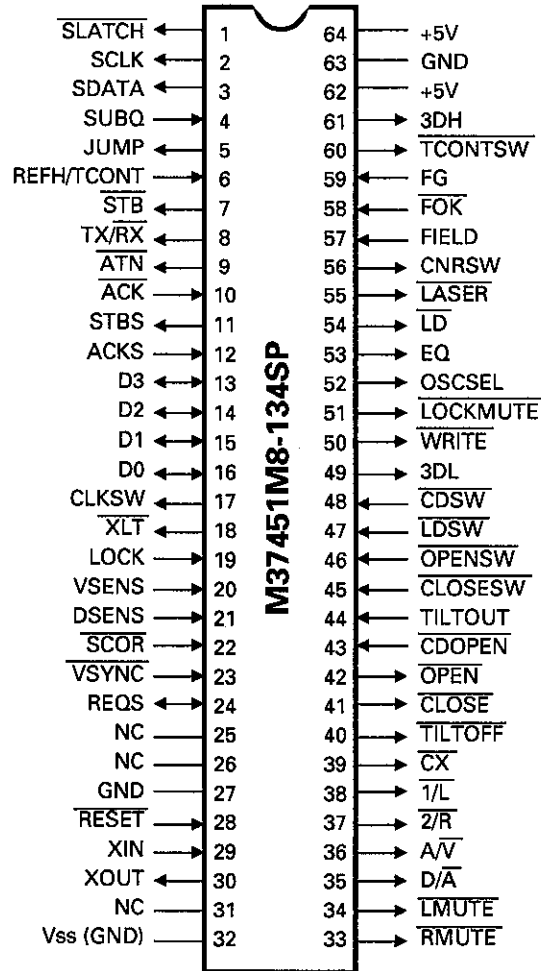
1-6. Video unit : Digital (X35-2110-00)

Ref No.	Semi. name	Use and Function	Operation
IC1	CXD1176Q	A/D converter	A/D conversion of video signal. Sampling CLK is 4fsc.
IC2	CXD1177Q	D/A converter	D/A conversion of video signal. Sampling CLK is 8fsc.
IC3	TC7S04F	Inverter	Inversion of PB 4fsc (4fsc of TBC) signal.
IC4	KAG03	TBC control	TBC control and video field synchronizer.
IC5, IC6	CXK1206M	Field memory	Field memory for field synchronizer.
IC7, IC8	MN4760S	Line memory	1H line memory for 3-line Y/C separation.
IC9	KAG04	3L Y/C separation	Logical com filter for 3 line Y/C separation.
IC10	KAG05	3L Y/C separation	3-dimensional Y/C separation.
IC11 ~ IC13	TMS4C1070B-30N	Frame memory	1-frame memory for 3-dimensional Y/C separation.
IC14	KAM01	CNR	Frame cyclic digital color noise reduction.
IC15, IC16	HM53051FP-45	Frame memory	1-frame memory for CNR.
IC17	KAN01	BPF	Band pass filter for color signal. Over-sampling of brightness signal. Sampling CLK is 8fsc.
IC18	TC74HCU04AF	VCXO	VCXO for reference 8fsc (28.63636 MHz)

CIRCUIT DESCRIPTION

2. Main μ -com : M37451M8-134SP (IC11, X29-2380)

2-1. Pin connection



2-2. Pin function

No.	Pin name	I/O	Function
1	SLATCH	O	Latch output to FTS IC
2	SCLK	O	Clock output to FTS / CD IC
3	SDATA	O	Data output to FTS / CD IC
4	SUBQ	I	Q data input
5	JUMP	O	Pulse output pin for one track jump
6	REFH/TCONT	I	Event count pin for REFH or TCONT
7	STB	O	PD0011A strobe
8	TX/RX	O	Low level : Input from PD0011A (High level : Output to PD0011A)
9	ATN	O	PD0011A attention
10	ACK	I	PD0011A acknowledge
11	STBS	O	STBS output (To sub μ -com)
12	ACKS	I	ACKS input (From sub μ -com)
13 ~ 16	D3 ~ D0	I/O	Data I/O pin
17	CLKSW	O	SCLK changing pin (High level : CD IC, Low level : FTS IC)
18	XLT	O	Latch output pin to CD IC
19	LOCK	I	Frame sync lock detection pin (High level : Lock)
20	VSENS	I	HD49403NT sense pin

CIRCUIT DESCRIPTION

No.	Pin name	I/O	Function			
21	DSENS	I	Disc detection signal input (High level : with disc)			
22	SCOR	I	Q data sync signal interruption pin			
23	VS $\overline{\text{YNC}}$	I	Video sync signal interruption pin			
24	REQS	I/O	REQS I/O pin to sub μ -com, Rising edge interruption			
25, 26	NC	—	No used			
27	GND	—	GND			
28	$\overline{\text{RESET}}$	I	Reset pin.			
29	Xin	I	Clock oscillator input (10MHz)			
30	Xout	O	Clock oscillator output			
31	NC	—	No used			
32	Vss	—	GND			
33	$\overline{\text{RMUTE}}$	O	Muting relay control			
34	$\overline{\text{LMUTE}}$	O	Analog mute pin (Low level : Mute ON)			
35	D/ $\overline{\text{A}}$	O	Digital /Analog change signal output			
36	A/ $\overline{\text{V}}$	O	Audio /Video change signal output			
37	2/ $\overline{\text{R}}$	O	Stereo output : 0	Rch output : 0	Lch output : 1	MUTE ON : 1
38	1/ $\overline{\text{L}}$	O	Stereo output : 0	Rch output : 1	Lch output : 0	MUTE ON : 1
39	$\overline{\text{CX}}$	O	CX mode selection output			
40	$\overline{\text{TILTOFF}}$	O	Tilt servo gain control			
41	$\overline{\text{CLOSE}}$	O	Tray motor control (Low level : Toward close)			
42	$\overline{\text{OPEN}}$	O	Tray motor control (Low level : Toward open)			
43	$\overline{\text{CDOPEN}}$	I	Low level : Half open switch ON			
44	$\overline{\text{TILTOUT}}$	I	Photo interruption input (High level : Light pass)			
45	$\overline{\text{CLOSESW}}$	I	Tray close signal input (Low level : Close switch ON)			
46	$\overline{\text{OPENS}}\overline{\text{W}}$	I	Tray open signal input (Low level : Open switch ON)			
47	$\overline{\text{LDSW}}$	I	LD lead-in signal input (Low level : LD switch ON)			
48	$\overline{\text{CDSW}}$	I	CD lead-in signal input (Low level : CD switch ON)			
49	3DL	O	3D Y/C mode control			
50	$\overline{\text{WRITE}}$	O	Field memory writing control			
51	$\overline{\text{LOCKMUTE}}$	O	Disc motor lock mode control			
52	OSCSEL	O	Disc motor oscillator control (High level : Audio, Low level : Video)			
53	EQ	O	Video equalizer selection (CAV with frame No more than 8000 : L)			
54	$\overline{\text{LD}}$	O	LD/other change pin			
55	$\overline{\text{LASER}}$	O	Laser ON/OFF port (Low level : Laser ON)			
56	$\overline{\text{CNRSW}}$	O	Color noise reduction switch (High level : ON)			
57	FIELD	I	No used			
58	$\overline{\text{FOK}}$	I	Focus OK input			
59	FG	I	FG input pin of disc motor (24 pulses per turn)			
60	$\overline{\text{TCONT}}\overline{\text{SW}}$	O	H : TCONT count, L : Disc unclamp detection			
61	3DH	O	3D Y/C mode control			
62	+5V	—	+5V			
63	GND	—	GND			
64	+5V	—	+5V power supply			

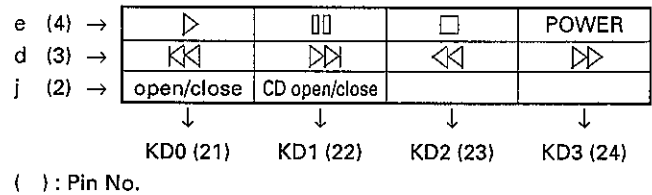
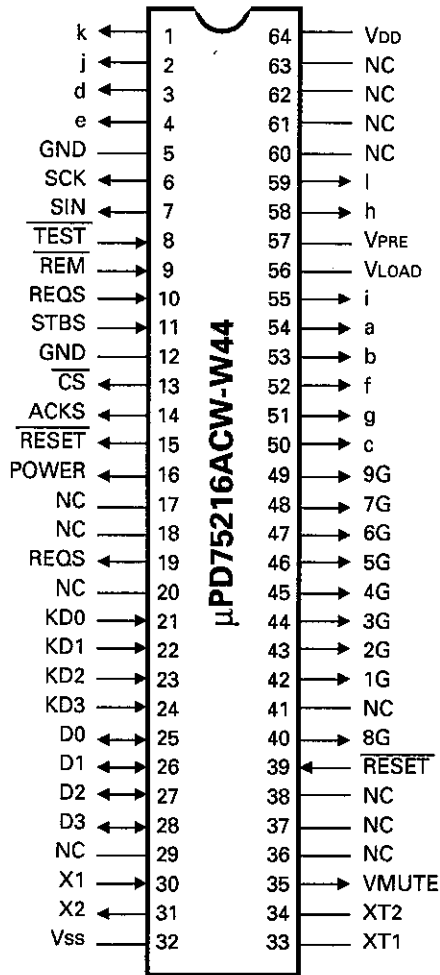
2-3. 3D Y/C mode setting

	3DL (49pin)	3DH (61pin)
3D NORMAL	L	L
3D LOW	H	L
3D HIGH	L	H

CIRCUIT DESCRIPTION

3. Sub μ -com : μ PD75216ACW-W44 (IC5, X25-5080)

3-1. Pin connection



3-2. Pin function

No.	Pin name	I/O	Function
1	k	O	FL segment k
2	j	O	FL segment j / key scan port
3	d	O	FL segment d / key scan port
4	e	O	FL segment e / key scan port
5	GND	-	No used
6	SCK	O	Super impose clock output
7	SIN	O	Super impose data output
8	TEST	I	Test mode setting pin
9	REM	I	Remote control input, interrupt on the falling edge
10	REOS	I	REOS input, interrupt on the rising edge (To main μ -com)

CIRCUIT DESCRIPTION

No.	Pin name	I/O	Function
11	STBS	I	STBS input pin (To main μ -com)
12	GND	-	No used
13	CS	O	Super impose chip select output
14	ACKS	O	ACKS output (To main μ -com)
15	RESET	O	Reset output (To main μ -com)
16	POWER	O	Relay drive output
17	NC	-	No used
18	NC	-	No used
19	REQS	O	REQS output pin (To main μ -com)
20	NC	-	No used
21 ~ 24	KD0 ~ KD3	I	Key input pin
25 ~ 28	D0 ~ D3	I/O	Data I/O pin (To main μ -com)
29	NC	-	No used
30	X1	I	Oscillator input (4.19MHz)
31	X2	O	Oscillator output
32	Vss	-	GND
33	XT1	-	GND
34	XT2	-	OPEN
35	VMUTE	O	VMUTE output (High : MUTE)
36 ~ 38	NC	-	No used
39	RESET	I	Reset input
40	8G	O	FL grid 8G
41	NC	-	No used
42 ~ 48	1G~7G	O	FL grid 1G~7G
49	9G	O	FL grid 9G
50	c	O	FL segment c
51	g	O	FL segment g
52	f	O	FL segment f
53	b	O	FL segment b
54	a	O	FL segment a
55	i	O	FL segment i
56	VLOAD	-	FL erase voltage power supply
57	VPRE	-	FL pre-driver power supply
58	h	O	FL segment h
59	j	O	FL segment j
60 ~ 63	NC	-	No used
64	VDD	-	+5V power supply

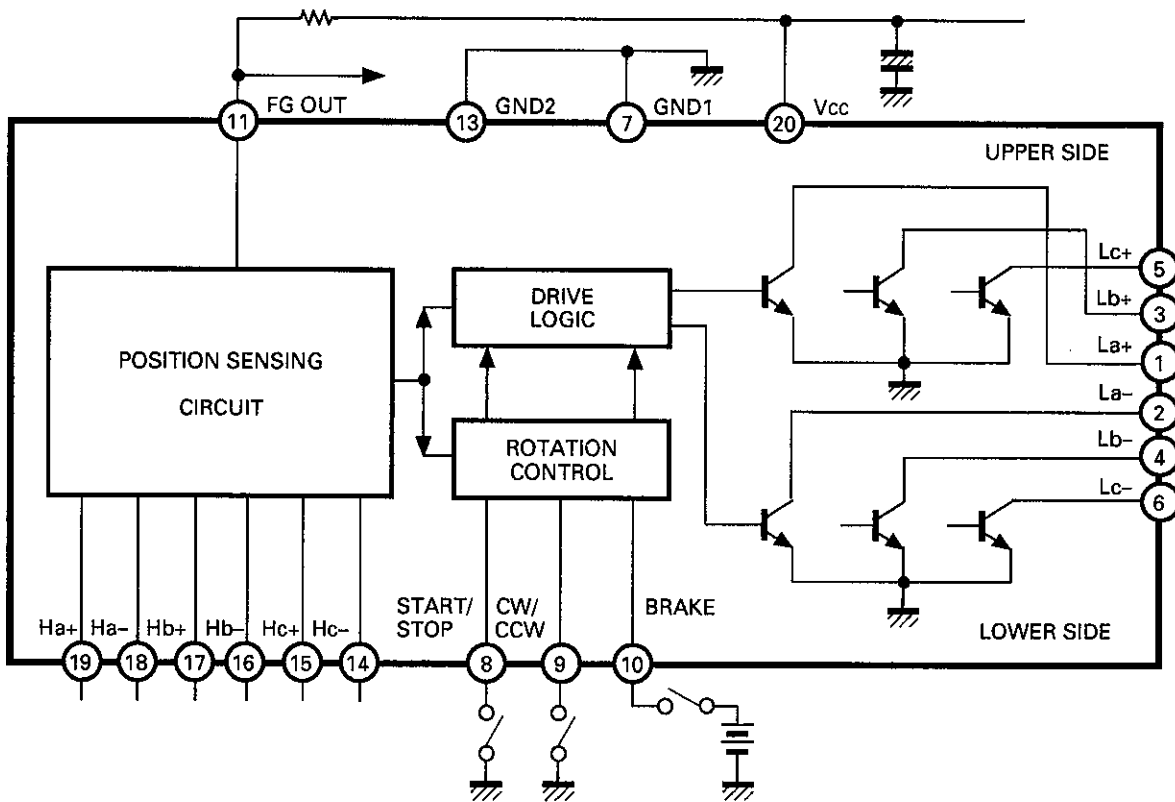
CIRCUIT DESCRIPTION

4. Disc Driver : TA8413P (IC4, X29-2380)

4-1. Features : For motor control (3-phase two-way type)

- FG is not necessary (The rotating speed signal is taken by detecting a position).
- The start/stop function, CW/CCW function, and brake function are installed.
- The position sensing circuit has a high gain and a hysteresis.
- A Rotation signal output is supplied. (A frequency signal three times the position sensing output [Hole element output] can be taken out.)
- Outside transistor type.

4-2. Block diagram



CIRCUIT DESCRIPTION

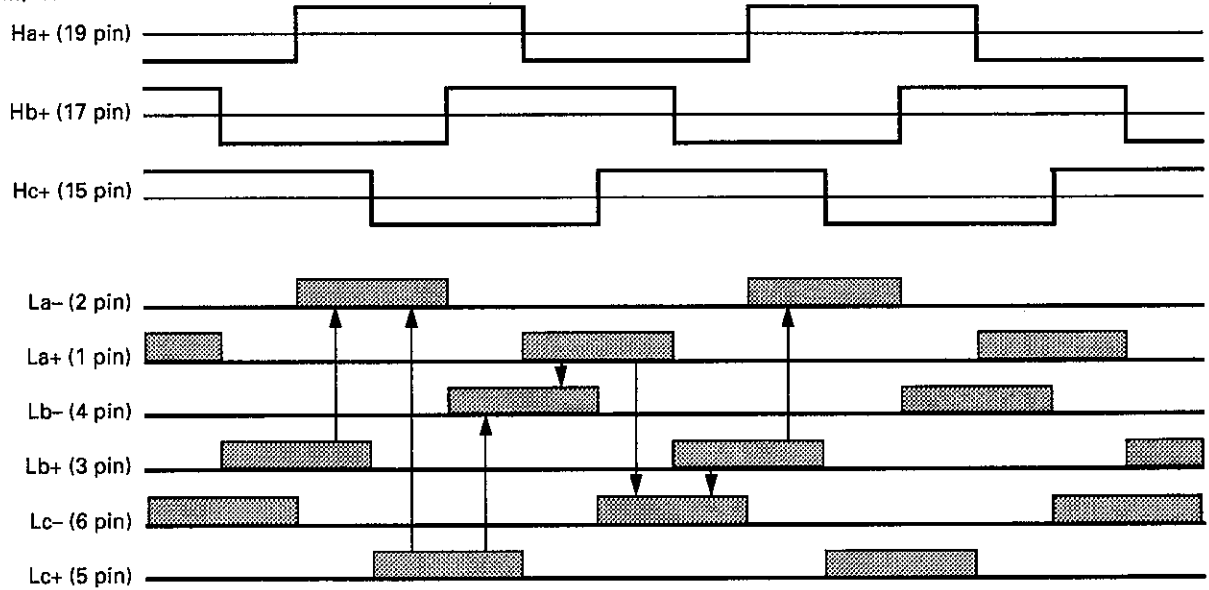
4-3. Timing chart

Forward rotation (Detecting position signal : $H_a \rightarrow H_b \rightarrow H_c$)

START/STOP (8 pin) "H"

CW/CCW (9 pin) "L"

BRAKE (10 pin) "H"

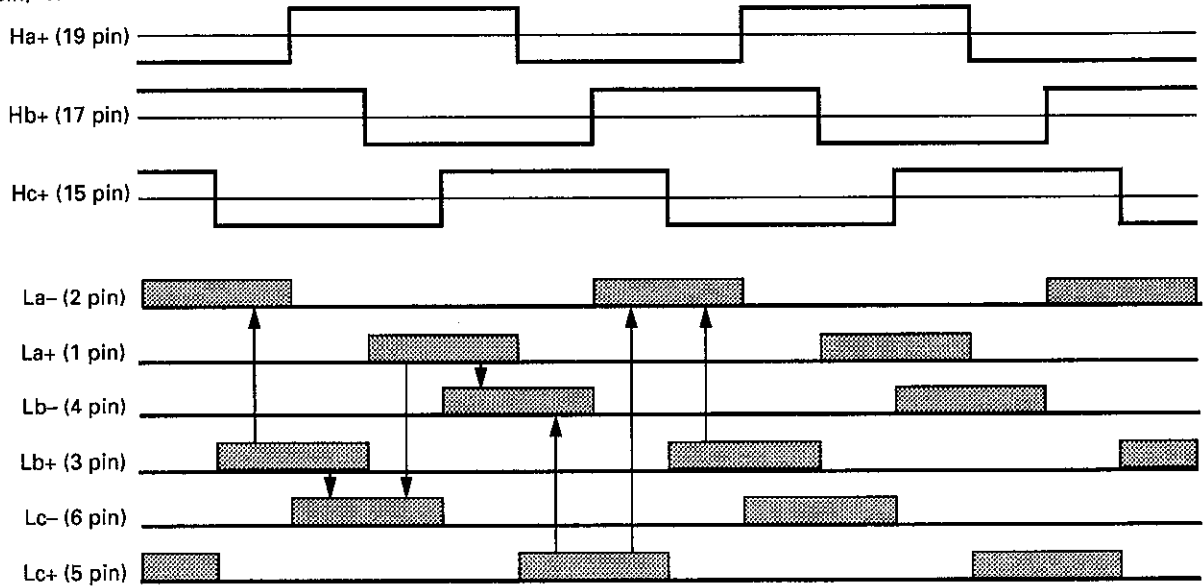


Reverse rotation (Detecting position signal : $H_a \rightarrow H_c \rightarrow H_b$)

START/STOP (8 pin) "H"

CW/CCW (9 pin) "L"

BRAKE (10 pin) "H"



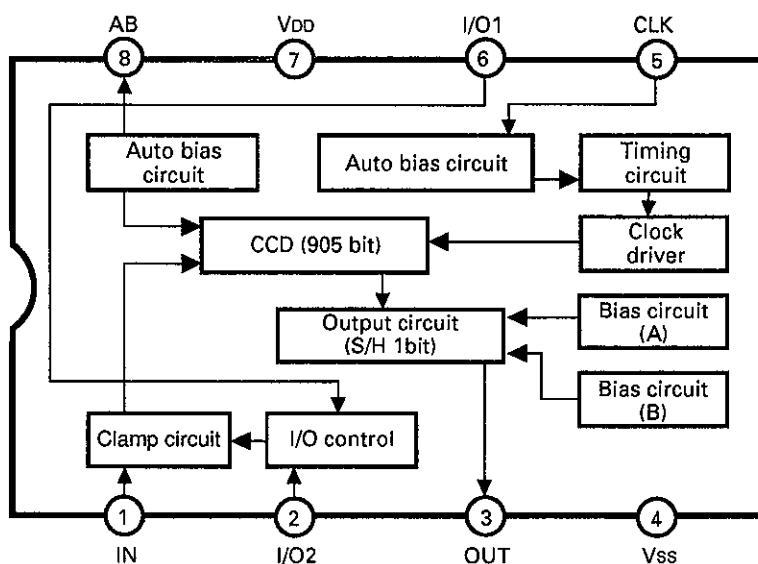
CIRCUIT DESCRIPTION

5. 1H Delay CCD : CXL5504P (IC5, X35-2100)

5-1. Outline

CXL5504P is a CMOS-CCD delay element which gives a delay of 1H to the NTSC signal, including the outside low-pass filter.

5-2. Block diagram



5-3. Pin function

No.	Name	I/O	Function	Impedance
1	IN	I	Signal input	>10k Ω : Non clamp state
2	I/O2	I	I/O control 2	
3	OUT	O	Signal output	40 Ω ~ 500 Ω
4	Vss	-	GND	
5	CLK	I	Clock input	>100k Ω
6	I/O1	I	I/O control 1	
7	VDD	-	Power supply (5V)	
8	AB	O	Auto bias DC output	600 ~ 200k Ω

CIRCUIT DESCRIPTION

6. Video A/D Converter : CXD1176Q (IC1, X35-2110)

6-1. Outline

CXD1176Q is an 8-bit CMOS A/D converter for video which has a synchronous clamp function. Since the 2step-Parallel method is employed, the maximum conversion speed of 20MSPS is attained although less power is consumed.

6-2. Features

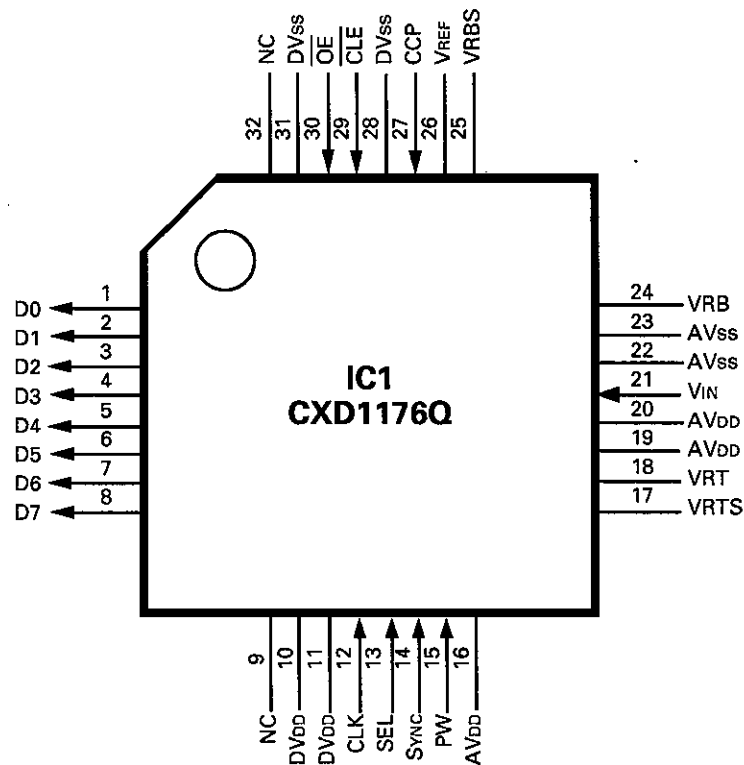
- Resolution of 8bits $\pm 1/2$ LSB (DL).
- The maximum sampling frequency of 20MSPS.
- Low power consumption of 60mW (at 20MSPS Typ) (Excluding the reference current).
- Built-in synchronous clamp function.
- Built-in mono-multi for generation of clamp pulses.
- Built-in synchronous pulse polarity selecting function.
- Clamp pulses can be directly input.
- Built-in clamp ON/OFF function.

- Built-in reference voltage self-bias circuit.
- The compatible input CMOS.
- 3-state TTL compatible output.
- Only one source voltage of 5 V is required.
- Low input capacity of 11pF.
- Reference impedance is 300 Ω (Typ).

6-3. Type of output

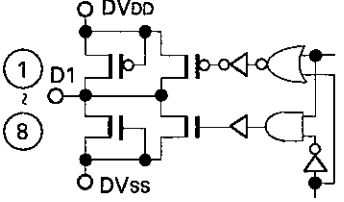
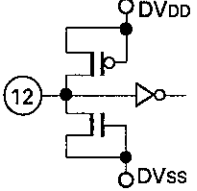
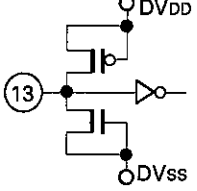
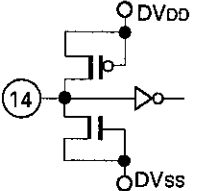
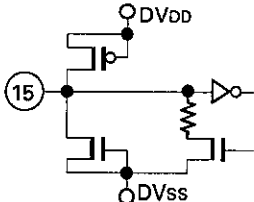
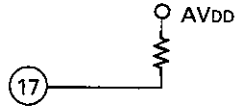
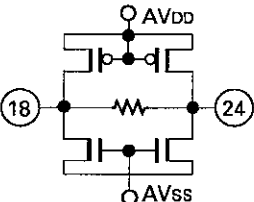
Input signal voltage	Step	Digital output code							
		MSB				LSB			
VRT	0	1	1	1	1	1	1	1	1
⋮	⋮								
⋮	127	1	0	0	0	0	0	0	0
⋮	128	0	1	1	1	1	1	1	1
⋮	⋮								
VRB	255	0	0	0	0	0	0	0	0

6-4. Pin connection



CIRCUIT DESCRIPTION

6-5. Explanation of terminals

No.	Name	Explanation	Equivalent circuit
1 ~ 8	D0 ~ D7	D0 (LSB) ~ D7 (MSB) output	
10, 11	DVDD	Digital +5V	
12	CLK	Clock input	
13	SEL	- When SEL=Low, mono-multi generates a clamp by using a fall of 14 pin (Sync) input as a trigger. - When SEL=High, mono-multi generates a clamp by using a rise of 14 pin (Sync) input as a trigger.	
14	SYNC	Trigger pulse input for mono-multi. Polarity of trigger can be set according to 13 pin (SEL) input.	
15	PW	- When mono-multi generates a clamp pulse, pulse width is determined by outside R and C. - When a clamp pulse is directly input, it is input to 15 pin (PW). Voltage signal in Low section is clamped. (At this time, 14 pin [Sync] is fixed to Low or High.)	
16, 19, 20	AVDD	Analog +5V	
17	VRTS	If shorted to VRT, about +2.6V is generated.	
18	VRT	Reference voltage (Top)	
24	VRB	Reference voltage (Bottom)	

CIRCUIT DESCRIPTION

No.	Name	Explanation	Equivalent circuit
21	V _{IN}	Analog input	
22, 23	AV _{SS}	Analog GND	
25	VR _{BS}	If shorted to VR _B , about +0.5V is generated.	
26	V _{REF}	Clamp reference voltage input. Clamps so that reference voltage and input signal of clamp section will be the same.	
27	CCP	Integrates voltage for clamp control. Change of CCP voltage and V _{IN} are positive phase.	
28, 31	DV _{SS}	Digital GND	
29	$\overline{\text{CLE}}$	- Clamp function works when $\overline{\text{CLE}}$=Low. - Clamp function is turned OFF and only ordinary A/D converter function is available when $\overline{\text{CLE}}$=High. - Clamp pulse can be measured by connecting $\overline{\text{CLE}}$ pin to DV_{DD} through a resistance higher than 100Ω.	
30	$\overline{\text{OE}}$	Data is output when $\overline{\text{OE}}$ =Low. Impedance of D0 ~ D7 terminals becomes high when $\overline{\text{OE}}$ =High.	

CIRCUIT DESCRIPTION

7. Y/C 2-channel D/A Converter : CXD1177Q (IC2, X35-2110)

7-1. Outline

CXD1177Q is an 8-bit high-speed D/A converter for the video band, having inputs and outputs for two channels of Y/C. This converter is suitable for the use in a digital television, graphic display, etc.

7-2. Features

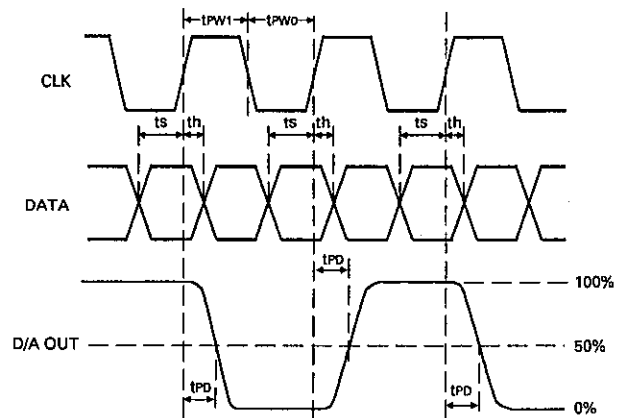
- Resolution of 8 bits.
- Maximum conversion speed of 40MSPS.
- Inputs and outputs of 2 channels of Y/C.
- Differentiation linearity error of ± 0.3 LSB.
- Low power consumption of 160 mW (When 200 Ω Load and 2Vp-p output).
- Only one source voltage of 5V is required.

7-3. Inputs and outputs table

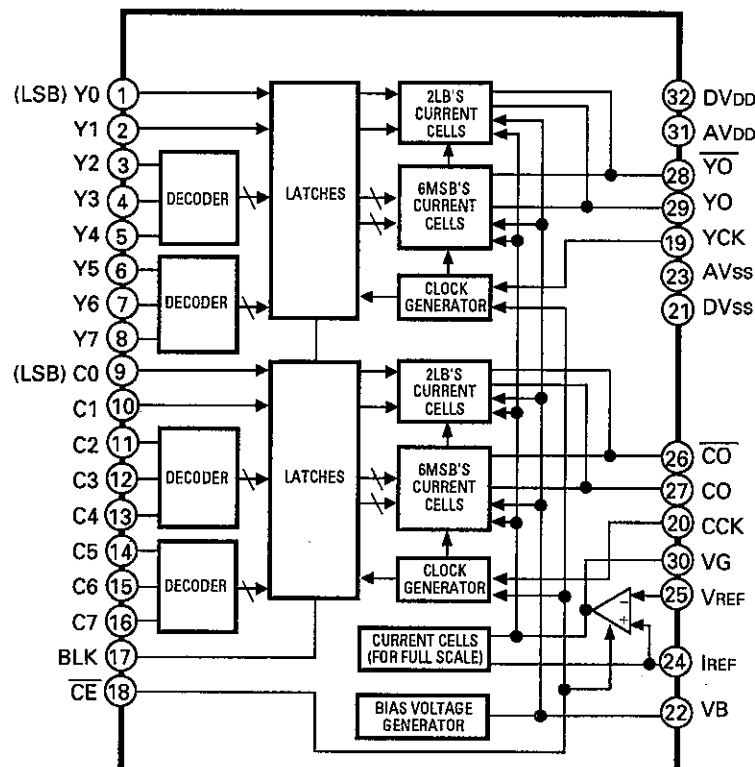
(When output full-scale voltage is 2.00V)

Input code								Output voltage
MSB							LSB	
1	1	1	1	1	1	1	1	2.0V
								↓
1	0	0	0	0	0	0	0	1.0V
								↓
0	0	0	0	0	0	0	0	0V

7-4. Timing chart



7-5. Block diagram



CIRCUIT DESCRIPTION

7-6. Explanation of terminals

No.	Name	Explanation	Equivalent circuit
1 ~ 8	Y0 ~ Y7	Digital input	
9 ~ 16	C0 ~ C7		
17	BLK	Blanking terminal. No signals are output when "H" (Output : 0V), and signals are output when "L".	
18	$\overline{\text{CE}}$	Chip enable terminal. No signals are output (Output : 0V) to minimize power consumption when "H".	
19	YCK	Clock terminal. All input terminals are compatible with TTL-CMOS.	
20	CCK		
21	DVss	Digital GND	

CIRCUIT DESCRIPTION

No.	Name	Explanation	Equivalent circuit
22	VB	Connect the capacitor of 0.1μF.	
23	AVss	Analog GND	
24	IREF	Connect "16R" which is 16 times as high as output resistance "R".	
25	VREF	Set the full-scale rate of output.	
30	VG	Connect the capacitor of 0.1μF.	
26	$\overline{CO}$	Inversion current output pin. Normally, connect to analog GND.	
28	$\overline{YO}$		
27	CO	Current output pin. Output can be taken out by connecting a resistance.	
29	YO		
31	AVDD	Analog GND.	
32	DVDD	Digital GND.	

CIRCUIT DESCRIPTION

8. Memory Control (1) : KAG03 (IC4, X35-2110)

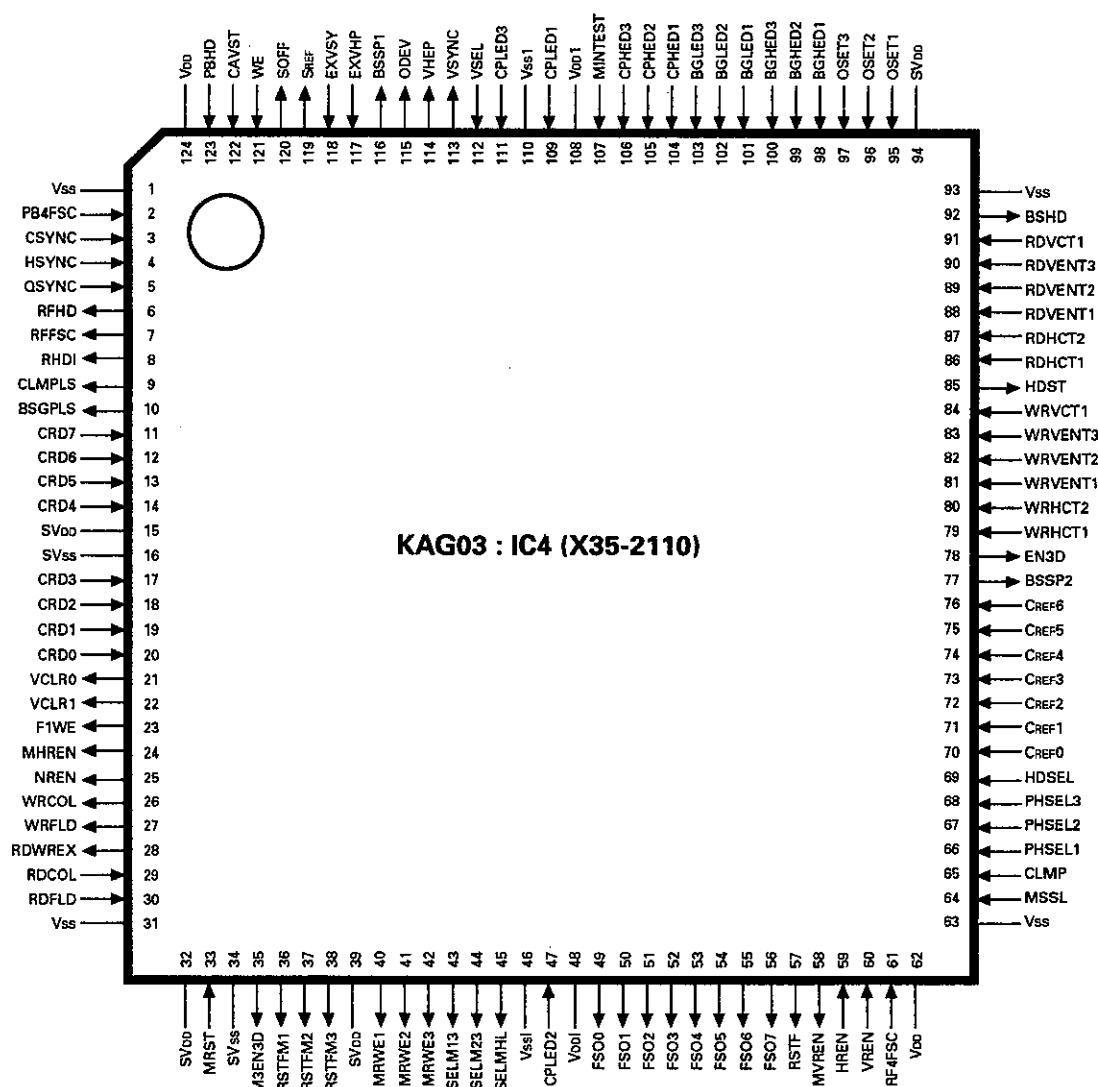
8-1. Outline

KAG03 has a field synchronizing function for special replay of still pictures etc. It also generates signals to control the field memory for time axis correction and controls KAG05 for 3- dimensional Y/C separation.

8-2. Features

- Built-in TBC of PLL type.
- Built-in digital clamp circuit.
- Built-in H system phase error detecting circuit.
- Built-in control function for 3-dimensional Y/C separation (KAG05).
- Special replay based on still pictures by control of field memory is available.

8-3. Pin connection



CIRCUIT DESCRIPTION

8-4. Pin function

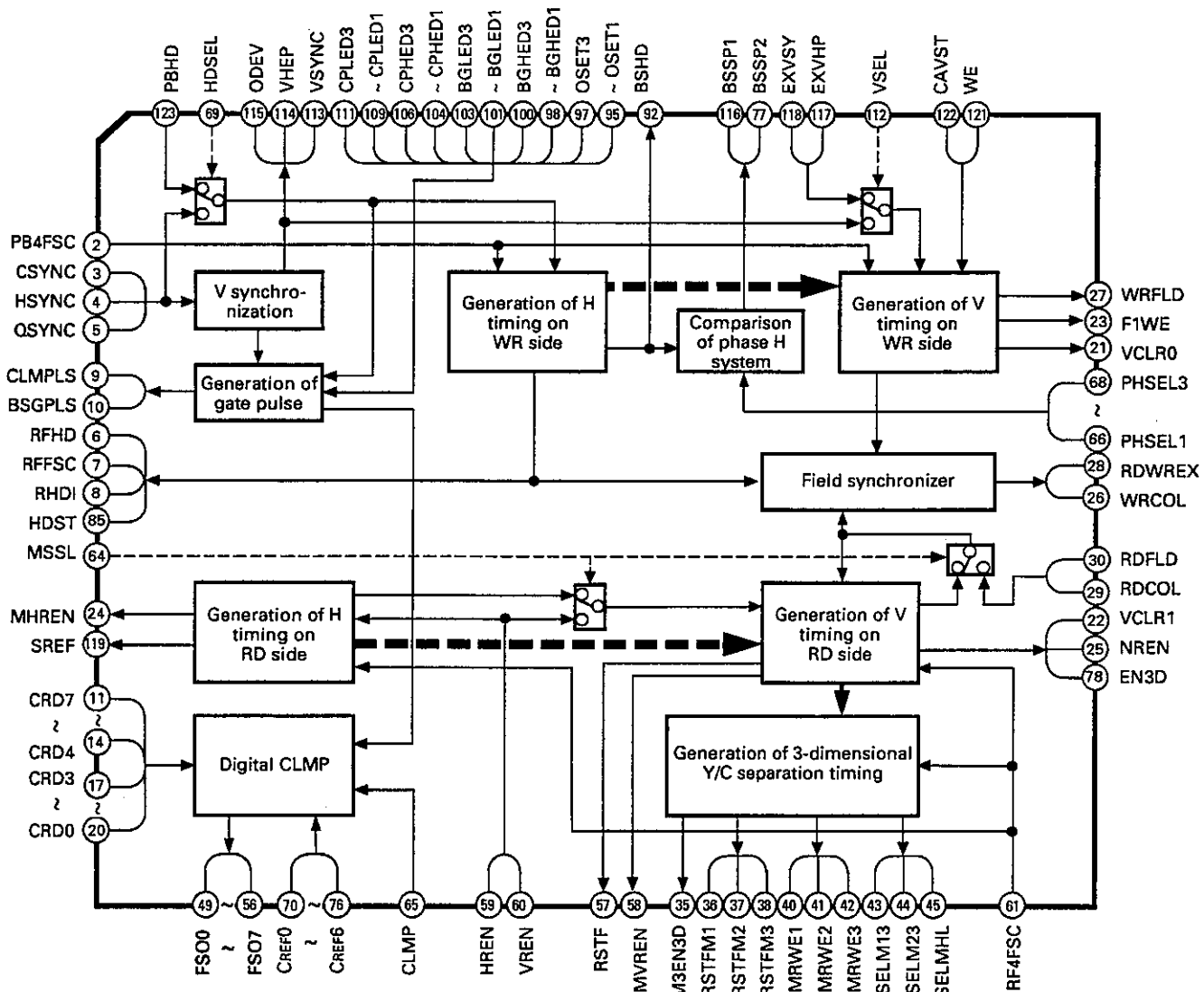
Pin No.	Symbol	I/O	Function
1	Vss	–	GND
2	PB4FSC	I	WR side clock input
3	CSYNC	I	Composite sync input
4	HSYNC	I	Half killer pulse input
5	QSYNC	I	Quarter killer pulse input
6	RFHD	O	Reference HD output (Division of PB4fSC into 910)
7	RFFSC	O	Reference FSC output (Division of PB4fSC into 4)
8	RHDI	O	Drop-out correction reference signal
9	CLMPLS	O	Clamp pulse
10	BSGPLS	O	Burst gate pulse
11 ~ 14	CRD7 ~ CRD4	I	Digital clamp input (CRD7 : MSB)
15	Vdd	–	Power supply
16	Vss	–	GND
17 ~ 20	CRD3 ~ CRD0	I	Digital clamp input (CRD0 : LSB)
21	VCLR0	O	TBC WR side memory address reset signal
22	VCLR1	O	TBC RD side memory address reset signal
23	F1WE	O	TBC memory write enable signal
24	MHREN	O	H reference signal on TBC RD side (When master operates)
25	NREN	O	Noise reduction enable signal
26	WRCOL	O	WR side color phase signal
27	WRFLD	O	WR side field signal
28	RDWREX	O	RD-WR field agreement signal
29	RDCOL	I	RD side color phase signal in slave mode
30	RDFLD	I	Field phase signal on RD side (When slave operates)
31	Vss	–	GND
32	Vdd	–	Power supply
33	MRST	I	Master reset
34	Vss	–	GND
35	M3EN3D	O	Y/C separation 3-line fixed signal matched to movement (When FM=3M)
36 ~ 38	RSTFM1 ~ RSTFM3	O	Field memory (1) ~ (3), RD-WR reset signal (FM=3M)
39	Vdd	–	Power supply
40 ~ 42	FMRWE1 ~ FMRWE3	O	Field memory (1) ~ (3), RD-WR enable signal
43	SELM13	O	Field memory output (1), (3) setting signal
44	SELM23	O	Signal to change field memory outputs (2) and (3)
45	SELMHL	O	Field memory (3), Input bit selecting signal
46	Vss	–	GND
47	CPLED2	I	Switch to set fall of ground pulse (Bit 2)
48	Vdd	–	Power supply
49 ~ 56	FSO0 ~ FSO7	O	Digital clamp output (FSO0 : LSB, FSO7 : MSB)
57	RSTF	O	Field memory RD-WR reset signal (FM=4M)
58	MVREN	O	V reference signal on TBC RD side (When master operates)
59	HREN	I	H reference signal on TBC RD side (When slave operates)
60	VREN	I	V reference signal on TBC RD side (When slave operates)

CIRCUIT DESCRIPTION

Pin No.	Symbol	I/O	Function
61	RF4FSC	I	RD side clock input
62	VDD	–	Power supply
63	VSS	–	GND
64	MSSL	I	Master/Slave selecting switch (Master=L)
65	CLMP	I	Digital clamp enable switch (enable=H)
66 ~ 68	PHSEL1 ~ PHSEL3	I	HD phase control switch for burst slip (PHSEL1 : LSB, PHSEL3 : MSB)
69	HDSEL	I	Playback HD selecting switch
70 ~ 76	CREF0 ~ CREF6	I	Digital clamp reference level setting switch (CREF0 : LSB, CREF6 : MSB)
77	BSSP2	O	HD phase difference output signal (2)
78	EN3D	O	Y/C separation 3-line fixed signal matched to movement (When FM=4M)
79	WRHCT1	I	Test pin (WR side V counter · carry up signal)
80	WRHCT2	I	Test pin (WR side V counter · carry up signal)
81 ~ 83	WRVENT1 ~ WRVENT3	I	Test pin (WR side V counter · enable signal)
84	WRVCT1	I	Test pin (WR side V counter · carry up signal)
85	HDST	O	Reference H of trapezoidal wave for PLL of H system
86	RDHCT1	I	Test pin (RD side H counter · carry up signal)
87	RDHCT2	I	Test pin (RD side H counter · carry up signal)
88 ~ 90	RDVENT1 ~ RDVENT3	I	Test pin (RD side V counter · carry up signal)
91	RDVCT1	I	Test pin (RD side H counter · carry up signal)
92	BSHD	O	Reference signal to detect of HD phase difference
93	VSS	–	GND
94	VDD	–	Power supply
95 ~ 97	OSET1 ~ OSET3	I	Timing pulse · Off set setting switch (OSET1 : LSB, OSET3 : MSB)
98 ~ 100	BGHED1 ~ BGHED3	I	Burst gate pulse rise edge position setting switch (BGHED1 : LSB, BGHED3 : MSB)
101 ~ 103	BGLED1 ~ BGLED3	I	Burst gate pulse fall position setting switch (BGLED1 : LSB, BGLED3 : MSB)
104 ~ 106	CPHED1 ~ CPHED3	I	Clamp pulse rise position setting switch (CPHED1 : LSB, CPHED3 : MSB)
107	MINTEST	I	I/O buffer test pin
108	VDD	–	Power supply
109	CPLED1	I	Switch to set fall of clamp pulse (LSB)
110	VSS	–	GND
111	CPLED3	I	Switch to set fall of clamp pulse (MSB)
112	VSEL	I	VSYNC input selecting switch
113	VSYNC	O	VSYNC output
114	VHEP	O	V blanking output
115	ODEV	O	Field signal
116	BSSP1	O	HD phase difference output signal (1)
117	EXVHP	I	V blanking input (V sync external input state)
118	EXVSY	I	VSYNC input (V sync input from outside)
119	SREF	O	Disc servo reference signal
120	SOFF	O	Signal to turn OFF disc servo when WR-RD approaches.
121	WE	I	TBC memory writing mask signal
122	CAVST	I	TBC memory writing mask signal
123	PBHD	I	Playback HD
124	VDD	–	Power supply

CIRCUIT DESCRIPTION

8-5. Block diagram



8-6. Explanation of operation

The video signal is A/D converted, then input to KAG03, where it is clamped, then output. The clamp level is set with 7-bits of CREF0 ~ CREF6. If the CLMP terminal is set to "L", clamping can be stopped. In LVD-Z1, digital signals are not clamped.

• Synchronizing system on writing side

Both field signal (ODEV) and equivalent blanking period pulse (VHEP) are generated by CSYNC, HSYNC, and QSYNC which are input after synchronization separation of V, and they are used as the reference signal of V on writing side.

The H timing generating block consists of a counter and a decoder and generates various timing pulses for 1H section. It also sends the timing pulse to V timing

generating block. In the V timing generating block, the reference pulse VCLR0 on writing side of the field synchronizer and the writing enable signal F1WE of the memory are generated.

• Timing processing system on reading side

While the master is in operation, the counter of the H system and that of the V system operate according to the self-reset determined by the reset timing, and the reference signal VCLR1 on the reading side is generated.

While the slave is in operation, HREM is input as the reference signal of H and VREN as the reference signal of V from KAM01 for the operation. Various timing signals for 3-dimensional Y/C separation are generated according to these reference signals.

CIRCUIT DESCRIPTION

8-7. Explanation of each block

• Judgment of field and separation of vertical synchronization

Even in the gate array, digital vertical synchronization separation VSYNC and blanking section VHEP can be extracted in the IC by inputting CSYNC, HSYNC (HALF KILLER PULSE), and QSYNC (QUARTER KILLER PULSE).

Since digital separation is applied, however, when LD signal, VTR signal, etc. which drop-out frequently are handled, the separation may not be continued. To avoid this trouble, the outside input terminals EXVHEP and EXVSY for the vertical synchronization section and blanking section are installed, which are changed with the VSEL signal (Fig. 1).

The signal obtained by dividing 14.31818MHz (4 times the burst signal) into 910 by the above vertical synchronizing signal is held as a sample to output the field judging signal ODEV (The timing of the input and output terminals are shown in Fig. 3 and Fig. 4).

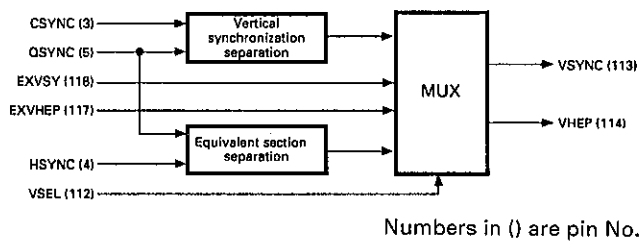


Fig. 1 Vertical synchronization and equivalent section separation

• Generation of gate pulse

The burst gate pulse to compare the phase of each burst and the clamp pulse to clamp both digital and analog signals are generated. The position of each pulse is generated by decoding the count cleared by the replay HD signal (Rise of PBHD or fall of HKPL).

This pulse has an offset to change the clearing position of the counter. The decoded rise and fall values can be changed, too. Accordingly, the positions of various timing pulses can be changed according to the AC characteristics of synchronization separation.

The positions of pulses for various bit settings are shown in Fig. 2 and Table 1. As shown in Fig. 3 and Fig. 4, the clamp pulses are not output which the equivalent section VHEP is at "L".

Gate control SW				Burst gate		Clamp pulse	
3	2	1	OSET	BGHED	BGLED	CPHED	CPLED
0	0	0	0.00	5.09	6.50	7.54	8.10
0	0	1	0.07	5.16	6.57	7.61	8.17
0	1	0	0.14	5.23	6.63	7.68	8.24
0	1	1	0.21	5.30	6.70	7.75	8.31
1	0	0	0.28	5.37	6.77	7.82	8.38
1	0	1	0.35	5.44	6.84	7.89	8.45
1	1	0	0.42	5.51	6.91	7.96	8.52
1	1	1	0.49	5.58	6.98	8.03	8.59

Unit : μsec

Table 1 Gate pulse timing table

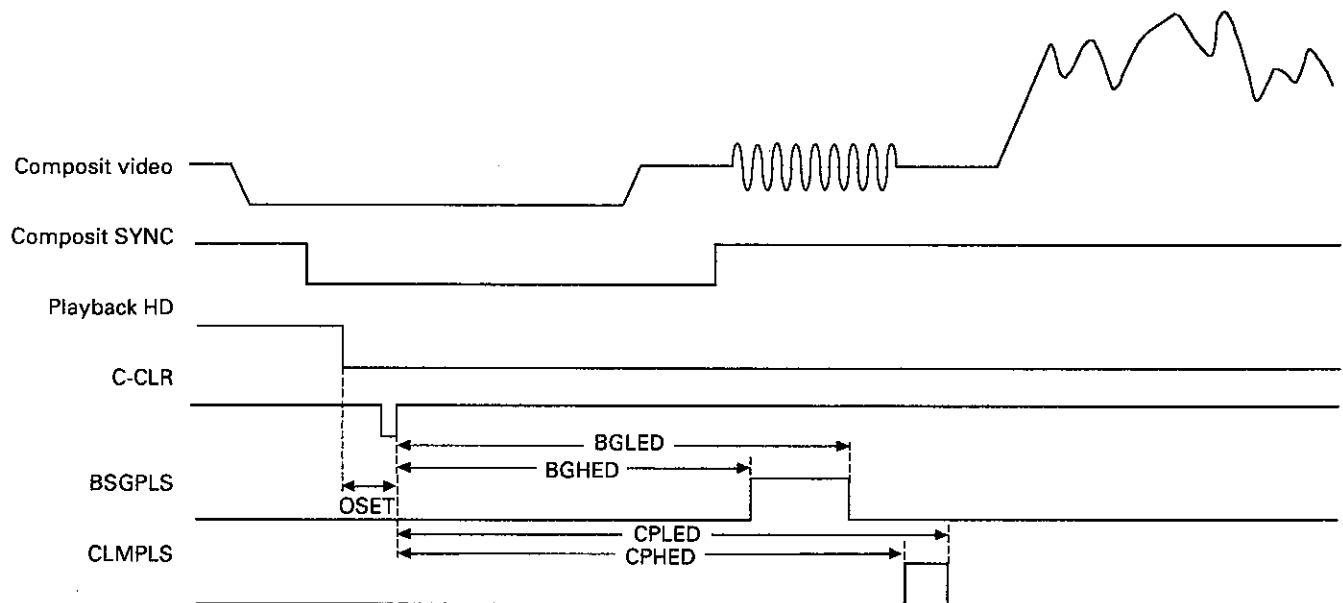


Fig. 2 Gate pulse generation timing

CIRCUIT DESCRIPTION

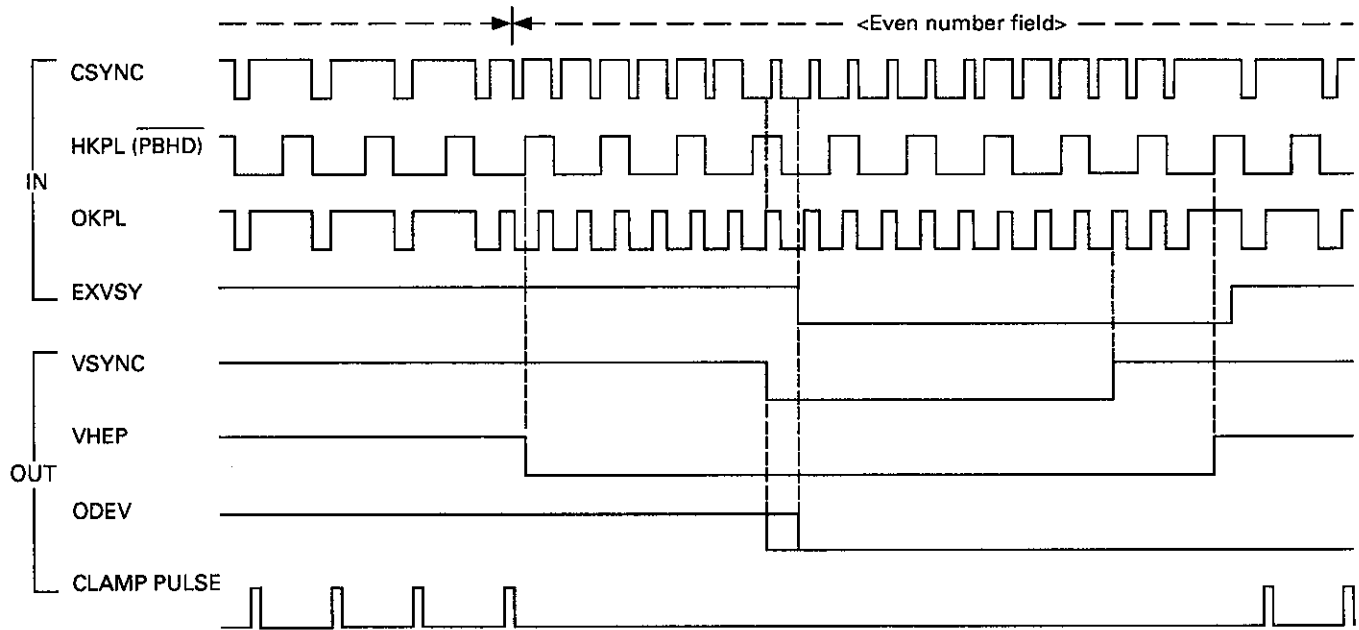


Fig. 3 Various pulse timings of even number field

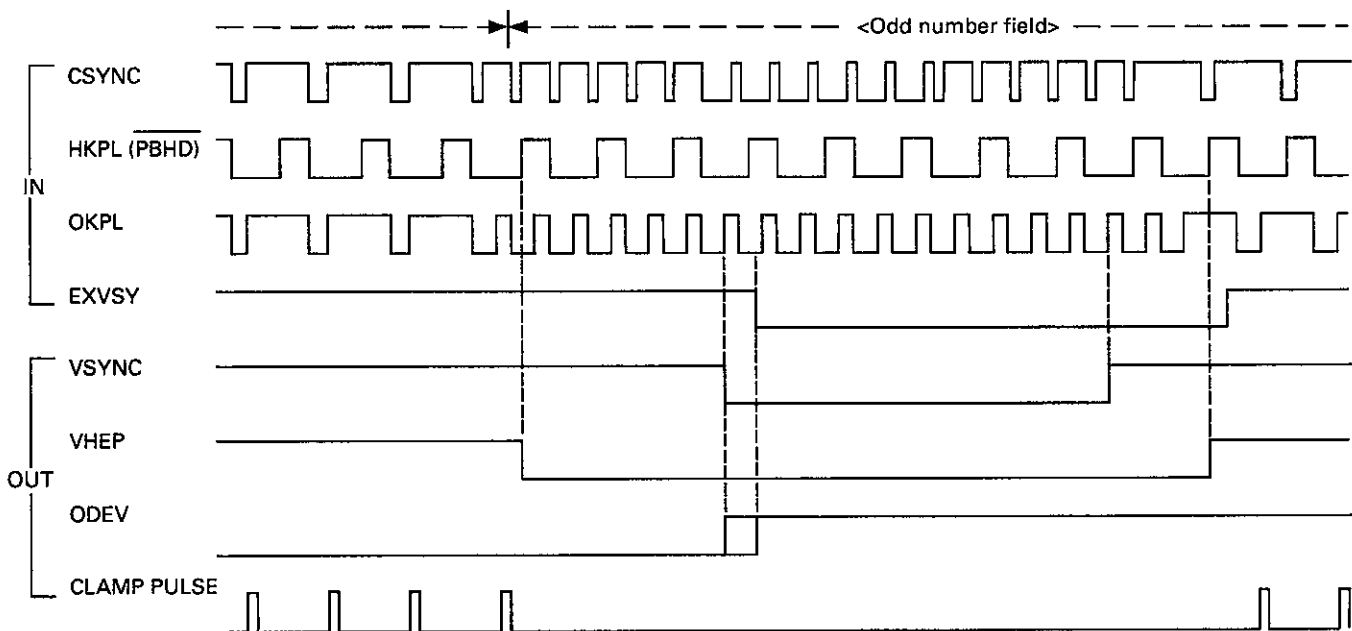


Fig. 4 Various pulse timings of odd number field

CIRCUIT DESCRIPTION

• Timing control on WR side

The timing pulses on WR side for TBC and the control signals on WR side of the field synchronizer are generated. The inside consists of a line counter cleared every 1H and a field counter cleared every 1V.

The counter cleared every 1H uses a clock 4 times as high as the burst signal. Accordingly, if it is cleared at 910 counts, the result is 1H. To obtain a signal divided by this counter into four when PLL for the burst signal is formed, however, it is cleared at 1820 counts which is the sampling frequency equivalent to the least minimum multiple of 910 and 4. Various timing pulses

are generated by decoding that counter value (The timing pulses of the H system are shown in Fig. 5).

Since RFHD in this figure is the reference of the WR counter, the phase of PLL of the H system is adjusted (For example, the gradient of the trapezoid is adjusted in case of LVD-710) so that the fall of RFHD will be at the fall of CSYNC.

RHDI is a reference signal for drop out of replayed HD made by the disc motor control LSI, and HDST is used to start the trapezoid wave. BSHD is used as the reference signal of the PLL of H system for counter-measures against burst slip described separately.

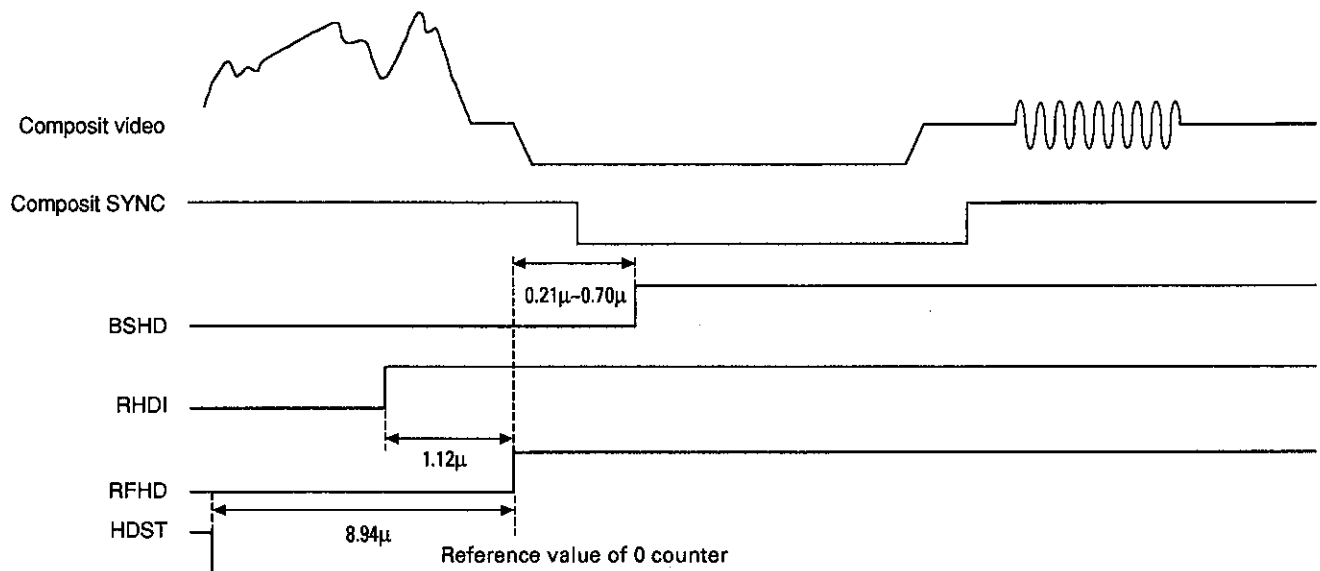


Fig. 5 Various timing pulse of H system

CIRCUIT DESCRIPTION

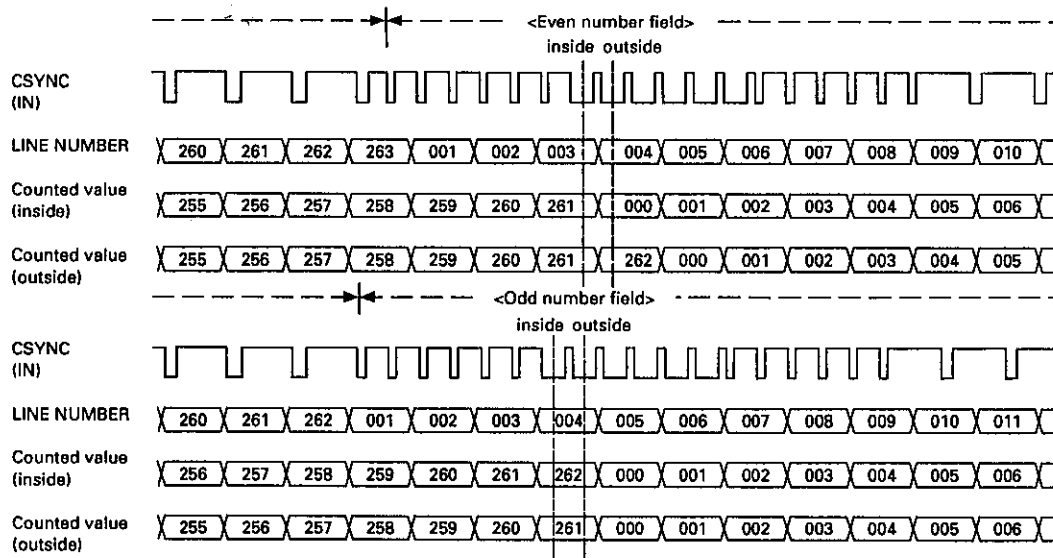


Fig. 6 V counter values

The counter the V system counts 1 every time the counter of the system counts 910. It is cleared at the first 0 count of the H system after the fall of VSYNC.

Since the timing of the vertical synchronizing signal of the inside synchronization separation is different from that of outside synchronizing separation, the counter of the V system becomes 0 at 4H in the odd number field in both cases. In case of the vertical synchronization separation, however, the counter value becomes 0 at 267H in the even number field, and at 268H out of the even number field. In the field synchronizer, the odd number field is defined as 263H and the even number field as 262H for counting (The V counter values are shown in Fig. 6).

The memory clearing VCLR0 on the WR side of the field synchronizer is generated by combining this V counter value and the decoded value of the H counter explained above. The decoded values in and out of the V synchronization separation are different from each other.

• Detection of frame information on WR side

As for the even number and odd number of the field, the field information WRFILD signal on WR side

is obtained by latching the ODEV signal with the VCLR0 signal. Since the starting point of the field defined by this field synchronizer is before the fall of the vertical synchronizing signal, however, the polarities of the ODEV and WRFILD signals are opposite to each other as shown in Table 2. The ODEV signal changes according to the signal input to A/D in the still picture mode, but the WRFILD signal does not change while the FIWE signal is at "H", that is, writing in the memory is masked (The WRCOL signal behaves similarly, too).

Field	ODEV	WRFILD
Odd number	H	L
Even number	L	H

Table 2 Even and odd number flags on WR side

The color information is detected by latching the COLOR signal obtained by latching the WRFSC signal obtained by dividing the VCO signal into four by the VSYNC signal. Because of the frequency interleaving of NTSC, the color phase inverted every frame is detected (Fig. 7 shows the actual output signals).

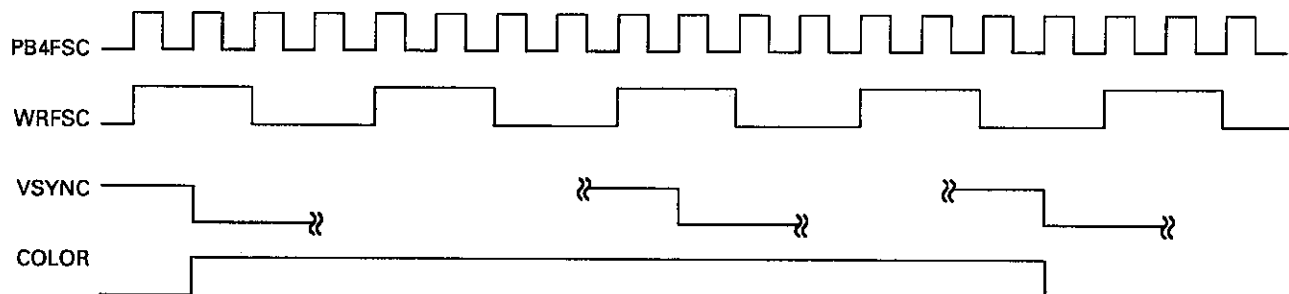


Fig. 7 Generation of color phase signals

CIRCUIT DESCRIPTION

• Digital phase comparison

For the generation of the clock synchronized with the input video signal in the LD mode, a PLL loop is formed in the line system (15.73kHz) to remove the jitter elements of disc servo. Then, a PLL loop is formed in the burst system (3.58MHz) to eliminate the color phase error. Finally, all the error elements are added up to form a closed PLL loop.

Accordingly, if the gains of the line system and burst system are not balanced, they are locked to either system. Even if the gains are fixed to the line system, there is not a problem, as long as the frequency interleaving relationship between the burst system and line system is maintained. If the interleaving relationship is broken as in case of a still picture of the CAV disc, the image may be colorless.

On the other hand, if the gains are locked to the burst system, the phase of the H system is shifted to a multiple of the burst (Burst slip), the above described timing pulse of the WR system is not synchronized with the true video signals. Accordingly, a burst slip must be detected, independent from the closed PLL loop, to adjust the gains of the line system and burst system.

To detect the burst slip, a digital phase comparator of the line system is installed. If PBHD is ahead of BSHD, a rise pulse is output to BSSP1, and if the former is behind the later, a rise pulse is output to BSSP2 (Fig. 8).

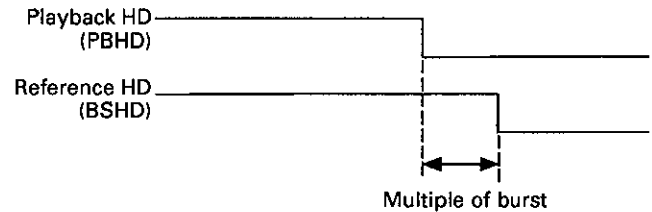


Fig. 8 Burst slip

• Digital clamp

The method of digital clamp was explained in the section of principle. Actually, the buffer is cleared at the rising point of the clamp pulse, then the clamp pulse is input. Eight data are added up, then the result is divided by 8 to obtain the average.

The obtained data and reference data are compared with each other, and the difference is added to the input data. Accordingly, the difference between the clamp reference data and the input data is added to that input data every line.

If the clamp results exceeds 256 when added or they are below 0 when subtracted, the limiter in the latch of the output stage fixes the values to 256 and 0 in the respective cases. The clamp circuit which always set the difference from the reference data to 0 can be turned off (Fig. 9 shows the configuration and timing of the clamp circuit).

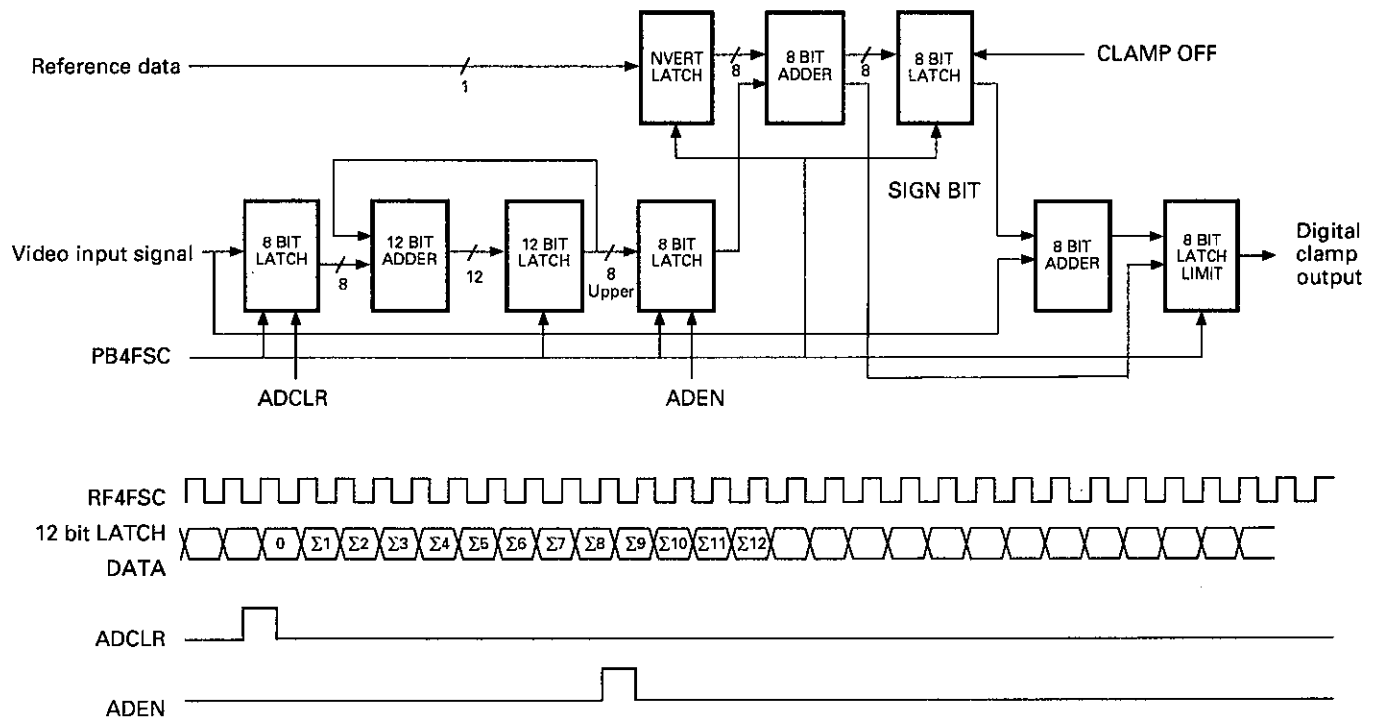


Fig.9 Clamp circuit and clamp timing

CIRCUIT DESCRIPTION

• Timing control on RD side

This chip generates the timing pulse on the RD side for TBC, the control signal on RD side for the field synchronizer, and the reference signal of the disc servo. The inside consists of the H counter which is cleared every 910 counts and the V counter which is enabled by the clearing signal of the H counter and cleared alternately every 263 and 262 counts, and the section which decodes those counter values and generates pulses.

The counters are cleared in the master mode (MHREN) in which the counters count and clear themselves or in the slave mode in which clearing signals

(HREN and VREN) are input from outside to synchronize the counters with the outside signals.

Generally, this chip is used in the slave mode since it is used together with a noise reduction chip etc. It is used in the master mode when only TBC needs to be operated. The master and slave modes can be changed to each other by changing MSSL.

MODE	Setting
MASTER	L
SLAVE	H

Table 3 Outside synchronizing mode

(A) When fields are matched

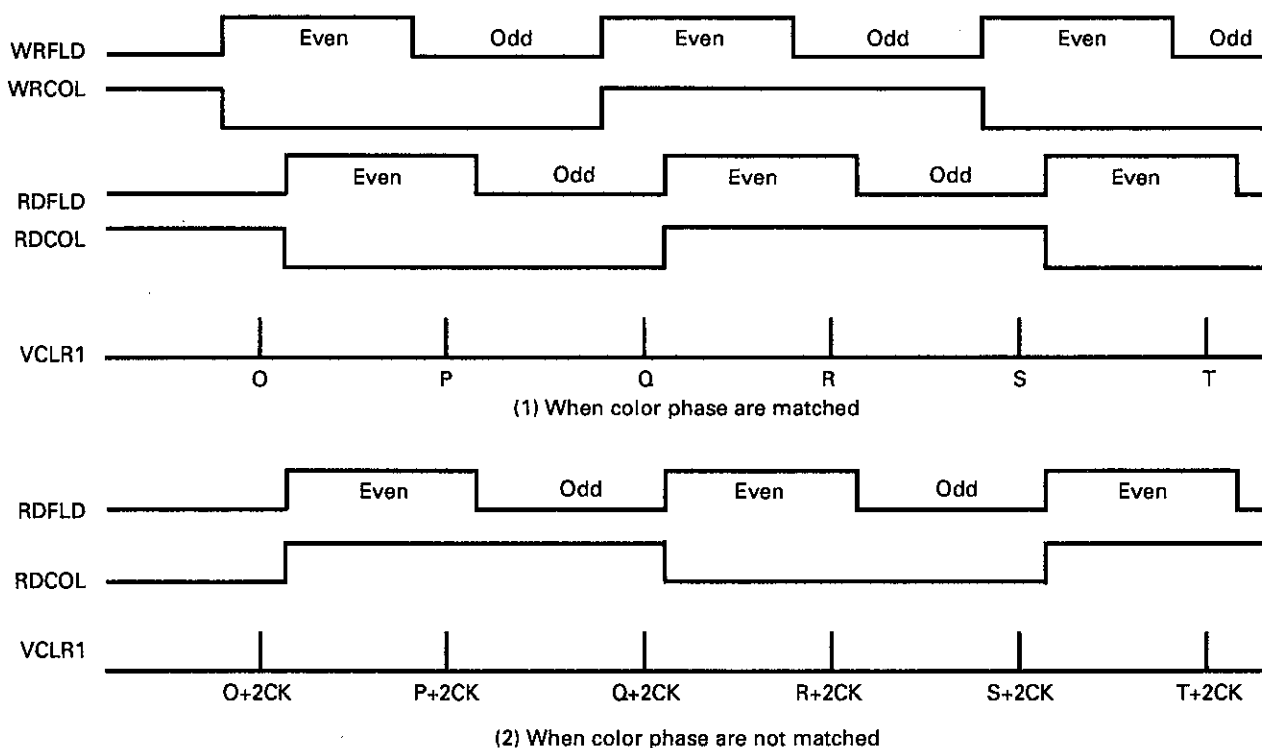
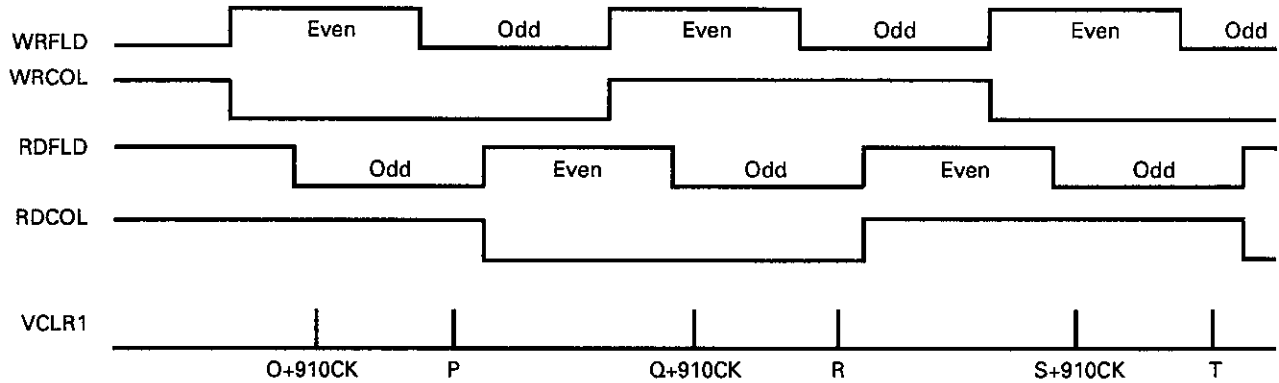


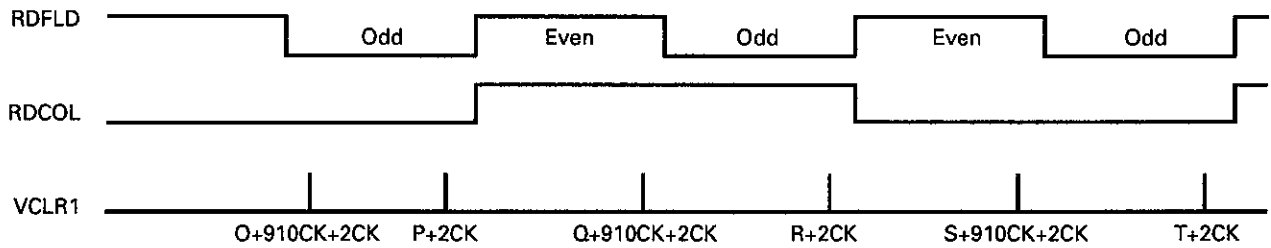
Fig.10 Reset timing on RD side in case of matched fields

CIRCUIT DESCRIPTION

(B) When fields are not matched



(1) When color phase are matched



(2) When color phase are not matched

Fig.11 Reset timing on RD side in case of unmatched fields

(C) In case of still picture

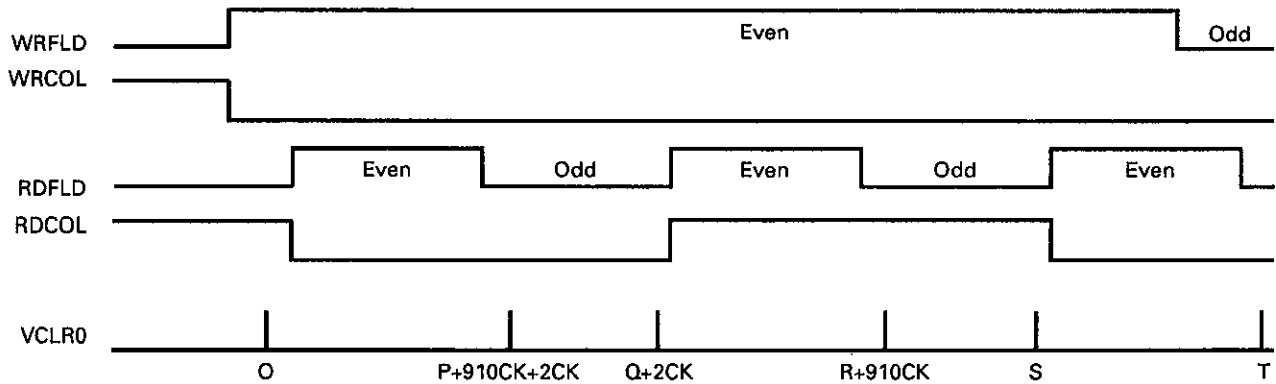


Fig.12 Reset timing on RD side in case of still picture

CIRCUIT DESCRIPTION

• **Control on reading side of field synchronizer**

The basic operation of the TBC and field synchronizer is realized by reading the data written in the memory with the reference signal from the reference position. If the reference position for reading is not changed according to the wringing condition, the read video signal is abnormal.

Since the odd number field is set to 263H and the even number field to 262H for the control of the field synchronizer, if the fields on the writing side and reading side are different from each other, some lines may not be read and undefined data may be read. In addition, since the color phases on the writing side and reading side are also different from each other, the relationship of frequency interleaving is broken.

As the result, the continuity of the burst signal (continuity of color) cannot be maintained and the images may not be colored of their color phases may be shifted. In case of a still picture of the memory, particularly, since the data in one field must be read under various conditions, various controls are required.

The field and color phase on the reading side are fixed by the timing at a reset, and their continuity is maintained until the power is turned off. That is, the filed signal changes to 263H and 262H alternately, and the color phase information changes when the odd number field changes to the even number field.

When the fields and colors on the writing side and reading side are matched to each other and the reset points on the reading side are set to the reference positions "P", "Q", "R", "S", "T", and "U" as shown in Fig. 11 (1), if the field and color information on the writing side are different from those points, the reset points on the reading side are shifted relatively as shown in Fig. 10 ~ Fig. 12.

(A) If the fields on the writing side and reading side are matched to each other as shown in Fig. 10, the reset position on the reading side is delayed by 2CK

depending on the matching condition of the color phase. To delay the reset position on the reading side means to turn the color phase on the reading side by 180°. Since the sampling frequency is four times the burst signal, the delay of 2CK is equivalent to turning the phase by a half period of the burst signal, or 180°.

(B) When the fields on the writing side and reading side are different from each other and the data of the odd number field is read in the even number field, only the data of 262 lines are read while the data of 263 lines must be read. When the data of the even number field is read in the odd number field, an undefined data is read at the 263th line since there is no data of the 263th line.

For this reason, as shown in Fig. 11, the reset position to read the odd number field is delayed by 1H to keep the reading position of the even number field at the reference position. As the result, all the 263 lines in the odd number field can be read, and only the 262 lines is read and any undefined data is not read from the even number field.

If the color phase is different, the reset position on the reading side is delayed by 2CK. If the fields are different, it is impossible to judge if the color phases are matched. If the still picture of in the memory is considered, however, matching of the color phases can be judged as shown in Fig. 11 (1).

(C) In case of a still picture in the memory, both field and color on the writing side are kept fixed, the signals are changed to video signals on the reading side according to the NTSC Standard. If the fields are different, the reset position on the reading side is shifted by 1H, similarly to the case of a moving picture. If the color phases are different, the reset position is shifted by 2CK (As shown in Fig. 12).

CIRCUIT DESCRIPTION

• Control of 3-dimensional Y/C separation

For 3-dimensional Y/C separation, a signal of difference of 1 frame is required. If sampling is executed at 4fsc and 8bits, the following memory capacity is required to delay by 1 frame.

$$8 \times 910 \times 525 = 3,822,000 \text{ bits} \dots\dots\dots (1)$$

The capacity of the field memory in the market at present is as follows.

$$262,144 \times 4 = 1,048,576 \text{ bits} \dots\dots\dots (2)$$

Accordingly, $(1) / (2) = 3.64$ units of the memory are required.

In the vertical blanking section of the NTSC signal and the section from the horizontal synchronizing signal section to the color burst signal (Fig. 13), if all the frames are perfectly correlated to one another, all the

lines are perfectly correlated to one another, too. If the frames are not correlated to one another, the lines are not correlated to one another, either. Accordingly, the difference among the frames is eliminated and the 3-dimensional processing is not required. Therefore, 3-line processing is performed forcedly not to take the difference among the frames.

As the result, the necessary capacity of the field memory is as follows.

$$8 \times (910 - 120) \times (525 - 30) = 3,128,400 \text{ bits} \dots\dots (3)$$

Accordingly, the quantity of the necessary memory is $(3) / (2) = 2.98$ pieces, that is, the data of the difference among the frames can be stored in three field memories.

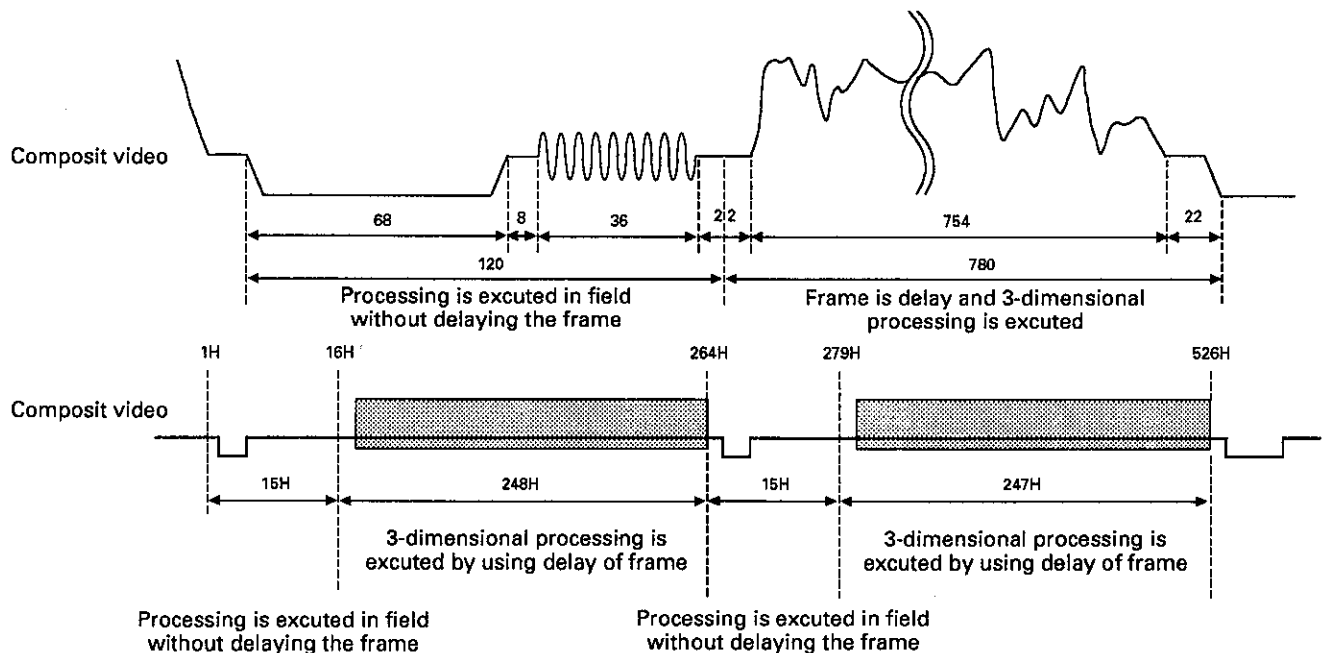


Fig. 13 Forced 3-line processing section

CIRCUIT DESCRIPTION

Since all the field memories are for 4-bit operation at present, if three memories are used, the upper 4bits and lower 4bits must be changed over when used (The timing chart for the use of the memories in that case is shown in Fig. 14). Although the horizontal synchronizing section, burst section, and a part of the back porch and front porch are write-masked actually as explained above, only the V section is shown in this figure.

The 30 lines among the 525 lines are not written in the memory. The other 495 lines are divided into 3 (165 lines each). The first 165 lines are written in the

memories "1" and "2", the second 165 lines in the memories "2" and "3", and the last 165 lines in the memories "1" and "3". The memory "2" is used to record only the lower 4bits. The upper 4bits are selected with the SELM13 signal.

RSTF1 ~ RSTF3 are the address resets of each field memory. The frames are reset at interval of 165 lines. FMWRE1 ~ FMWRE3 are write and read enable signals of each field memory. SEL23 is the signal to select a memory to record the lower 4bits, and SELMHL is used to select a memory from which the upper 4bits will be output.

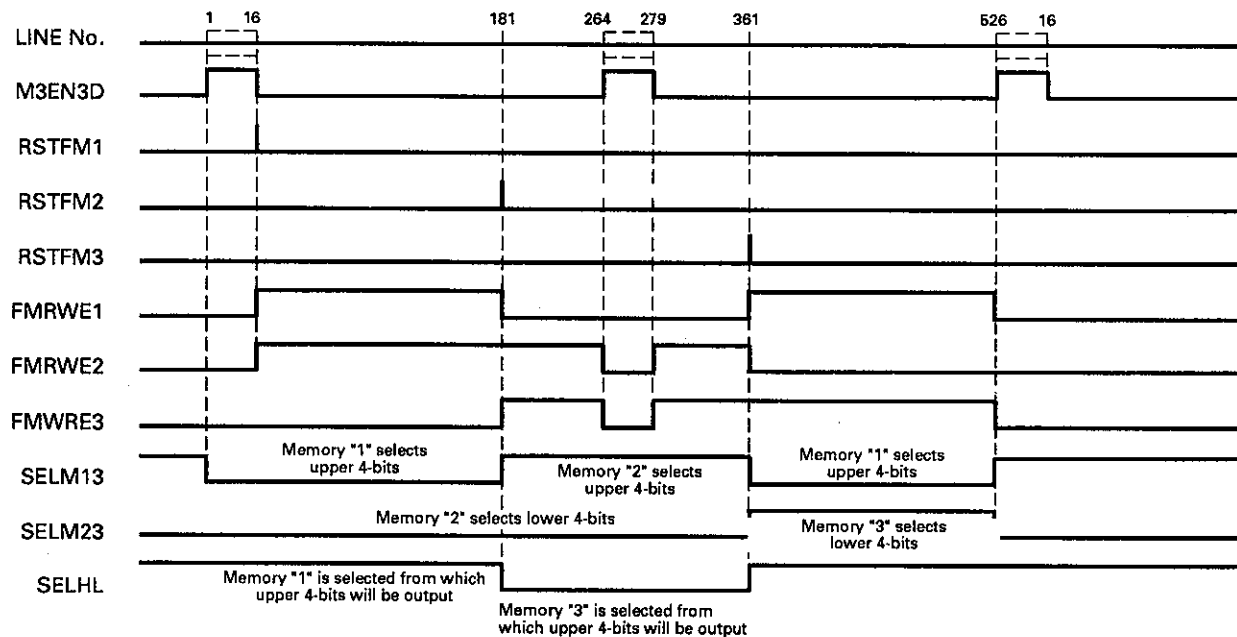


Fig.14 3M 4-bits timing field memory (only V section)

CIRCUIT DESCRIPTION

9. Digital Comb Filter : KAG04 (IC9, X35-2110)

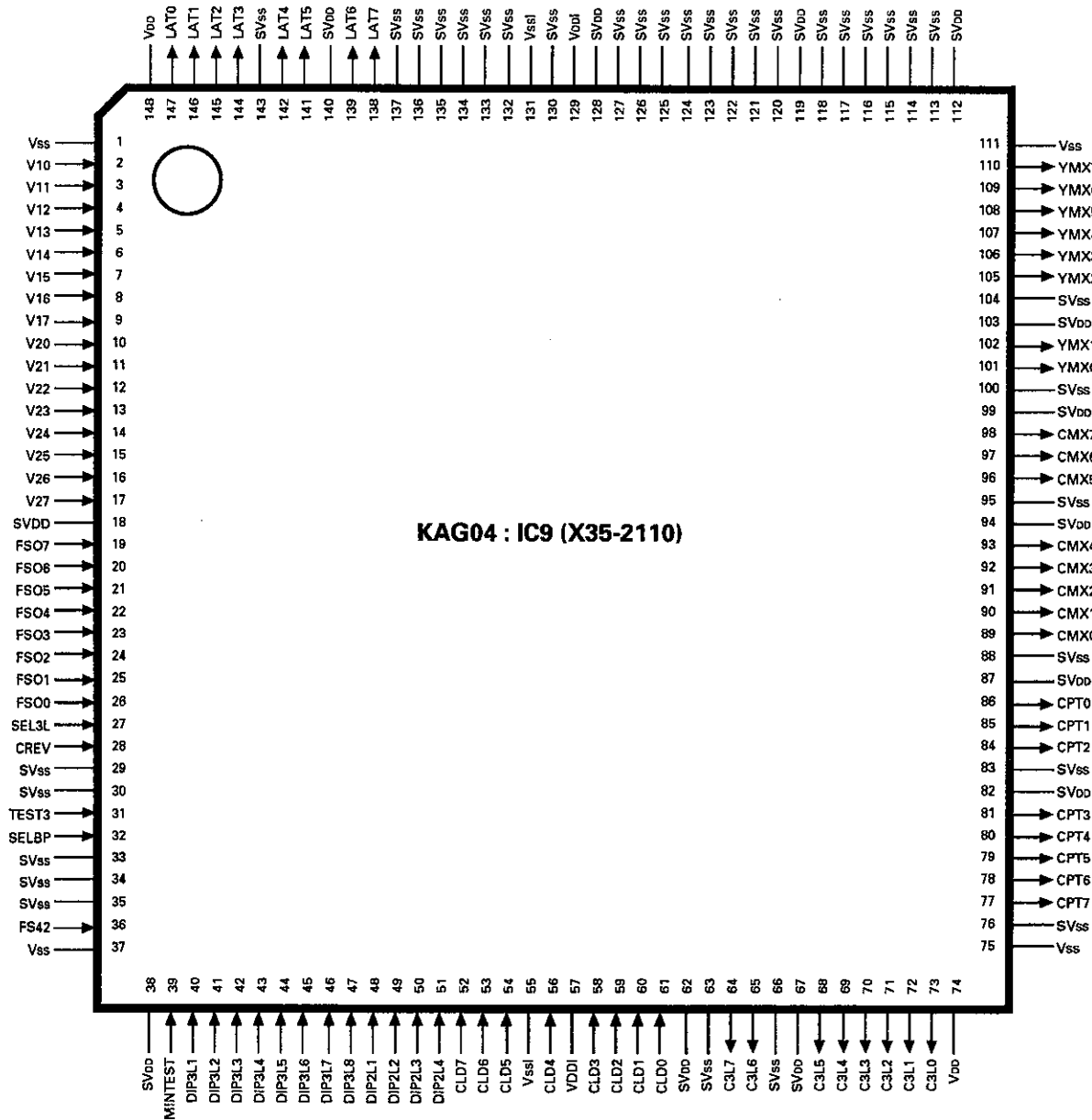
9-1. Outline

KAG04 is a 3-line digital comb filter for NTSC, which can execute Y/C separation well and which causes less dot disturbance and cross color.

9-2. Features

- 3-line Y/C separation by judging color correlation.
- A 3-dimensional Y/C separation filter can be made up if this filter is combined with KAG05.
- Clock of 4fsc and formation by 8bits.
- Separation characteristics can be changed by changing the parameter values and judging formula.

9-3. Pin connection



CIRCUIT DESCRIPTION

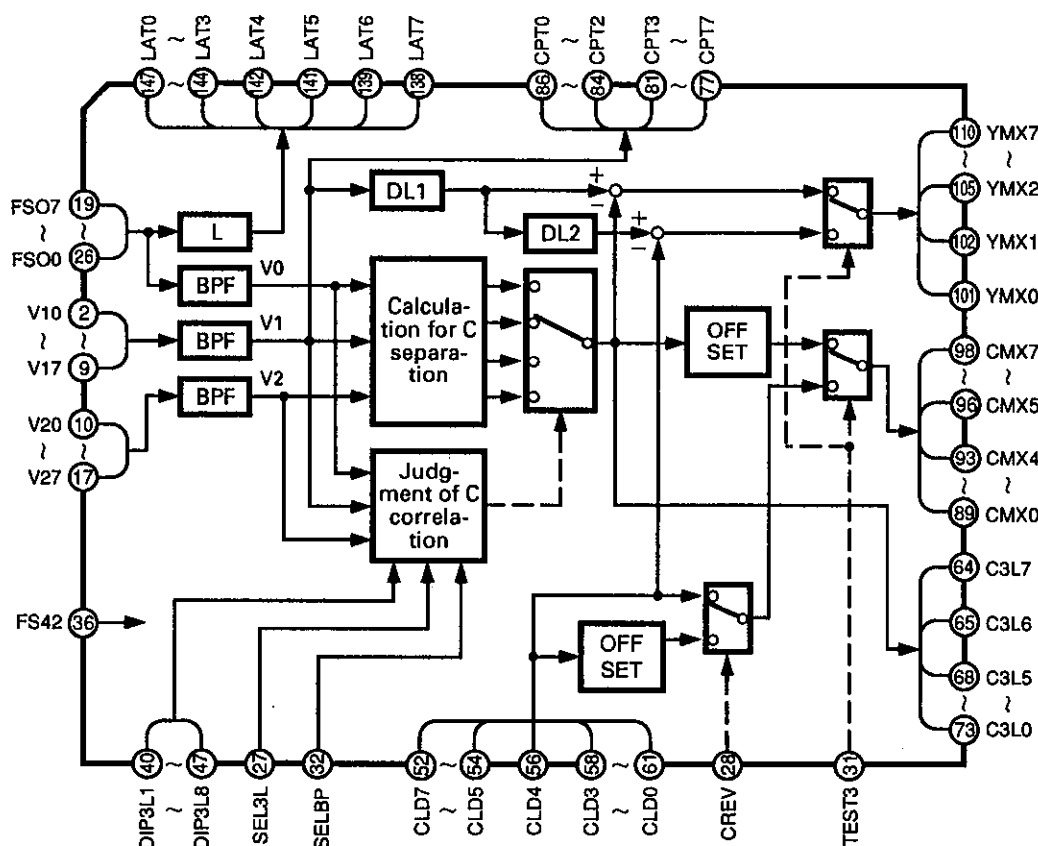
9-4. Pin function

Pin No.	Name	I/O	Function
1	Vss	–	GND
2 ~ 9	V10 ~ V17	I	1H delay signal input V10 : LSB, V17 : MSB
10 ~ 17	V20 ~ V27	I	2H delay signal input V20 : LSB, V27 : MSB
18	SVdd	–	Power supply
19 ~ 26	FSO7 ~ FSO0	I	Composite signal input FSO7 : MSB, FSO0 : LSB
27	SEL3L	I	Change of 3-line judging formula "L" : BPF, "H" : 3-line
28	CREV	I	Change of C signal symbol "L" : Symbol used, "H" : Symbol not used
29, 30	SVss	–	GND
31	TEST3	I	Comb filter test pin "L" : For movement, "H" : Comb filter
32	SELBP	I	Change of BPF judging formula "L" : V1–V0, "H" : V1+V2
33 ~ 35	SVss	–	GND
36	FS42	I	Clock input (4fsc=14.31818MHz)
37	Vss	–	GND
38	SVdd	–	Power supply
39	MINTEST	I	Test pin fixed 'L'
40 ~ 47	DIP3L1 ~ DIP3L8	I	3-line change-over level DIP3L1 : LSB, DIP3L8 : MSB
48 ~ 51	DIP2L1 ~ DIP2L4	I	2-line change-over level fixed 'L'
52 ~ 54	CLD7 ~ CLD5	I	3-dimensional C signal input CLD7 : MSB
55	Vssl	–	GND
56	CLD4	I	3-dimensional C signal input
57	Vddl	–	Power supply
58 ~ 61	CLD3 ~ CLD0	I	3-dimensional C signal input CLD0 : LSB
62	SVdd	–	Power supply
63	SVss	–	GND
64, 65	C3L7, C3L6	O	Comb filter C signal output
66	SVss	–	GND
67	SVdd	–	Power supply
68 ~ 73	C3L5 ~ C3L0	O	Comb filter C signal output C3L0 : LSB

Pin No.	Name	I/O	Function
74	Vdd	–	Power supply
75	Vss	–	GND
76	SVss	–	GND
77 ~ 81	CPT7 ~ CPT3	O	1H composite output, CPT7 : MSB
82	SVdd	–	Power supply
83	SVss	–	GND
84 ~ 86	CPT2 ~ CPT0	O	1H composite output, CPT0 : LSB
87	SVdd	–	Power supply
88	SVss	–	GND
89 ~ 93	CMX0 ~ CMX4	O	C output for movement CMX0 : LSB
94	SVdd	–	Power supply
95	SVss	–	GND
96 ~ 98	CMX5 ~ CMX7	O	C output for movement CMX7 : MSB
99	SVdd	–	Power supply
100	SVss	–	GND
101, 102	YMX0, YMX1	O	Y output for movement YMX0 : LSB
103	SVdd	–	Power supply
104	SVss	–	GND
105 ~ 110	YMX2 ~ YMX7	O	Y output for movement YMX7 : MSB
111	Vss	–	GND
112	SVdd	–	Power supply
113 ~ 118	SVss	–	GND
119	SVdd	–	Power supply
120 ~ 127	SVss	–	GND
128	SVdd	–	Power supply
129	Vddl	–	Power supply
130	SVss	–	GND
131	Vssl	–	GND
132 ~ 137	SVss	–	GND
138, 139	LAT7, LAT6	O	Composite signal output LAT7 : MSB
140	SVdd	–	Power supply
141, 142	LAT5, LAT4	O	Composite signal output
143	SVss	–	GND
144 ~ 147	LAT3 ~ LAT0	O	Composite signal output (LAT0 : LSB)
148	Vdd	–	Power supply

CIRCUIT DESCRIPTION

9-5. Block diagram



9-6. Explanation of block

1) Judgment of C correlation

Correlation among the lines is checked by the judging formulae, and a signal to select the most suitable calculation of C separation is output. The following four judging formulae are used for the cases where the three lines are correlated to one another (3-line) and where the lines are not correlated to one another (BPF).

- When $(V1+V0) \leq A$ and $(V1-V0) \leq A$, BPF is selected (1)
- When $(V1+V0) > A$ and $(V1+V2) > A$, BPF is selected (2)
- When $(V1+V0) / 2 < (V1-V0)$ and $(V1-V0) / 2 < (V1+V0)$,
BPF is selected (3)
- When $(V0+V2) / 4 < V1 < (V0+V2)$, 3-line is selected (4)

9-7. Detail of setting of mode

1) CREV

When combined with KAG05 for the 3-dimensional Y/C separation for movement, the C signal is output as the complement of 2 having the symbol bit of MSB in the "WITH SYMBOL" mode, and a positive number with offset is output in the "WITHOUT SYMBOL" mode.

2) TEST3

Y and C of the 3-dimensional Y/C separation for movement are output to the output of YMX and CMX (when

combined with KAG05) in the "FOR MOVEMENT" mode. Y and C of the 2-dimensional Y/C separation are output in the "Comb filter" mode. If the 2-dimensional Y/C separation is selected, C is output as the C signal having no symbols, regardless of setting of "CREV".

3) SELBP

(1) of the two judging formulae to select the 3-line or BPF (Judging formulae for C correlation (1) and (2)) is selected in "V1-V0" mode, and (2) is selected in "V1+V2" mode.

4) DIP3L

This is used to set the value of A in the judging formulae (1) and (2). "1" is the 8-bit data of LSB, and "8" is that of MSB. Accordingly, the changeover level of the 3-line and BPF can be changed by combining the values of "SELBP" and "DIP3L".

5) SEL3L

The "AND" is taken from the results of the judging formula selected by SELBP and the judging formula (3) so that the BPF can be selected more easily in "BPF" mode. The "OR" is taken so that the 3-line can be selected more easily in the "3-line" mode.

CIRCUIT DESCRIPTION

10. 3-dimensional Y/C Separation Digital Filter : KAG05 (IC10, X35-2110)

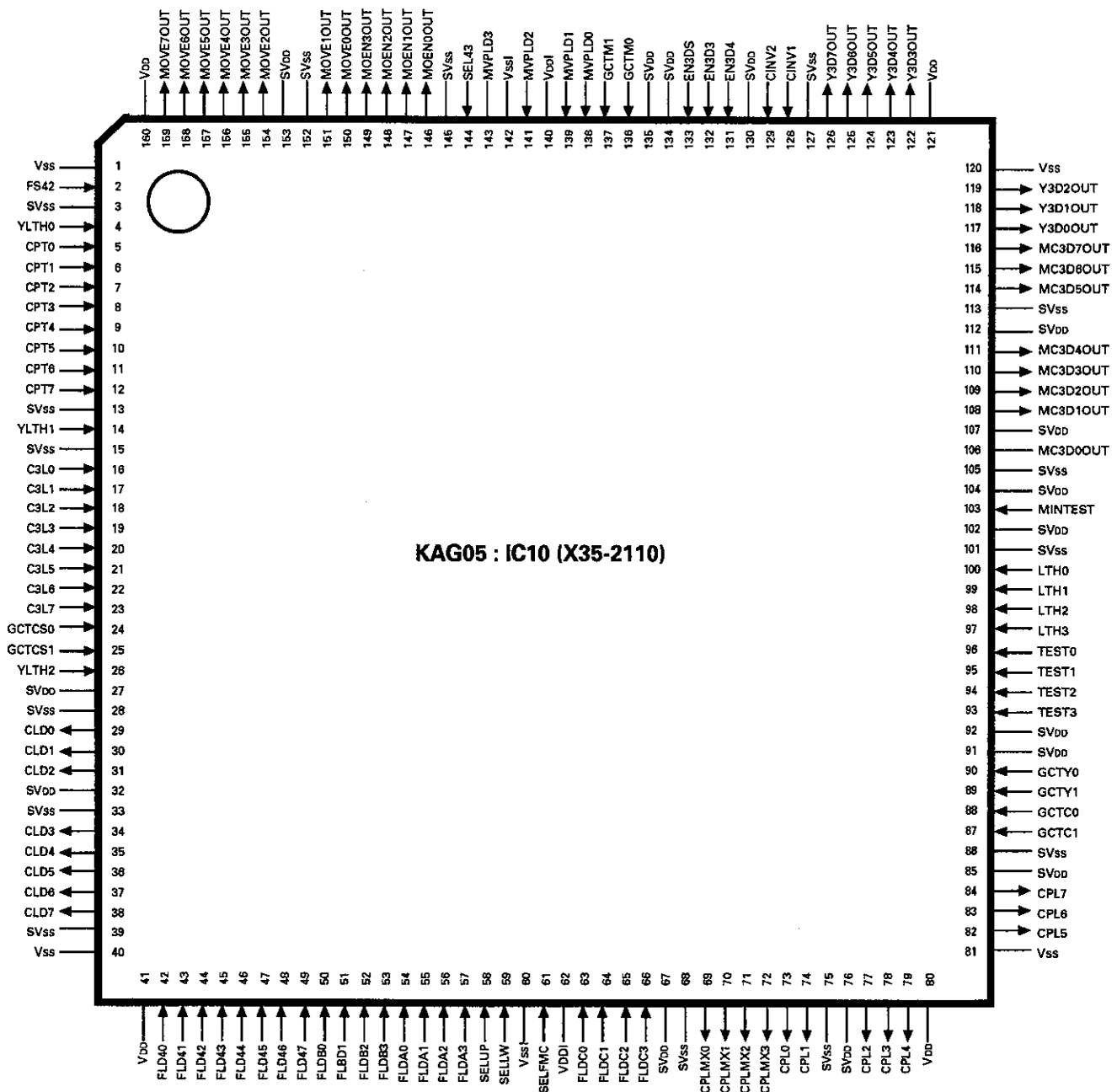
10-1. Outline

KAG05 is a 3-dimensional Y/C separation filter applicable to the NTSC method. If this filter is combined with KAG04, it can execute Y/C separation without making much less dot disturbance and cross color.

10-2. Features

- Detection of movements among frames. 3-dimensional Y/C separation.
- If combined with KAG04, a 3-dimensional Y/C separation for movement filter can be made up.
- Clock of 4fsc and formation by 8bits.
- The movement sensing accuracy can be changed by changing the parameter values.

10-3. Pin connection



CIRCUIT DESCRIPTION

10-4. Pin function

Pin No.	Name	I/O	Function
1	Vss	—	GND
2	FS42	I	Clock input (4fsc=14.31818MHz)
3, 13, 15	SVss	—	GND
4	YLTH0	I	Setting of movement limiter circuit level of low-band elements of brightness (LSB).
5 ~ 12	CPT0 ~ CPT7	I	1H delay composite signal input (CPT0 : LSB, CPT7 : MSB)
14	YLTH1	I	Setting of movement limiter circuit level of low-band elements of brightness.
16 ~ 23	C3L0 ~ C3L7	I	Comb filter Y/C separation chroma signal input (C3L0 : LSB, C3L7 : MSB).
24, 25	GCTCS0, GCTCS1	I	Inter-frame chroma elements movement detecting sensitivity selection. (GCTCS0 : LSB, GCTCS1 : MSB)
26	YLTH2	I	Setting of movement limiter circuit level of low-band elements of brightness.
27, 32	SVdd	—	Power supply
28, 33	SVss	—	GND
29 ~ 31	CLD0 ~ CLD2	O	Chroma mixture output of 3-dimensional Y/C separation for movement (CLD0 : LSB).
34 ~ 38	CLD3 ~ CLD7	O	Chroma mixture output of 3-dimensional Y/C separation for movement (CLD7 : MSB).
39, 40	SVss, Vss	—	GND
41	Vdd	—	Power supply
42 ~ 49	FLD40 ~ FLD47	I	Test pin, fixed to "L".
50 ~ 53	FLDB0 ~ FLDB3	I	Input from outside field memory (2). (FLDB0 : LSB, FLDB3 : MSB)
54 ~ 57	FLDA0 ~ FLDA3	I	Input from outside field memory (1). (FLDA0 : LSB, FLDA3 : MSB)
58	SELUP	I	Changeover signal input for upper 4bits
59	SELLW	I	Changeover signal input for lower 4bits
60	Vssl	—	GND
61	SELFMC	I	Changeover input of input signal of outside field memory (3).
62	Vddl	—	Power supply
63 ~ 66	FLDC0 ~ FLDC3	I	Input from outside field memory (3). (FLDC0 : LSB, FLDC3 : MSB)
67	SVdd	—	Power supply
68	Vss	—	GND
69 ~ 72	CPLMX0 ~ CPLMX3	O	Output to outside field memory (3). (CPLMX0 : LSB, CPLMX3 : MSB)
73, 74	CPL0, CPL1	O	Output to outside field memory (2). (CPL0 : LSB)
75	SVss	—	GND
76	SVdd	—	Power supply
77, 78	CPL2, CPL3	O	Output to outside field memory (2). (CPL3 : MSB)
79	CPL4	O	Output to outside field memory (1). (LSB)
80	Vdd	—	Power supply
81	Vss	—	GND
82 ~ 84	CPL5 ~ CPL7	O	Output to outside field memory (1). (CPL7 : MSB)
85	SVdd	—	Power supply
86	SVss	—	GND
87, 88	GCTC1, GCTC0	I	Brightness and chroma high-band elements movement detecting sensitivity selection.
89, 90	GCTY1, GCTY0	I	Brightness low-band elements movement detecting sensitivity selection.
91, 92	SVdd	—	Power supply
93	TEST3	I	Test pin, fixed to "H".
94	TEST2	I	Forced comb filter control signal input.
95	TEST1	I	Test pin, fixed to "L".
96	TEST0	I	Test pin, fixed to "H".
97 ~ 100	LTH3 ~ LTH0	I	Setting of movement limiter circuit level of chroma elements (LTH3 : LSB, LTH0 : MSB).
101, 105, 113	SVss	—	GND
102, 104	SVdd	—	Power supply
103	MINTEST	I	Test pin, fixed to "L".
106	MC3D0OUT	O	Frame Y/C separation chroma signal output (LSB).
107, 112	SVdd	—	Power supply
108 ~ 111	MC3D1OUT ~ MC3D4OUT	O	Frame Y/C separation chroma signal output
114 ~ 116	MC3D5OUT ~ MC3D7OUT	O	Frame Y/C separation chroma signal output (MC3D7OUT : MSB).
117 ~ 119	Y3D0OUT ~ Y3D2OUT	O	Frame Y/C separation brightness signal output (Y3D0OUT : LSB).
120	Vss	—	GND

CIRCUIT DESCRIPTION

Pin No.	Name	I/O	Function
121	Vdd	–	Power supply
122 ~ 126	Y3D3OUT ~ Y3D7OUT	O	Frame Y/C separation brightness signal output (Y3D7OUT : MSB).
127, 145	SVss	–	GND
128, 129	CINV1, CINV2	I	Test pin (Fixed to "L" : pin 128, "H" : pin 129).
130	SVdd	–	Power supply
131	EN3D4	I	Test pin, fixed to "L".
132	EN3D3	I	Forced comb filter fixed control signal input (FM=3M).
133	EN3DS	I	Test pin, fixed to "H".
134, 135	SVdd	–	Power supply
136, 137	GCTM0, GCTM1	I	Brightness high-band elements movement detecting sensitivity selection (GCTM0 : LSB, GCTM1 : MSB).
138, 139	MVPLD0, MVPLD1	I	Test pin, fixed to "L".
140	Vddl	I	Power supply
141, 143	MVPLD2, MVPLD3	–	Test pin, fixed to "L".
142	Vssl	–	GND
144	SEL43	I	Test pin, fixed to "H".
146 ~ 149	MOEN0OUT ~ MOEN3OUT	O	Test pin (open)
150, 151	MOVE0OUT, MOVE1OUT	O	Test pin (open)
152	SVss	–	GND
153	SVdd	–	Power supply
154 ~ 159	MOVE2OUT ~ MOVE7OUT	O	Test pin (open)
160	Vdd	–	Power supply

- GCTY0, GCTY1 : Brightness low-band elements movement detecting sensitivity selection.
00 → High sensitivity, 01 → ..., 10 → Low sensitivity, 11 → No detection
- YLTH0 ~ YLTH2 : Level setting of brightness low-band elements movement limiter circuit
000 → Maximum, 001 → ..., 110 → , 111 → Minimum
- GCTC0, GCTC1 : Brightness and chroma high-band elements movement detecting sensitivity selection.
00 → High sensitivity, 01 → ..., 10 → Low sensitivity, 11 → No detection
- GCTM0, GCTM1 : Brightness high-band elements movement detecting sensitivity selection.
00 → High sensitivity, 01 → ..., 10 → Low sensitivity, 11 → No detection
- GCTCS0, GCTCS1 : Chroma elements movement detecting sensitivity selection.
00 → High sensitivity, 01 → ..., 10 → Low sensitivity, 11 → No detection
- LTH0 ~ LTH3 : Level setting of chroma elements movement limiter circuit.
0000 → Minimum, 0001 → ..., 1110 → , 1111 → Maximum
- SELFMC : Signal input to change output data for outside field memory (3).
The upper and lower 4bits of 8-bit 1H delay composite signal input from outside are changed over by the control signal SELMHL (SELFMC) sent from KAG03, then output to the outside field memory (3).
0 → Upper 4bits, 1 → Lower 4bits
- SELUP : Signal input to change input data from outside field memories (1) and (3).
The 4-bit data of the field memories (1) and (3) input from outside are changed over by the control signal SEL13 (SELUP) sent from KAG03 and used as the upper 4bits of the 1-frame delay signal.
0 → Field memory (1), 1 → Field memory (3)
- SELLW : Signal input to change input data from outside field memories (2) and (3).
The 4-bit data of the field memories (2) and (3) input from outside are changed over by the control signal SEL23 (SELLW) sent from KAG03 and used as the lower 4bits of the 1-frame delay signal.
0 → Field memory (2), 1 → Field memory (3)
- EN3D3 : The horizontal synchronizing signal part, color burst signal part, and vertical blanking part are processed with the logical comb filter and output by the control signal M3EN3D (EN3D3) sent from KAG03.
- TEST2 : Forced comb filter control signal input The comb filter is forcedly fixed in the search and CAV disc still mode.
0 → Normal, 1 → Forced fixing of comb filter

CIRCUIT DESCRIPTION

10-5. Explanation of functions

1) Outline

• Processing in moving picture system

In the Y/C separation of the moving picture system, since the frames are not deeply correlated with one another, the result processed with the logical comb filter KAG04 is output as it is.

• Processing in still picture system

In the still picture mode, the chroma signals are separated with the frame comb filter by utilizing the fact that the phase of the chroma signal is inverted among the frames.

• Detection of movement

The movement detecting section detects movements of the low-band elements of brightness and the high-band elements of the brightness and chroma in one frame, and outputs the one having a larger absolute value as the movement.

2) Explanation of blocks

• Y/C separation circuit among frames

As 1-frame delay memory, three 1-Mbit field memories are used to form a frame memory. Y/C separation among the frames is executed with the frame comb filter formed with a digitized composite signal and a 1-frame delay signal.

• Brightness low-band elements movement detecting circuit

The difference between the composite signal and 1-frame delay signal is taken and passed through the LPF to limit its band to detect the movement of the low-band elements of brightness.

• Brightness low-band elements movement limiter circuit

Even in the still picture mode, "movement" may be detected because of noises etc. Accordingly, the brightness low-band elements limiter circuit assumes a picture having little movement to be a still picture and masks the movement. The level to judge a picture to be a still picture can be changed with YLTH0 ~ YLTH3.

• Brightness and chroma high-band elements movement detecting circuit

The width of the composite signal and 1-frame delay signal are limited by the BPF which allows the chroma signals to pass, then they are added and subtracted to detect the brightness chroma high-band elements movement. The movement detecting sensitivity of the high-band of the brightness can be changed with GCTM1 and GCTM0, and that of the chroma signals with GCTCS1 and GCTCS0.

• Chroma elements movement limiter circuit

In case of a monochrome video signal which does not contain chroma elements, it is judged that chroma elements do not move at all, and the movement of the chroma elements is masked by the chroma elements movement limiter circuit. The level of monochrome video signal detection is changed with LTH0 ~ LTH3.

• Comparator

The comparator sends the larger one of the detected movement signals of the brightness low-band elements movement detecting circuit and brightness/chroma high-band elements movement detecting circuit to the C mixing circuit. The brightness low-band elements movement detecting sensitivity can be changed with GCTY0 and GCTY1, and the brightness/chroma high-band elements movement detecting sensitivity with GCTC0 and GCTC1.

• C mixing circuit

This circuit calculates the chroma signals of the logical comb filter and frame comb filter, changing their ratio according to the signal from the comparator, then output the result. Then, this chroma signal is sent to the brightness signal separating circuit.

• Brightness signal separating circuit

This circuit subtracts the chroma signal sent from the C mixing circuit from the original composite signal, then outputs the brightness signal.

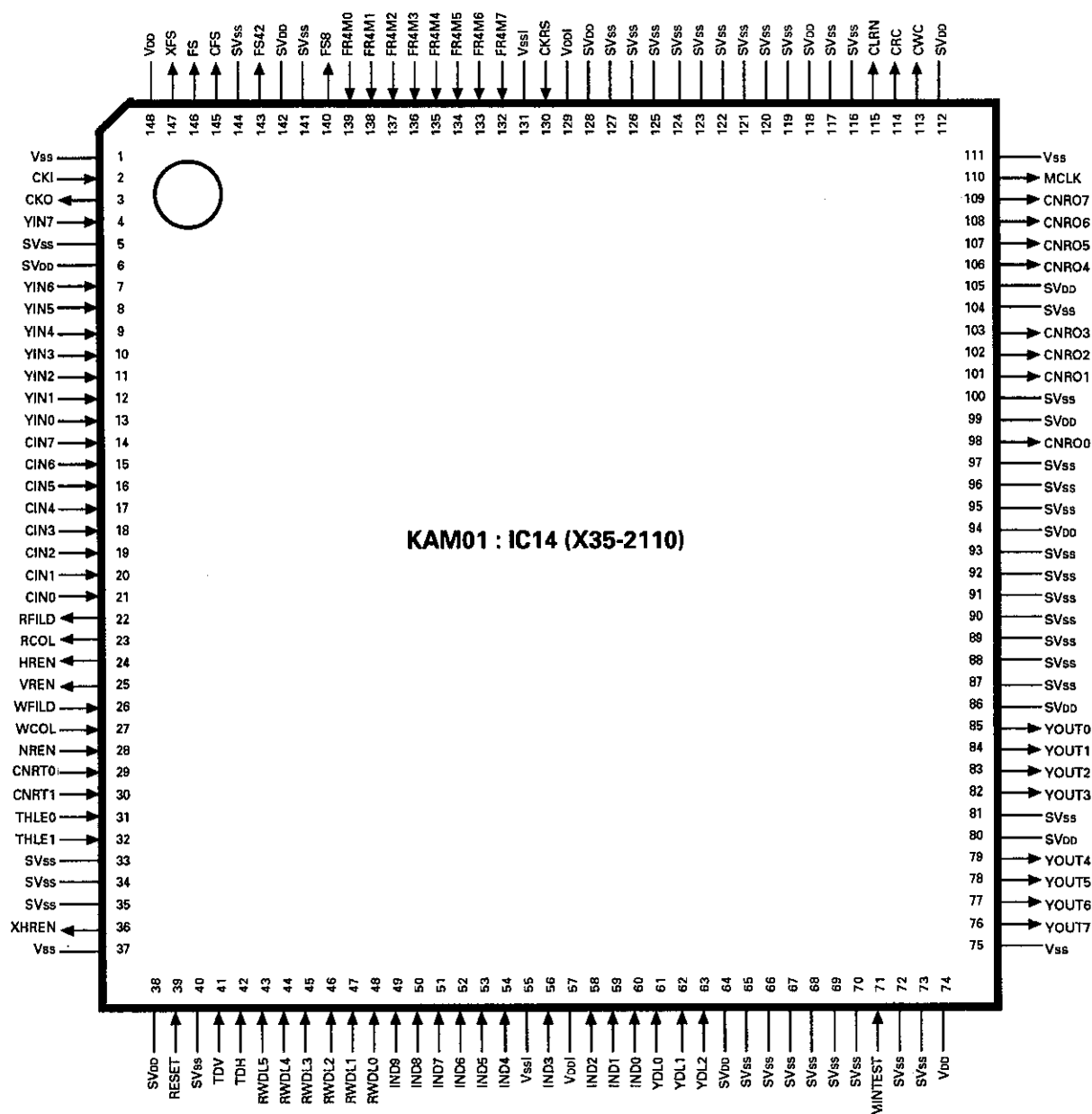
11-1. Outline

KAM01 is a color noise reduction element for NTSC, which reduces the phase noise and amplifies the color signals.

11-2, Features

- Frame cyclic filter.
- Reference signal generator.
- Clock of 8fsc and formation by 8bits.
- Built-in LPF for Y.

11-3. Pin connection



CIRCUIT DESCRIPTION

11-4. Pin function

Pin No.	Name	I/O	Function
1	Vss	–	GND
2	CKI	I	8fsc clock input
3	CKO	O	8fsc clock output
4	YIN7	I	Y input (MSB)
5	SVss	–	GND
6	SVdd	I	Power supply
7 ~ 13	YIN6 ~ YIN0	I	Y input (YIN0 : LSB)
14 ~ 21	CIN7 ~ CIN0	I	C input (CIN7 : MSB, CIN0 : LSB)
22	RFILD	O	Reference field output
23	RCOL	O	Reference color output
24	HREN	O	Reference 1H pulse
25	VREN	O	Reference field pulse
26	WFILD	I	Writing field input
27	WCOL	I	Writing color input
28	NREN	I	Noise reduction ON/OFF selecting
29, 30	CNRT0, CNRT1	I	Coefficient control of cyclic filter for movements among frames.
31, 32	THLE0, THLE1	I	Fine adjustment of CNRT0 and CNRT1.
33 ~ 35	SVss	–	GND
36	XHREN	O	Reference 1H pulse (Inverted output of HREN)
37	Vss	–	GND
38	SVdd	I	Power supply
39	RESET	I	Chip select
40	SVss	–	GND
41	TDV	I	Frame counter offset data pulse (For test). Fixed to "H".
42	TDH	I	1H counter offset data pulse (For test). Fixed to "H".
43 ~ 48	RWDL5 ~ RWDL0	I	Frame memory R/W phase adjustment. Fixed to 011011bin.
49 ~ 54	IND9 ~ IND4	I	1H/frame counter offset data. Fixed to 375hex (IND9 : MSB).
55	Vssl	–	GND
56	IND3	I	1H/frame counter offset data
57	VddI	I	Power supply
58 ~ 60	IND2 ~ IND0	I	1H/frame counter offset data (IND0 : LSB).
61 ~ 63	YDL0 ~ YDL2	I	Y output delay adjustment
64	SVdd	I	Power supply
65 ~ 70	SVss	–	GND
71	MINTEST	I	Test pin (fixed to "L").
72, 73	SVss	–	GND
74	Vdd	I	Power supply
75	Vss	–	GND
76 ~ 79	YOUT7 ~ YOUT4	O	Y output (YOUT7 : MSB).
80	SVdd	I	Power supply
81	SVss	–	GND

CIRCUIT DESCRIPTION

Pin No.	Name	I/O	Function
82 ~ 85	YOUT3 ~ YOUT0	O	Y output (YOUT0 : LSB).
86	SVDD	I	Power supply
87 ~ 93	SVSS	—	GND
94, 99	SVDD	I	Power supply
95 ~ 97	SVSS	—	GND
98	CNRO0	O	C output (LSB).
100, 104	SVSS	—	GND
101 ~ 103	CNRO1 ~ CNRO3	O	C output
105	SVDD	I	Power supply
106 ~ 109	CNRO4 ~ CNRO7	O	C output (CNRO7 : MSB).
110	MCLK	O	Frame memory clock
111	VSS	—	GND
112, 118	SVDD	I	Power supply
113	CWC	O	Frame memory writing clock
114	CRC	O	Frame memory reading clock
115	CLRN	O	Frame memory clear
116, 117, 119 ~ 127	SVSS	—	GND
128	SVDD	I	Power supply
129	VDDI	I	Power supply
130	CKRS	I	CNR ON/OFF change ("L" : ON, "H" : OFF)
131	VSSI	I	GND
132 ~ 139	FR4M7 ~ FR4M0	I	1 frame delay input (FR4M7 : MSB, FR4M0 : LSB)
140	FS8	O	8fsc output
141, 144	SVSS	—	GND
142	SVDD	I	Power supply
143	FS42	O	4fsc output
145	CFS	O	8/3fsc output
146	FS	O	8fsc output (Same phase as FS8)
147	XFS	O	Inverted output of FS
148	VDD	I	Power supply

11-5. Explanation of functions

1) Frame cyclic CNR

The C signal sampled at 4fsc is converted into an 8fsc signal by the interpolation LPF. This converted signal is thinned to 1/3 by the 8/3fsc clock, then input to the cyclic filter. The noise suppressing ratio R is determined by the depth of frame correlation.

$$R = \log [(1+K) / (1-K)] \text{ dB}$$

The C signal which underwent the noise reduction processing is input to KAN01 (BPF for C) to remove the folded noises. The capacity of the frame memory for frame correlation must be at least 2M bit.

2) Reference signal generator

This device generates the information on 1H, 262H, 263H, field, and color according to the counter of 1 frame to interface with TBC. Since the H synchronizing period and V synchronizing period are not processed by the CNR, the frame counter generates a prohibition gate.

3) YLPF

The Y signal sampled at 4fsc is over-sampled by the interpolation LPF and converted into an 8fsc signal, then output.

11-6. Details of setting of modes

1) Setting of NR effect : CNRT0, CNRT1, THLE0, THLE1

THLE0 and THLE1 are for fine adjustment. Their NR effect is large when L and L, and small when H and H.

CNRT0	CNRT1	NR effect	Residual image
H	L	Small	Small
L	H	Medium	Medium
H	H	Large	Large
L	L	No	No

CIRCUIT DESCRIPTION

12. BPF for Color Signals : KAN01 (IC17, X35-2110)

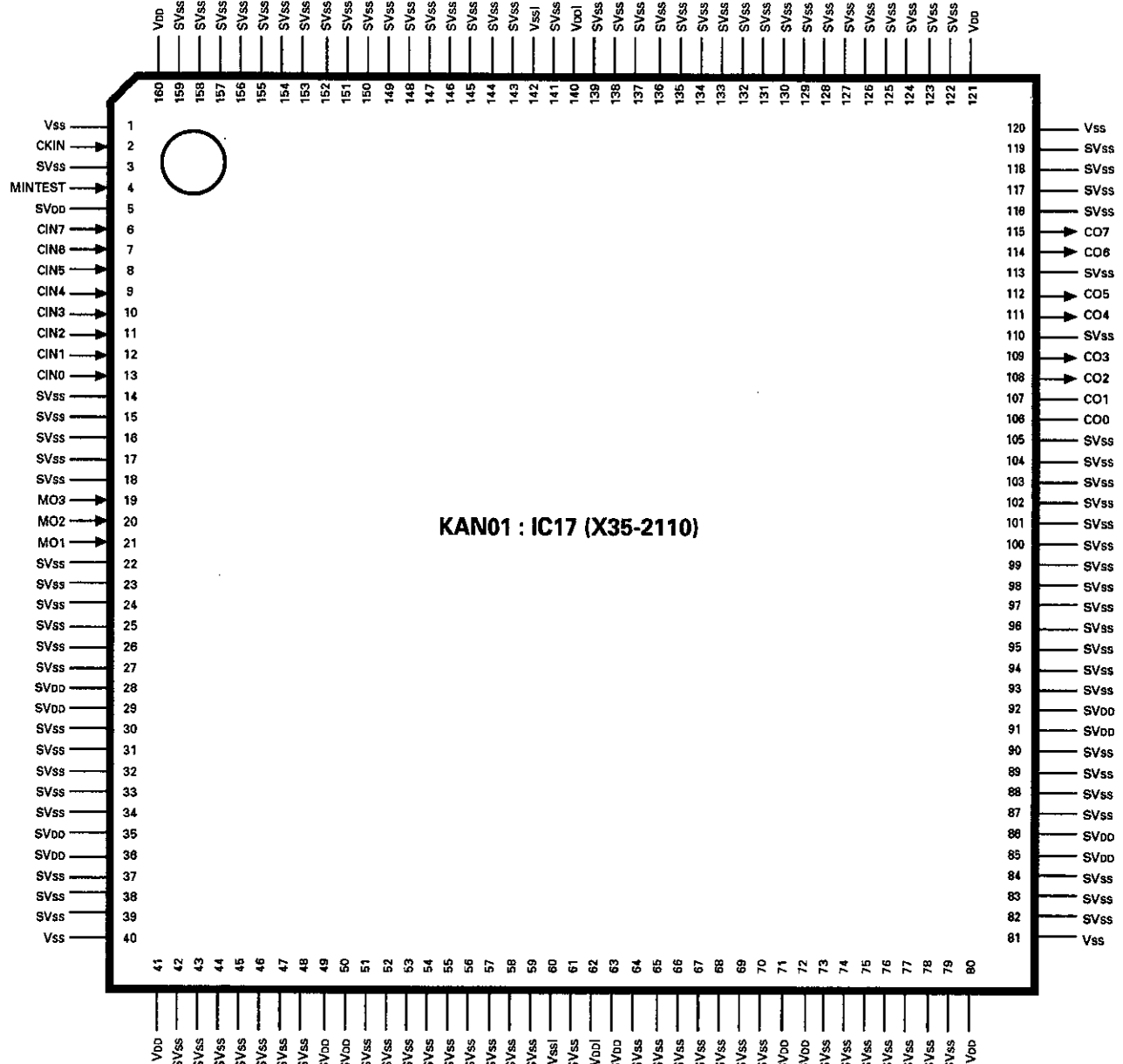
12-1. Outline

KAN01 is a band pass filter for the color signals, which extracts the frequency elements of 3.58MHz.

12-2. Features

Clock of 8fsc and formation by 8-bits.

12-3. Pin connection



CIRCUIT DESCRIPTION

12-4. Pin function

Pin No.	Name	I/O	Function
1	Vss	–	GND
2	CKIN	I	8fsc clock input
3	SVss	–	GND
4	MINTEST	I	Test pin
5	SVDD	I	Power supply
6 ~ 13	CIN7 ~ CIN0	I	C input (CIN7 : MSB, CIN0 : LSB)
14 ~ 18	SVss	–	GND
19 ~ 21	MO3 ~ MO1	I	Test pin MO3 : Fixed to "H" MO2, MO1 : Fixed to "L"
22 ~ 27	SVss	–	GND
28, 29	SVDD	I	Power supply
30 ~ 34	SVss	–	GND
35, 36	SVDD	I	Power supply
37 ~ 39	SVss	–	GND
40	Vss	–	GND
41	VDD	I	Power supply
42 ~ 48	SVss	–	GND
49, 50	SVDD	I	Power supply
51 ~ 59	SVss	–	GND
60	Vssl	I	GND
61	SVss	–	GND
62	VDDI	I	Power supply
63	SVDD	I	Power supply

Pin No.	Name	I/O	Function
64 ~ 70	SVss	–	GND
71, 72	SVDD	I	Power supply
73 ~ 79	SVss	–	GND
80	VDD	I	Power supply
81	Vss	–	GND
82 ~ 84	SVss	–	GND
85, 86	SVDD	I	Power supply
87 ~ 90	SVss	–	GND
91, 92	SVDD	I	Power supply
93 ~ 105	SVss	–	GND
106 ~ 109	CO0 ~ CO3	O	C output (CO0 : LSB)
110	SVss	–	GND
111, 112	CO4, CO5	O	C output
113	SVss	–	GND
114, 115	CO6, CO7	O	C output (CO7 : MSB)
116 ~ 119	SVss	–	GND
120	Vss	–	GND
121	VDD	I	Power supply
122 ~ 139	SVss	–	GND
140	VDDI	I	Power supply
141	SVss	–	GND
142	Vssl	I	GND
143 ~ 159	SVss	–	GND
160	VDD	I	Power supply

12-5. Explanations of functions

1) BPF for color signal

The color signal sampled at 4fsc is over-sampled by the BPF for interpolation, then converted into 8-fsc data.

CIRCUIT DESCRIPTION

13. 20-bit Input Bit-stream Conversion DAC : SAA7350 (IC11, X32-2350)

13-1. Functional description

General

The SAA7350 bit-stream conversion CMOS DAC contains a flexible interface supporting a variety of formats. This enables it to be used with a number of available digital filters with wordlengths of up to 20-bits and up-sampling up to 8fs.

The system sampling frequency (fs) can be between 16kHz and 53kHz.

The analog section contains four one-bit DACs operated in differential mode to achieve high performance signal-to-noise ratio, channel separation and total harmonic distortion.

Input interface

The SAA7350 supports the following modes :

- I²S with dataword rates of fs, 2fs or 4fs with wordlengths of up to 20-bits. A minimum of 16-bit-clock cycles per word is required.
- Sony serial format for dataword rate of fs, 2fs, or 4fs with wordlengths of 16, 18 or 20-bits. As this format idles on the MSB it is necessary to know how many bits are being transmitted.
- Simultaneous mode for dataword rates of fs, 2fs, 4fs or 8fs with wordlengths of up to 20-bits idling on the least significant bit. A minimum of 16-bit-clock cycles per word is required.
- Simultaneous mode for dataword rates of fs, 2fs, 4fs and 8fs with wordlengths of 18 or 20-bits idling on the MSB. As this format idles on the MSB it is necessary to know how many bits are being transmitted.
- Simultaneous mode for dataword rates of fs, 2fs, 4fs or 8fs with wordlengths of up to 20-bits using-burst clocks (see next page). A minimum of 16-bits-clock cycles is required. This mode is restricted to having the bit clock at less than or equal to half the master clock frequency supplied to the SAA7350.

The choice of these formats is given by the pins IDF1 to IDF3 as shown below.

13-2. Input data formats

IDF3	IDF2	IDF1	format
0	0	0	I ² S format up to 20-bits
0	0	1	Sony serial format 16-bits
0	1	0	Sony serial format 18-bits
0	1	1	Sony serial format 20-bits
1	0	0	Simultaneous format idling on LSB up to 20-bits
1	0	1	Simultaneous format idling on MSB 18-bits
1	1	0	Simultaneous format idling on MSB 20-bits
1	1	1	Simultaneous format burst clock up to 20-bits

The transfer on the serial input has to be synchronous to the master clock.

Clock frequency

The device can run at an input clock frequency of either 384fs or 256fs (pin XSEL) outputting a system clock at the same frequency on XSYS1 and half input clock frequency on XSY2. fs can be between 16kHz and 53kHz.

Noise shaping

Third order noise shaping is implemented on the SAA7350 to give an improved signal-to-noise ratio. DC offset and out-of-band dither is added to prevent idle patterns in the audio band.

Bit-stream conversion DAC

The digital-to-analog conversion in the SAA7350 is performed using the Philips bit-stream conversion technique. The input from the digital filter is over-sampled to 8fs by means of a digital sample and hold and converted to a 1-bit pulse density modulated (PDM) signal.

A switched capacitor technique is used for the bit-stream conversion to convert the PDM signal to an analog signal. A fixed charge is either added or subtracted from the virtual earth node of an integrator. As this output is a continuous time output a highly symmetrical operational amplifier is used to give a low distortion figure.

In order to increase the output signal-to-noise ratio and THD performance, internal operational-amplifiers are provided so that the device is operated in differential mode. With this technique, any common mode signals cancel thus improving the signal-to-noise ratio and total harmonic distortion.

TDA1547 interface

The SAA7350 can also be used to provide over-sampling and noise shaping for the TDA1547. One-bit codes and clock outputs are supplied for inputs to the TDA1547.

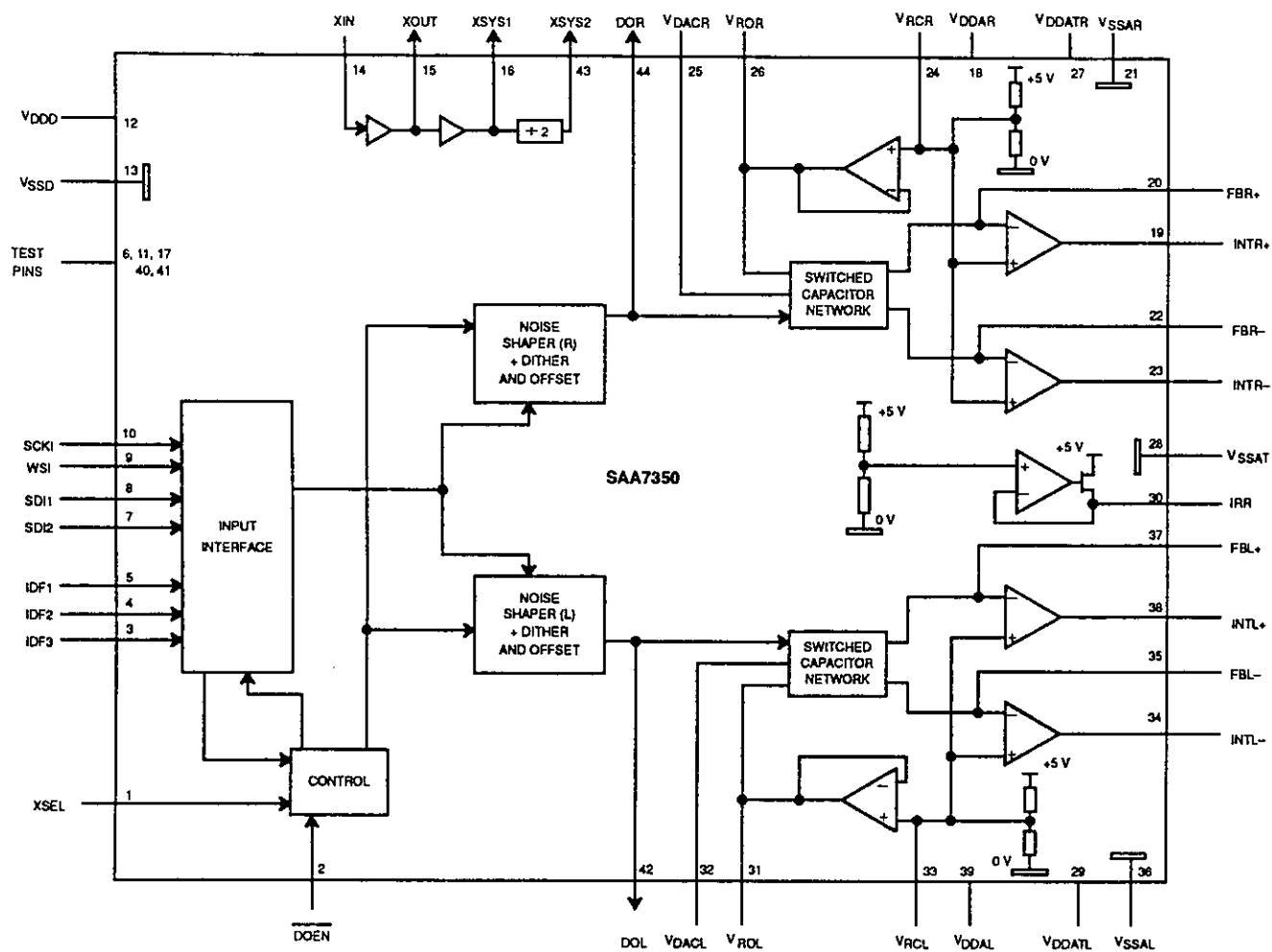
CIRCUIT DESCRIPTION

13-3. Pin function

Pin	Symbol	I/O	Description
1	XSEL	I	Crystal frequency select; this pin is used to select the master crystal frequency as follows : XSEL HIGH =384fs, XSEL LOW=256fs; if unconnected the pin will default HIGH
2	DOEN	I	One-bit digital output enable; when LOW, the one-bit code outputs are made available for TDA1547; if unconnected the pin will default HIGH (not connected)
3~5	IDF3~IDF1	I	Input data format; these three pins determine the input format the device is to operate in (see functional description); if unconnected these pins will default HIGH (i. e. burst clock mode)
6	TEST4	–	Test 4; this pin should be connected GND line
7	SDI2	I	Serial data input; used in simultaneous mode only (for the right channel signal)
8	SDI1	I	Serial data input; this should be a 16, 18 or 20-bit linear 2's complement PCM signal; in simultaneous mode this pin is used for the left channel signal
9	WSI	I	Serial input word select signal; signifies whether data word is for the left or right channel; can be either fs, 2fs, 4fs or 8fs where fs is the system sampling frequency; fs can be between 16kHz and 53kHz
10	SCKI	I	Bit clock input for the serial input interface
11	TEST1	–	Test 1; this pin should be left open-circuit
12	VDDD	–	+5V power supply for the digital section
13	VSSD	–	Ground connection for the digital section
14	XIN	I	Crystal oscillator input
15	XOUT	O	Crystal oscillator output
16	XSYS1	O	Buffered oscillator output
17	TEST5	–	Test 5; in normal operation this pin should be tied LOW
18	VDDAR	–	Connected to ground
19	INTR+	O	Output from the right positive switched-capacitor integrator; input to differential operational amplifier (Connected to ground)
20	FBR+	–	Feedback connection for the right positive switched-capacitor integrator (Connected to ground)
21	VSSAR	–	0V supply for right channel (Connected to ground)
22	FBR–	–	Feedback connection for the right negative switched-capacitor integrator (Connected to ground)
23	INTR–	O	Output from the right negative switched-capacitor integrator; input to differential operational amplifier (Connected to ground)
24	VRCR	–	High impedance voltage reference for right channel inputs; typically VDDAR/2 (Connected to ground)
25	VDACR	–	Reference voltage supply for right channel DAC's; normally this will be connected to Vss (Connected to ground)
26	VROR	O	Right channel voltage reference output; typically VDDAR/2 (Connected to ground)
27	VDDATR	–	5V supply for right channel analog timing (Connected to ground)
28	VSSAT	–	0V supply for left and right channel analog timing (Connected to ground)
29	VDDATL	–	5V supply for left channel analog timing (Connected to ground)
30	IRR	–	24kΩ bias resistor connection for the reference current generator circuit (Connected to ground)
31	VROL	O	Left channel voltage reference output; typically VDDAL/2 (Connected to ground)
32	VDACL	–	Reference voltage supply for left channel DAC; normally this will be connected to Vss (Connected to ground)
33	VRCL	–	High impedance voltage reference for left channel inputs and for bias current generator; typically VDDAL/2 (Connected to ground)
34	INTL–	O	Output from the left negative switched-capacitor integrator; input to differential operational-amplifier (Connected to ground)
35	FBL–	–	Feedback connection for the left negative switched-capacitor integrator (Connected to ground)
36	VSSAL	–	0V supply for left channel (Connected to ground)
37	FBL+	–	Feedback connection for the left positive switched-capacitor integrator (Connected to ground)
38	INTL+	O	Output from the left positive switched-capacitor integrator; input to differential operational-amplifier (Connected to ground)
39	VDDAL	–	Analog 5V supply for left channel (Connected to ground)
40	TEST2	–	Test 2; this pin should be left open-circuit
41	TEST3	–	Test 3; this pin should be left open-circuit
42	DOL	O	Digital output left; left channel one-bit code for TDA1547
43	XSYS2	O	Output clock at a frequency of half the master clock frequency
44	DOR	O	Digital output right; right channel one-bit code for TDA1547

CIRCUIT DESCRIPTION

13-4. Block diagram



CIRCUIT DESCRIPTION

14. Bit-stream DAC (1-bit) : TDA1547 (IC12, X32-2350)

14-1. General description

The TDA1547 is a dedicated one-bit digital-to-analog converter to facilitate a high fidelity sound reproduction of digital audio. The TDA1547 is extremely suitable for use in high quality audio systems such as Compact Disc and DAT players, or in digital amplifiers and digital signal processing systems.

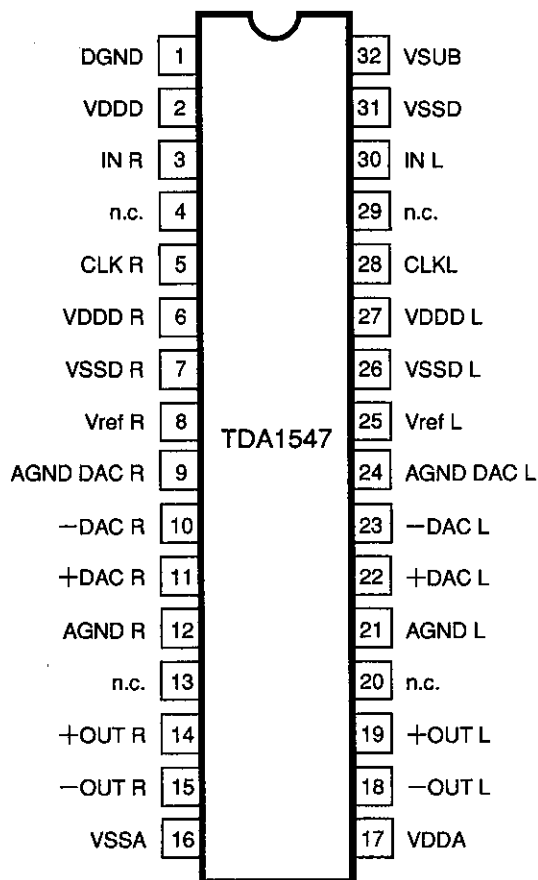
The TDA1547 is used in combination with the SAA7350 bitstream circuit, which includes the third-order noise shaper. The excellent performance of the SAA7350 and TDA1547 bitstream conversion system is obtained by separating the noise shaping circuit and the one-bit conversion circuit over two IC's thereby

reducing the crosstalk between the digital and analog parts.

The TDA1547 one-bit converter is processed in BIMOS. In the digital logic and drivers bipolar transistors are used to optimize speed and to reduce digital noise generation. In the analog part the bipolar transistors are used to obtain high performance of the operational amplifiers. Special layout precautions have been taken to achieve a high crosstalk immunity.

The layout of the TDA1547 has fully separated left and right channels and supply voltage lines between the digital and analog sections.

14-2. Pin connection



CIRCUIT DESCRIPTION

14-3. Pin functions

Pin	Symbol	I/O	Description
1	DGND	–	0V digital supply.
2	VDDD	–	5V digital supply for both channels.
3	IN R	I	Serial one-bit data input for the right channel.
4	n.c.	–	Pin not connected; should preferably be connected to digital ground.
5	CLK R	I	Clock input for the right channel.
6	VDDD R	–	5V digital supply for the right channel; this voltage determines the internal logic HIGH level in the right channel.
7	VSSD R	–	–3.5V digital supply for the right channel; this voltage determines the internal logic LOW level in the right channel.
8	VREF R	–	–4V reference voltage for the right channel switched capacitor DAC.
9	AGND DAC R	–	0V reference voltage for the right channel switched capacitor DAC; this pin should be connected to analog ground.
10	–DAC R	O	Output from the right negative switched capacitor DAC; feedback connection for the right negative operational amplifier.
11	+DAC R	O	Output from the right positive switched capacitor DAC; feedback connection for the right positive operational amplifier.
12	AGND R	–	0V reference voltage for both right channel operational amplifiers.
13	n.c.	–	Pin not connected; should preferably be connected to analog ground.
14	+OUT R	O	+ output of the switched capacitor operational amplifier.
15	–OUT R	O	– output of the switched capacitor operational amplifier.
16	VSSA	–	–5V analog supply.
17	VDDA	–	5V analog supply.
18	–OUT L	O	– output of the switched capacitor operational amplifier.
19	+OUT L	O	+ output of the switched capacitor operational amplifier.
20	n.c.	–	Pin not connected; should preferably be connected to analog ground.
21	AGND L	–	0V reference voltage for both left channel operational amplifiers.
22	+DAC L	O	Output from the left positive switched capacitor DAC; feedback connection for the left positive operational amplifier.
23	–DAC L	O	Output from the left negative switched capacitor DAC; feedback connection for the left negative operational amplifier.
24	AGND DAC L	–	0V reference voltage for the left channel switched capacitor DAC; this pin should be connected to analog ground.
25	VREF L	–	–4V reference voltage for the left channel switched capacitor DAC.
26	VSSD L	–	–3.5V digital supply for the left channel; this voltage determines the internal logic LOW level in the left channel.
27	VDDD L	–	5V digital supply for the left channel; this voltage determines the internal logic HIGH level in the left channel.
28	CLK L	I	Clock input for the left channel.
29	n.c.	–	Pin not connected; should preferably be connected to digital ground.
30	IN L	I	Serial one-bit data input for the left channel.
31	VSSD	–	–5V digital supply for both channels.
32	VSUB	–	–5V substrate voltage.

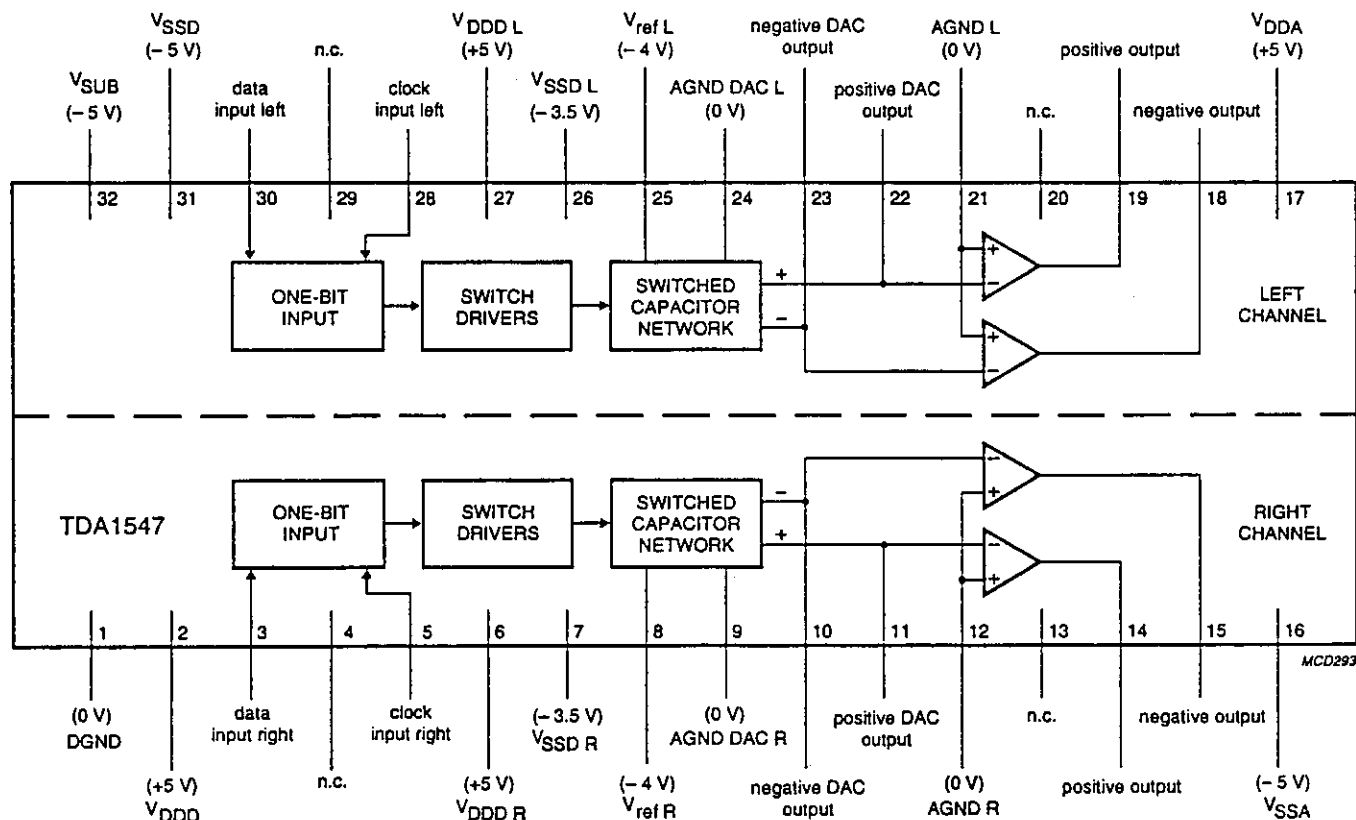
14-4. Function description

Both channels are completely separated to reach the desired high crosstalk suppression level. Each channel consists of the following functional parts :

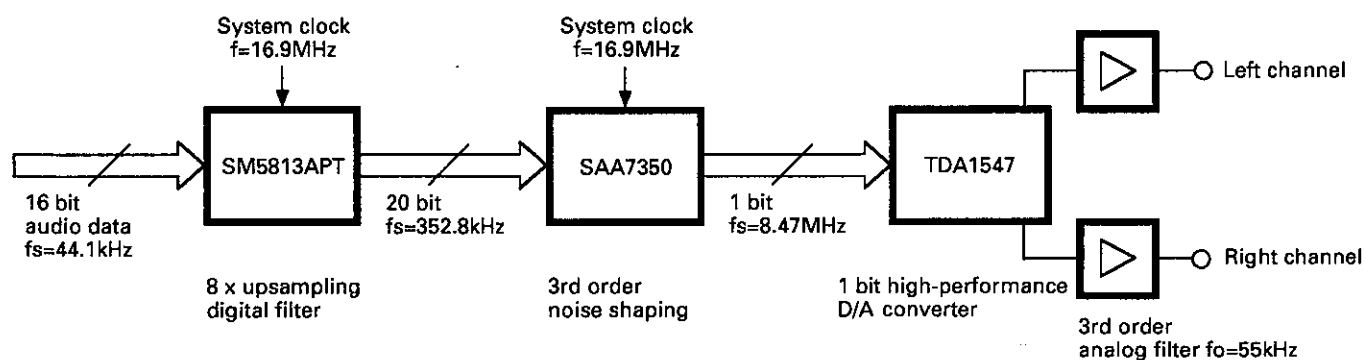
- One-bit input, which latches the incoming data to the system clock.
- Switch driver circuit, which generates the non-overlapping clock- and data-signals that control the DAC switched capacitor networks.
- Switched capacitor network, this forms the actual DAC function, it supplies charge packets to the low-pass filter, under control of the incoming one-bit code.
- Two high performance operational amplifiers, that perform the charge packet to voltage conversion and deliver a differential output signal. The first pole of the low-pass filter is built around them.

CIRCUIT DESCRIPTION

14-5. Block diagram

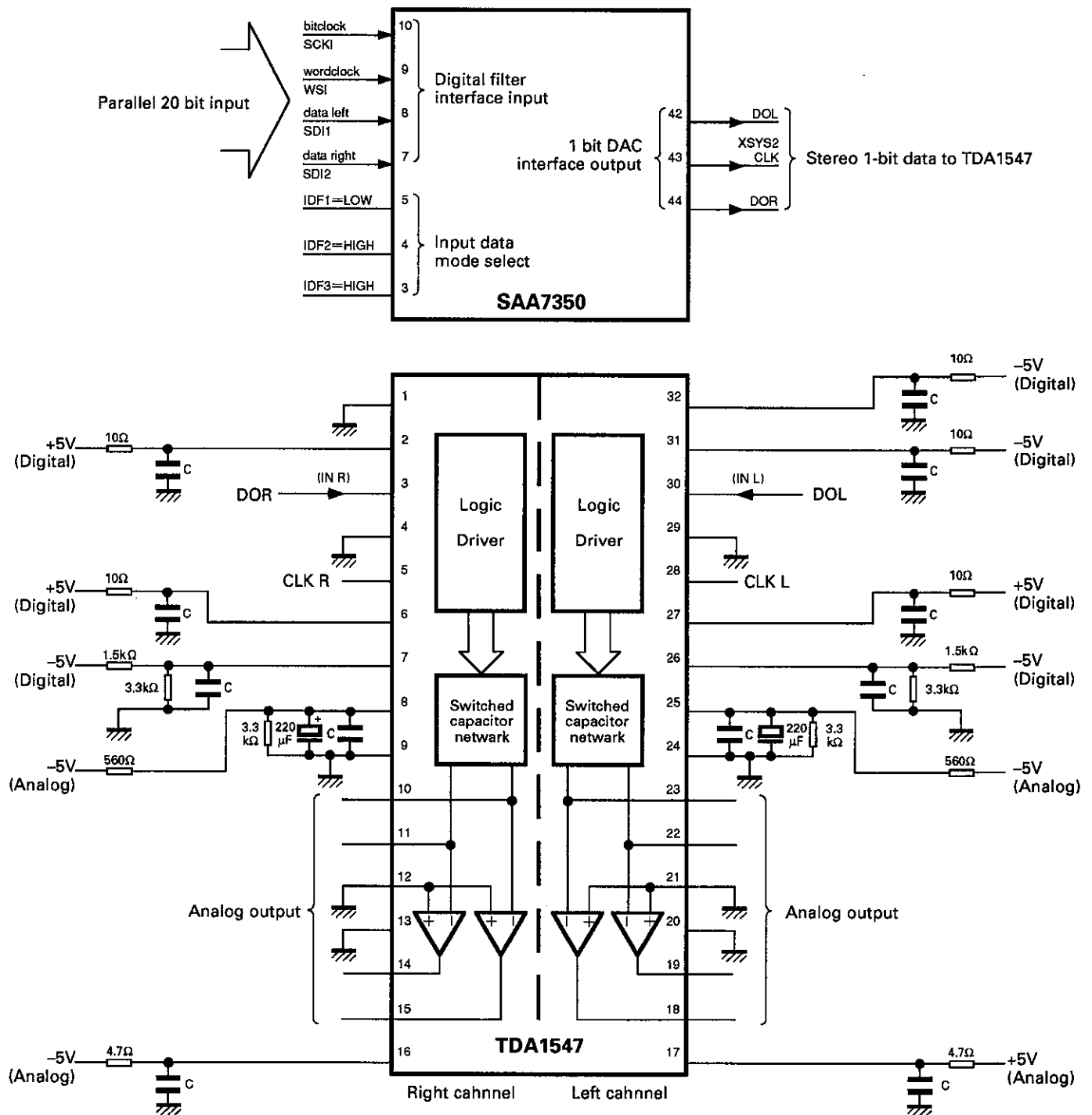


14-6. CD-range bit-stream system (192fs over-sampling)



CIRCUIT DESCRIPTION

14-7. Application diagram



C = 100 nF (chip capacitor)

CIRCUIT DESCRIPTION

15. Accurate LD Reference Master Clock Operation

15-1. Outline

When a digital sound LD is replayed with a conventional system, the master clock of VCXO is used for demodulation of the digital sound data. Since the clock of VCXO contains jitter elements larger than a fixed crystal oscillator, the sound quality of LD is lower than that of CD.

In LVD-Z1, however, a fixed quartz oscillator is used to replay a digital sound LD. By this method, the digital sound of LD which has been assumed to be lower than CD is heightened to the same level as CD.

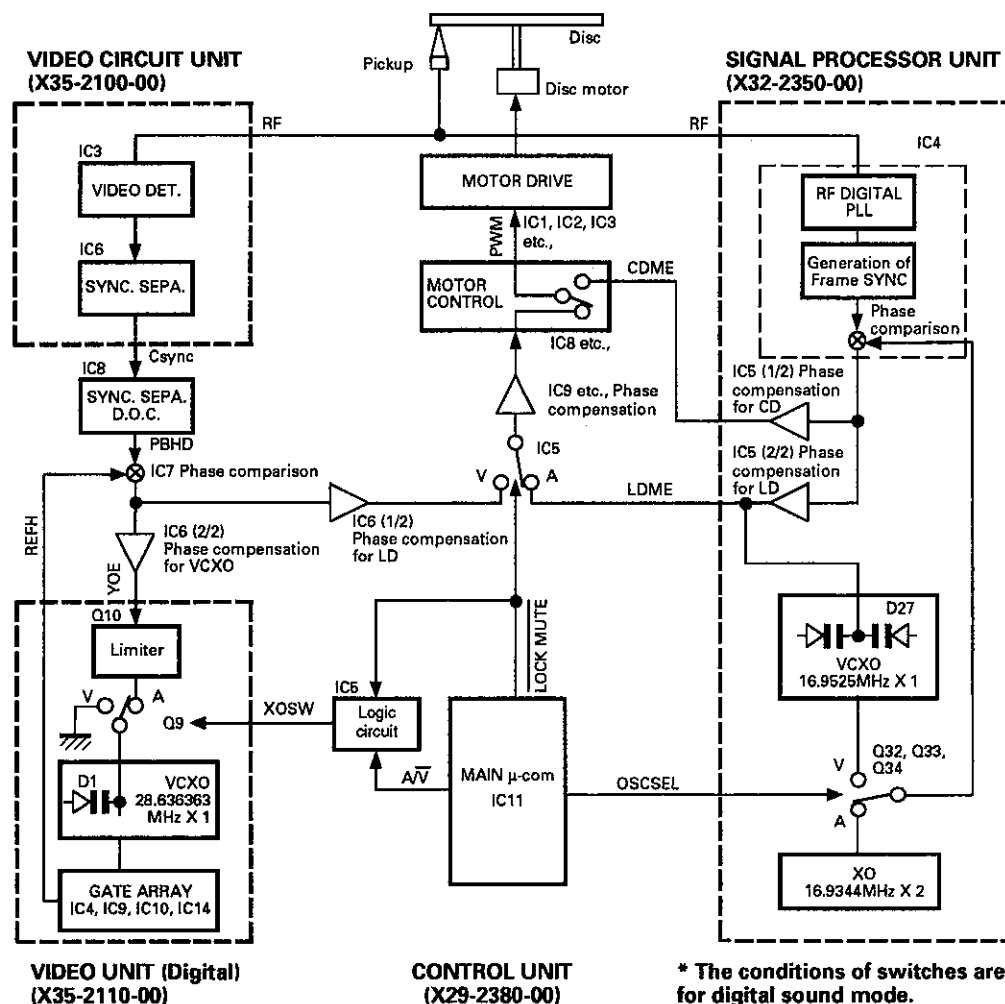
15-2. Explanation of functions

The disc servo of the LD player is so controlled that it will be synchronized with the reference clock for replay of video (14.31818MHz). The frequency of the digital sound of LD has been slightly shifted when played to synchronize the reference clock of CD (16.9344MHz) with that of the video signals (VCXO).

Accordingly, jitters which cannot be eliminated by the disc servo have shaken the reference clock of the sound, and that has caused lowering of sound quality of LD, frequency shift of OPTICAL OUTPUT (Digital out), etc.

To solve this problem, the disc servo of LVD-Z1 is so designed that the digital sound LD will synchronize with the reference clock of CD. Consequently, the reference clock for playing the video in the video system is changed to VCXO, which changes the reference clock for playing the video. Since the video system has a strong TBC (Time Base Collector) circuit, the jitters are removed and the images are little affected by the residual jitters. Furthermore, a limiter circuit is installed so that the frequency of the video signals will not be extremely shifted.

If the disc servo is controlled with digital sounds, the servo band cannot be set so widely as in CD. Accordingly, the RF PLL of the sound system cannot follow up and the loop cannot be closed in the search operation etc. The servo is locked with the digital sounds only in the play mode (Changed to the control of start of play and reference clock for playing the video). If the disc servo control is changed in the search mode, shock noises are added to the sound, thus it is not changed in the search mode.



CIRCUIT DESCRIPTION

15-3. Circuit configuration

The circuit consists of four units as shown in the previous section. The signal processor unit (X32-) has two independent circuits of a fixed quartz oscillator and a VCXO for higher sound quality, each of which is selected properly. The reference oscillation of the video unit (Digital: X35-2110) is set by changing the error voltage applied to the variable capacitance diode of VCXO.

The LOCK MUTE signal of the main μ -com becomes "H" only when a digital sound LD disc is played, and becomes "L" in any other mode (It becomes "L" in the V LOCK MODE, however.). The OSCSEL signal becomes "H" when a CD or a digital sound LD is played, and the fixed quartz oscillation circuit is used for oscillation of the signal processor unit (X32-). (The OSCSEL signal becomes "L" in another mode and the oscillation of VCXO is used). The OSCSEL signal does not change in the search mode.

Although the XOSW signal is synchronized with the LOCK MUTE signal, it becomes "H" and the fixed oscillator is used when the A/V signal is at "H" (CD). Accordingly, the frequency of the superimpose IC is generated by the fixed oscillation.

15-4. Change of master clock

The relationship between the video signal recording frequency and sound signal recording frequency of LD's of some types are out of the standard.

If one of these LD's is played, the frequency of the video signal output is out of the standard and the im-

ages in the television may be disordered. In this special case, the disc servo of LVD-Z1 can be changed to the conventional one with keys (V LOCK MODE).

The conventional disc servo can be selected by pushing the three keys of STOP, $\ll$, and $\gg$ at the same time after the disc is set (If the tray is opened, the VLOCK mode is reset).

16. VCO Error Voltage Changeover Circuit (X35-2100)

Unlike a conventional model, the TBC of LVD-Z1 is operated by only the error voltage of the burst system while an LD is played. In the search mode, however, the TBC must be operated with the H system since the operation cannot be locked with the burst system (Shown in Fig. 1).

- PBHD $\rightarrow$ Horizontal synchronizing signal of play system
- BSHD $\rightarrow$ Horizontal synchronizing signal of TBC system

The LOCK1 and LOCK2 signals are used to output the phase difference between PBHD and BSHD as shown in Fig. 2. The phase difference between PBHD and BSHD is detected by IC16 and IC17 as shown in Fig. 1. While PBHD and BSHD are near $\bar{Q}$ of IC16, "H" is output and the burst system is selected for the VCO voltage.

If PBHD and BSHD are separated (TBC is unlocked), "L" is output to $\bar{Q}$ of IC16 and the H system is selected for the VCO control voltage. The H system error detecting circuit is shown in Fig. 3.

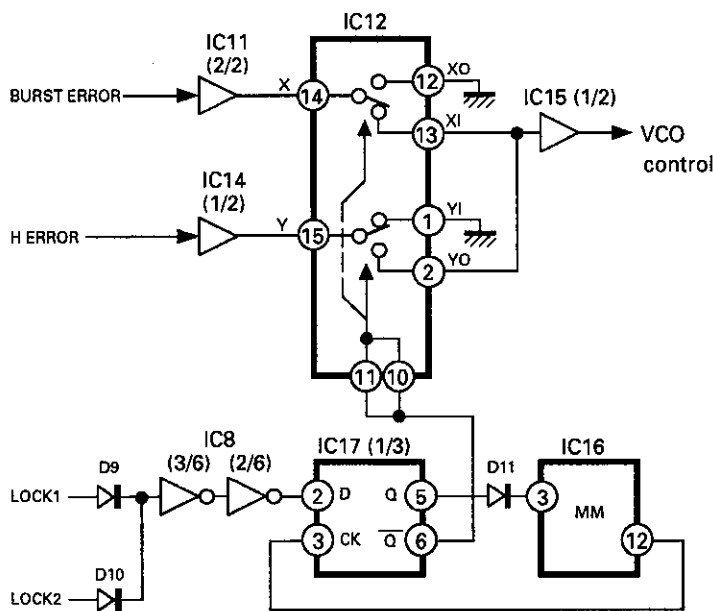


Fig.1

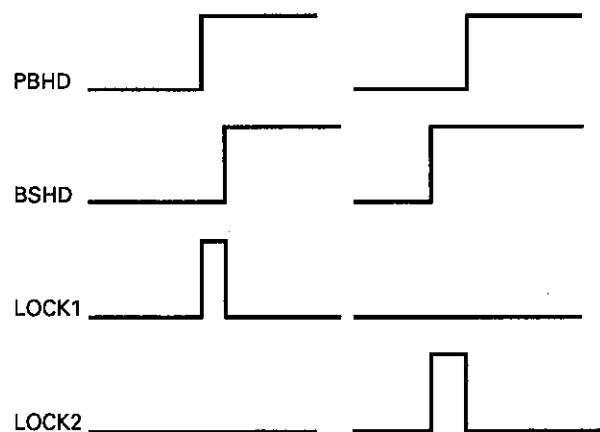


Fig. 2

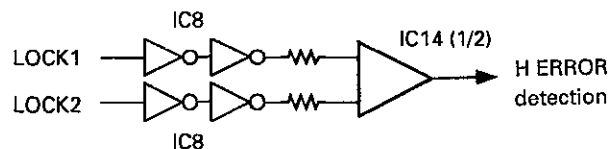


Fig. 3

CIRCUIT DESCRIPTION

17. Burst Detecting Circuit (X35-2100)

17-1. Outline

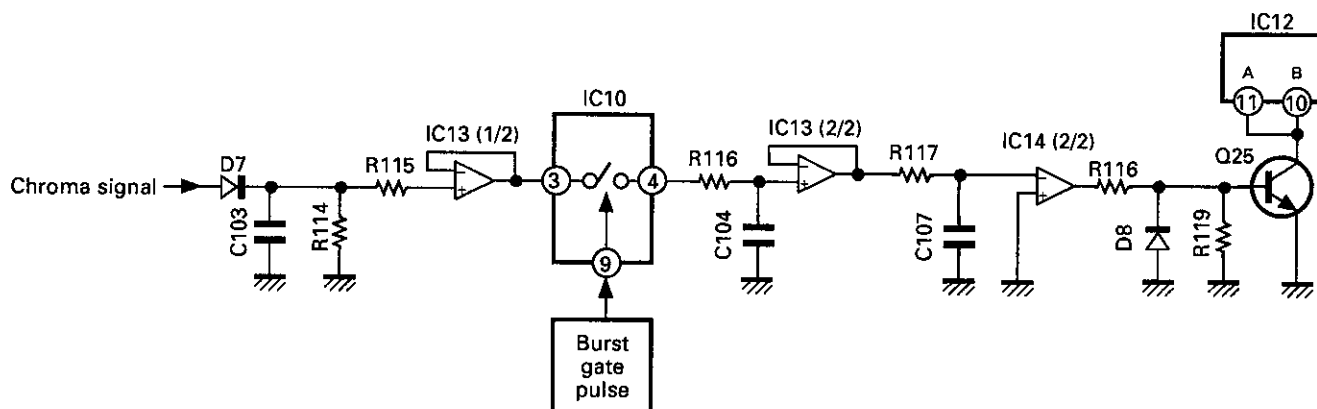
LVD-Z1 normally operates TBC with the burst signals. If a disc does not have a burst signal, it must be detected to operate TBC with the H system.

17-2. Explanation of functions

D7 and C103 half-wave rectify the chroma signals.

The burst part of the half-wave rectified signals is sampled and held by C104. C107 and R117 are used to turn off the detecting circuit when the disc does not have a burst signal (This operation is not turned on even if there is not a burst signal temporarily because of the L.P.F.).

Q25 is normally kept turned off, but turned on when there is not a burst signal. As the result, the TBC servo is operated by the H system.



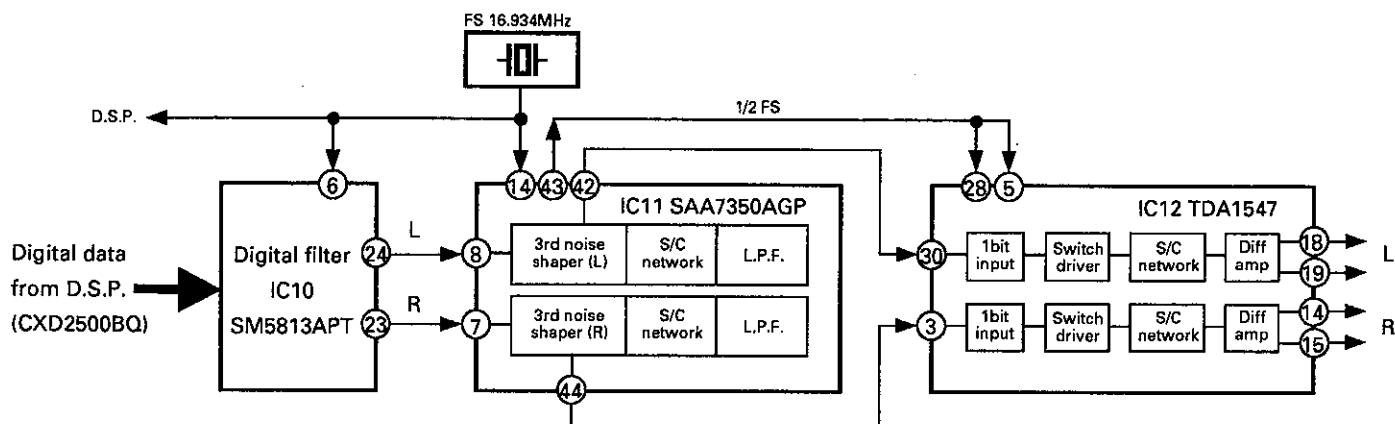
18. 1-bit DAC (X32-2350)

The digital sound of the LD or CD demodulated by the signal processing IC (CXD2500BQ) is input to the digital filter (SM5813APT). Then, it is 8-time over-sampled by the digital filter and converted into a 20-bit digital sound data, then output in parallel. This data of each channel is input to the bit-stream D/A converter (SAA7350AGP), where it undergoes digital processing of tertiary noise shaping, dithering, etc., then converted in to a PDM signal.

The above PDM signal is input to the switched ca-

pacitor D/A converter (TDA1547). It is converted by the switched capacitor network into positive and negative pulse lines based on the reference signal. Then, they are passed through the primary low-pass filter formed by the inside operating amplifier, then output as differential (Positive phase and negative phase) analog signals. They are filtrated by the difference amplifier and L.P.F. and converted in to analog audio signals.

Although the bit-stream D/A converter (SAA7350AG P) has a switched capacitor network, it is not used this time, but another chip TDA1547 is used.



CIRCUIT DESCRIPTION

19. Analog Sound OFF Circuit (X32-2350)

19-1. Outline

This circuit turns off the power supply of the analog sound demodulation IC CA0002AM (IC3, X32-2350), RF input, and VCO error input when digital sounds are played (CD DISC mode or digital sound mode of LD DISC). By this operation, the effects of the analog circuit are reduced for higher digital sound quality in the digital sound play mode.

19-2. Explanation of functions

(1) Power supply control of analog sound demodulation IC CA0002AM

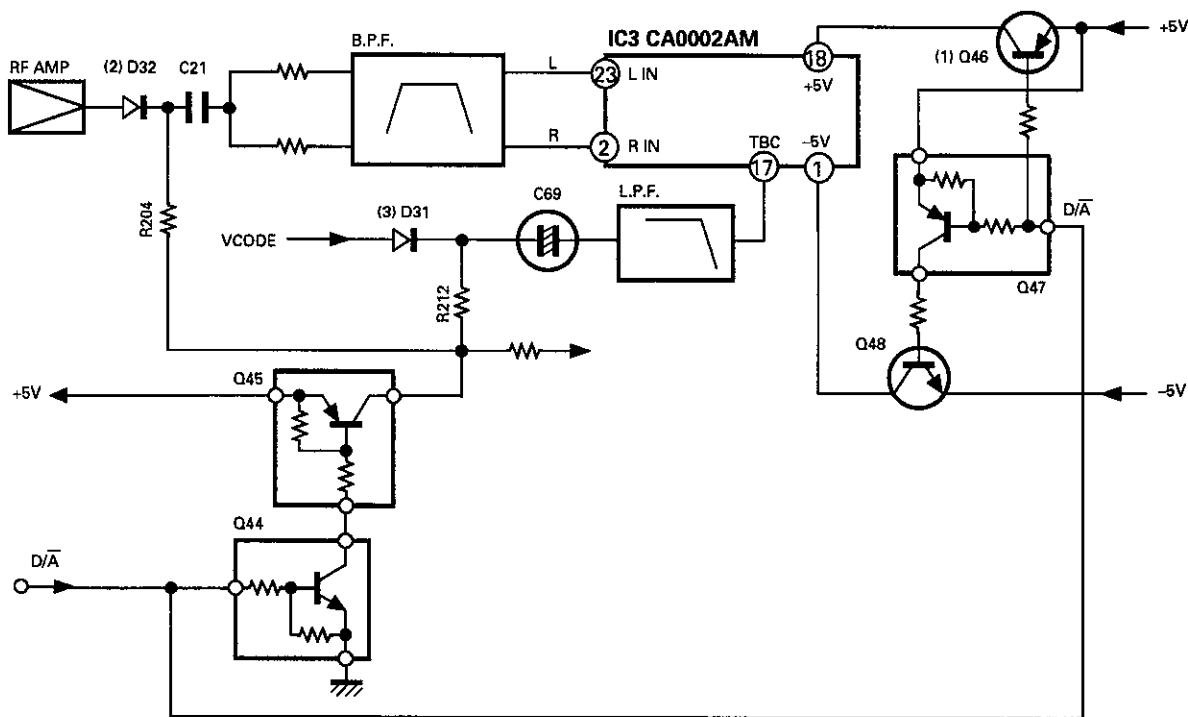
While digital sounds are replayed, the main μ -com outputs the control signal $D/\bar{A}$ ($D \rightarrow "H"$ in digital sound mode, $\bar{A} \rightarrow "L"$ in the analog sound mode). Q46 and Q48 are turned off by this $D/\bar{A}$ signal to turn off the power for CA0002AM. In the analog sound play mode, Q46 and Q48 are turned on to turn on the power for demodulation of analog sounds.

(2) RF signal input control

In the digital sound replay mode, the above $D/\bar{A}$ signal is used after inverted. The cathode side of D32 is set to the H level (5V). Since the signal on the anode side is an RF signal of 2Vp-p almost around 0V, D32 is turned off to cut the input of the RF signal. In the analog sound replay mode, the cathode side of D32 becomes negative and D32 is turned on to input the RF signal.

(3) Control of VCO error input

In the digital sound replay mode, the signals used in (2) above are used. The cathode side of D31 becomes the H level (5V). Since the VCO error on the anode is an error signal of 0.3Vp-p around 0V, D31 is turned off to cut the input of CA0002AM. In the analog sound replay mode, the cathode side of D31 becomes negative and D31 is turned on to input the VCO error.



CIRCUIT DESCRIPTION

20. 3-phase Brushless Motor Drive Circuit (X29-2380)

The disc motor error signal (MTM) PWM-converted at 15.73kHz is converted into voltage by Q1, Q5, and Q7. Then, it is smoothed through L1 and D4 by Q6 as the driver, and applied to the emitter of the motor drive transistor IC1. The current flowing in the motor and its revolving speed are determined by this smoothed voltage.

The direction of rotation of the motor is determined by MTP and controlled by IC4. The current flowing in the motor is detected by R1 and amplified by IC3 (1/2). If a current larger than 2A is detected by the compara-

tor of IC3 (2/2), the MTM signal is controlled by D5 to limit the current to 2A. The magnetic field is detected by the hole elements installed near each coil in the motor.

The output of the hole elements changes as shown below (Ha→Hb→Hc). According to the sensed position, IC4 forms a drive logic to control the drive transistor as indicated by the lower part of the timing chart.

In case of (1), for example, the transistors IC2 (2/3) and IC1 (1/3) are turned on, and the current flows from Lb → La in the motor as shown below. Since the current flows via ①→②→③→④→⑤→⑥→⑦→..., a rotating field is generated in the motor, and the 3-phase motor starts turning.

Timing chart

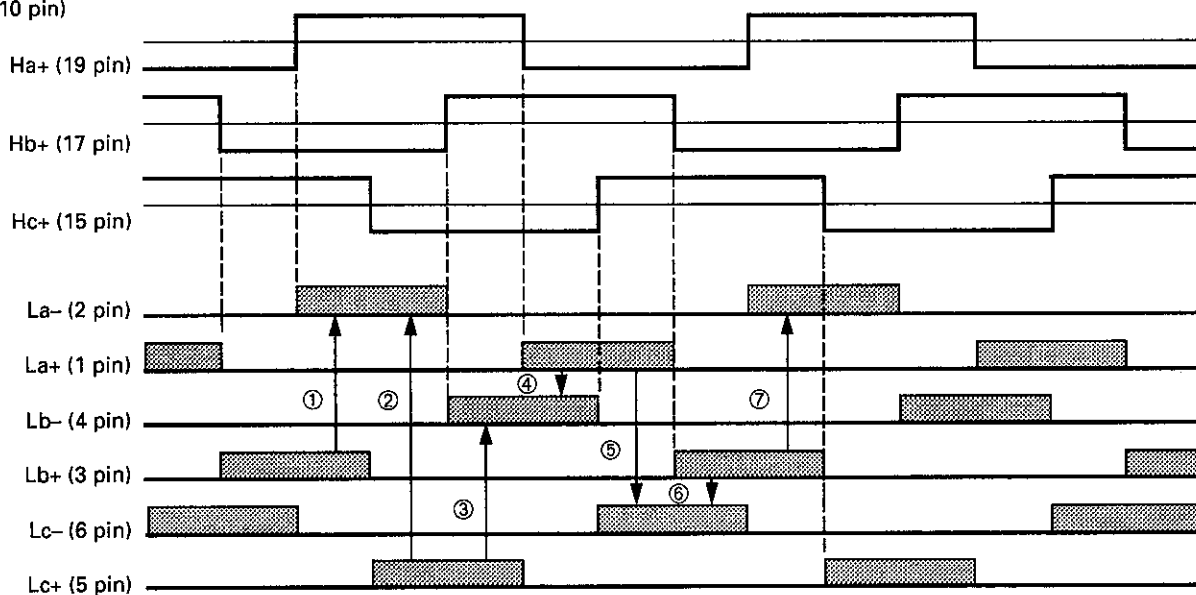
Forward rotation

(Position sensing signal moves via Ha→Hb→Hc).

START/STOP "H" (8 pin)

CW/CCW "L" (9 pin)

BRAKE "H" (10 pin)

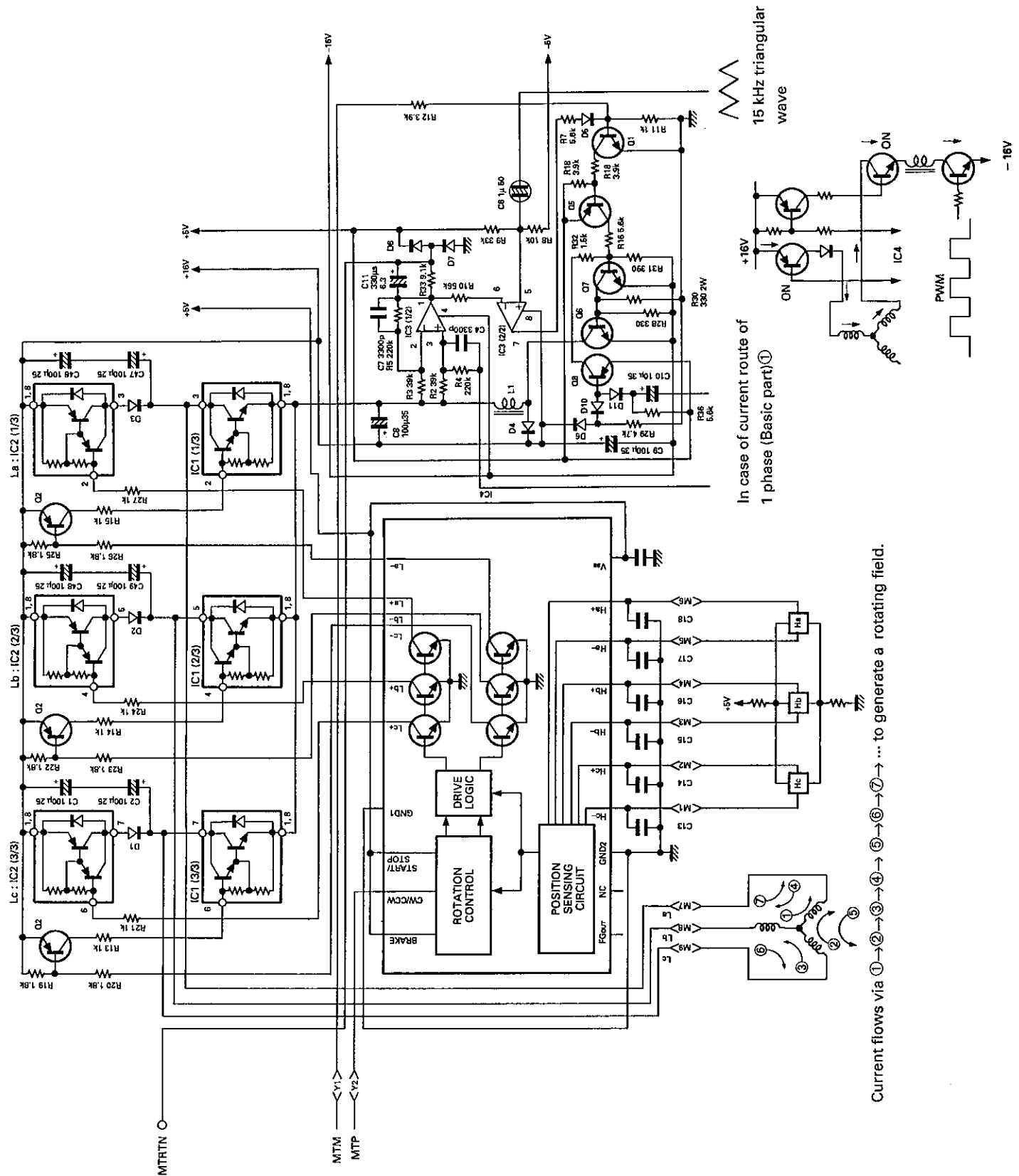


When the current limiter loop of the former type is braked, L1 vibrates at a frequency other than 15kHz, the coil sounds, and it has been a problem. In LVD-Z1, a triangular wave of 15kHz is used as the reference voltage of the comparator so that the brake timing is

modulate at 15kHz and the loop will always move near 15kHz to reduce the sound of the coil.

The coil consisting of Q8, D6, D10, and D11 stops the current from flowing in the motor when the power is turned on and off to prevent the turntable from turning wrongly.

CIRCUIT DESCRIPTION



CIRCUIT DESCRIPTION

21. Operation of Tray (X29-2380)

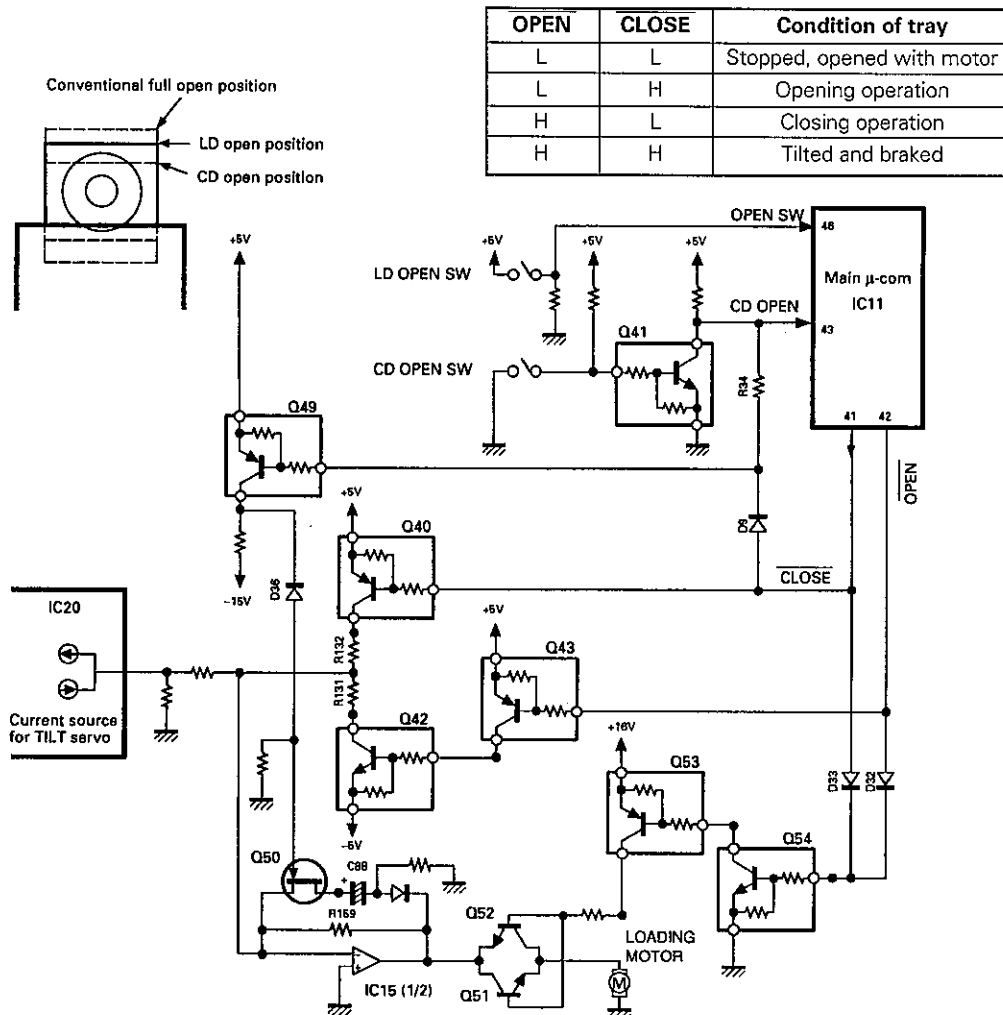
LVD-Z1 has a special switch to open the LD tray fully to eliminate a play when the tray is fully opened and to lighten the resistance when the tray is closed by pushing. This switch is installed a little more user's side (set side) than the former model. A CD open switch is also installed. With this switch, if the CD open key is pushed, the tray is half opened so that a CD can be set. When the tray is fully opened, the loading motor is disconnected so that it can be closed more lightly.

For higher quality, the tray is accelerated slowly until it passes the CD open switch when it is closed from the LD open position, and it is slightly braked when opened to prevent it from overrunning. If the open key is pushed, CLOSE becomes H and OPEN becomes L, and Q40 is turned off and Q42 is turned on. As the result, a voltage determined by R131 and R159 is applied to the motor to open the tray. Since D33 is turned on at this time, Q53 and Q51 are turned on.

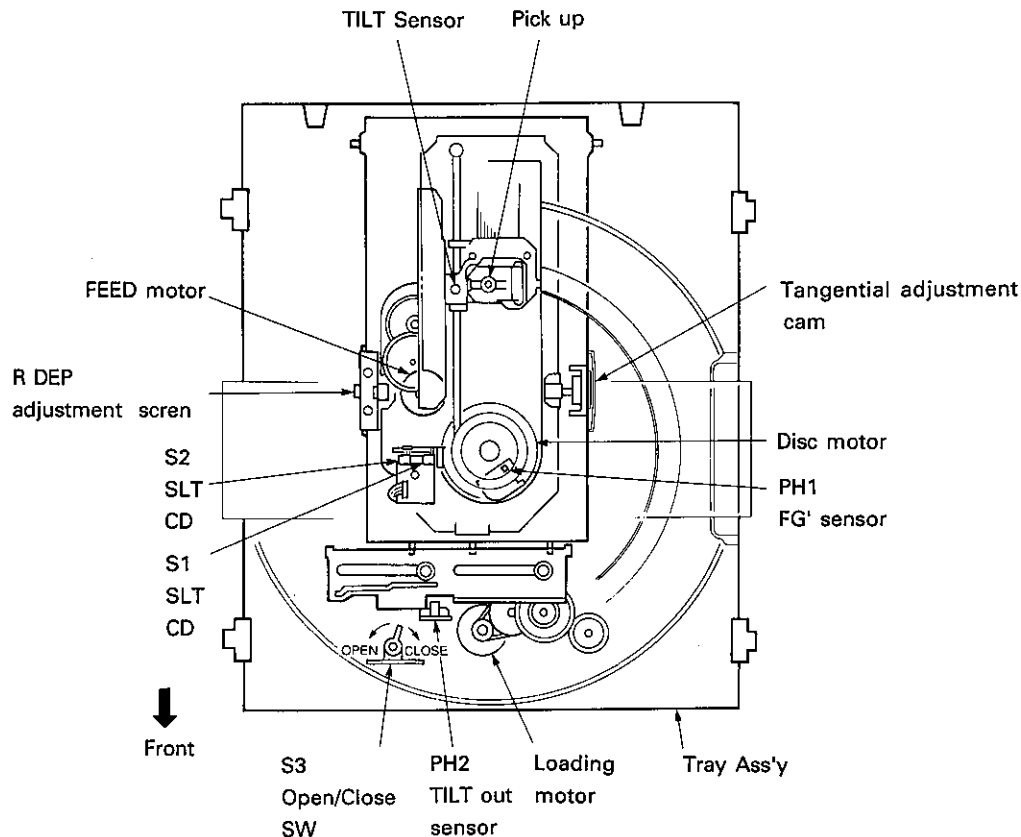
When the LD open switch is turned on, both CLOSE and OPEN become H for a moment to brake the tray, then both CLOSE and OPEN become L. Since D32, D33, Q53, Q51, and Q52 are turned off, the motor is released (The same operation is executed in the CD open mode). If the open key is pushed at the CD open position, the tray is fully opened according to the same sequence.

If the tray is closed with the close key or by pushing it and the LD open switch is turned off, CLOSE becomes L and OPEN becomes H, and Q42 is turned off and Q40, D32, and Q52 are turned on. As the result, an inverse voltage is applied to the motor (At this time, the CD open signal is at H). Since Q50 is turned on, the voltage applied to the motor is gradually heightened with the time constant determined by C88 and R159.

If the tray closes smoothly and exceeds the CD open switch, Q50 is turned off to close the tray normally. When the tray is opened, D9 is turned on. Since D36 is turned and Q50 is turned off, the time constant is not applied.



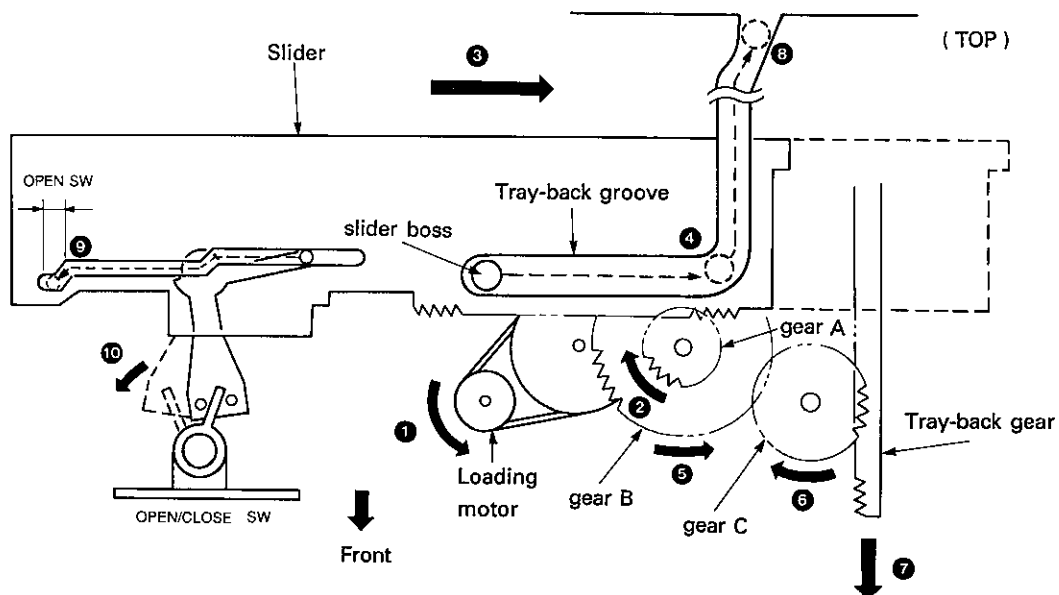
MECHANISM OPERATION DESCRIPTION



1. TRAY OPEN

The loading motor turns to the arrow direction (1) when pushing Tray-open button on the front panel. The gear (A or B), which is not locked, starts to turn. In this case, the gear A turns to arrow direction (2) because the tray is locked by slider boss. The slider starts to move to arrow direction (3) by the gear A. The Slider boss moves rightwards along the groove of the tray-back. The gear A and the slider stop when slider boss at the groove-end of the right side (4).

At this time, the tray-lock function is free because slider boss is in front and backwards. The gear B starts to turn to arrow direction (5) and the gear C (6), too. The tray-open function (7) starts when the gear of the tray-back moves. The slider boss moves rightwards slightly (8). This movement (9) changes switch to arrow direction (10) and tray-open function is finished perfectly.



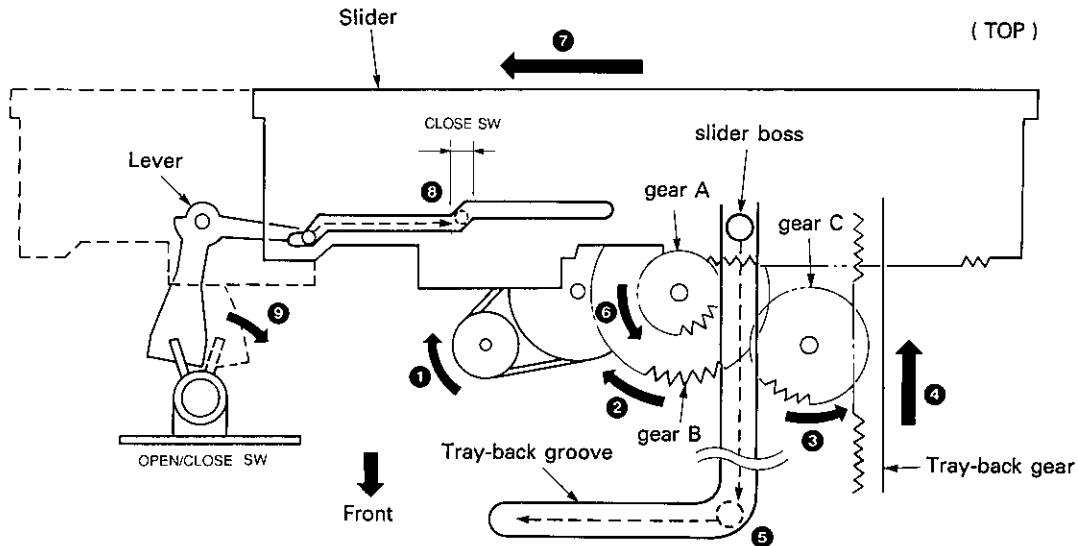
MECHANISM OPERATION DESCRIPTION

2. TRAY CLOSE

The loading motor turns to the arrow direction (1) when pushing Tray-close button on the front panel. Both gear B and C start to turn to arrow direction (2) (3). The tray-close function (4) starts by the gear of the tray-back. The gear B stops to turn when slider

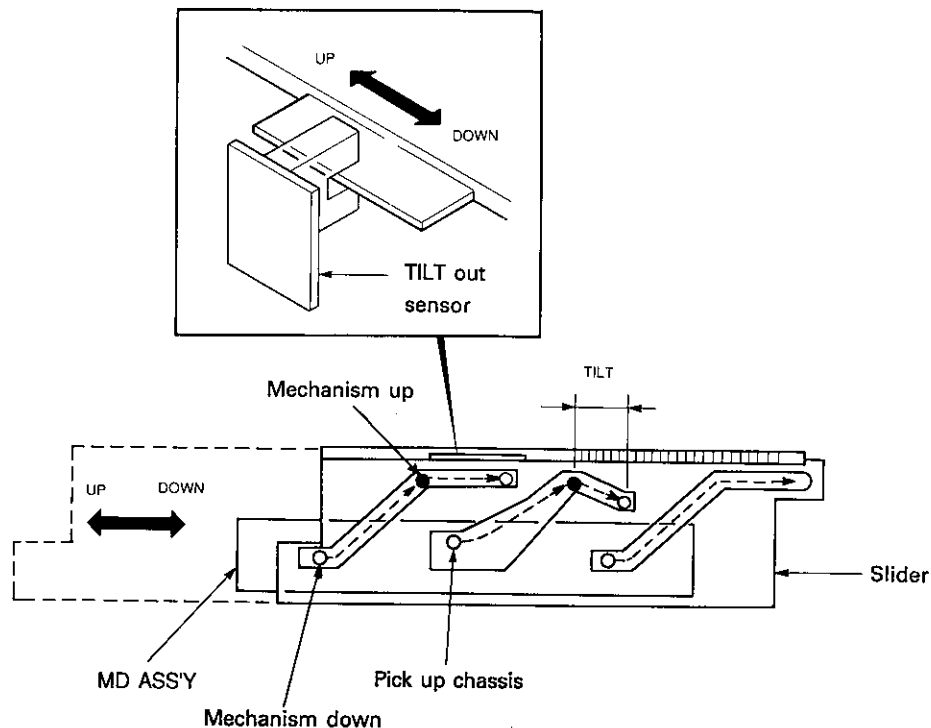
boss moves at the point (5) from front and backwards to right and leftwards.

The slider moves to arrow direction (7) when the gear A starts to turn (6). The slider moves the lever (8) and the lever changes switch to arrow direction (9), and the tray-close function is finished perfectly.



3. TILT

The slant of slider-center groove holds up position leads the tilt function after the pickup ass'y holding up-position.

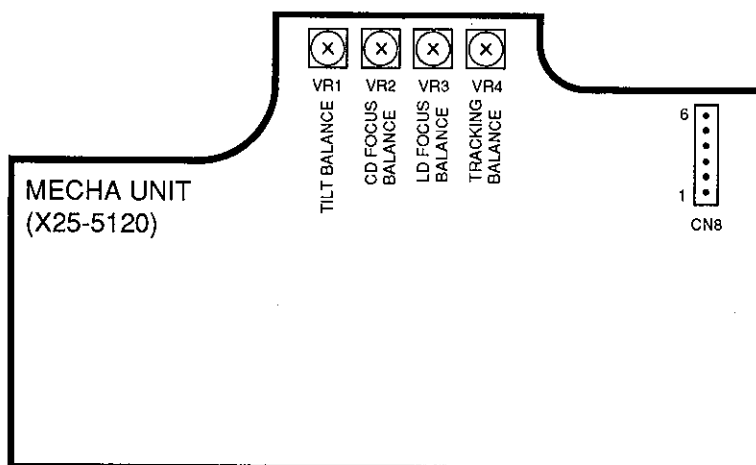


ADJUSTMENT

MECHANISM CONTROL UNIT (X25-5120)

NO.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG.
1	TILT BALANCE	LD test disc	Connect the TV monitor to the video output.	F.No.23402 STILL(still image)	VR1 (X25-5120,A/5)	Minimize the crosstalk on the screen.	①
		LD disc	Connect the oscilloscope to RF(CN6-6) on X32-2350(A/2).	F.No.20000 STILL(still image)		Maximize the RF signal (eye pattern) amplitude.	
2	LD FOCUS BALANCE	LD test disc or LD disc	Connect the oscilloscope to RF(CN6-6) on X32-2350(A/2).	PLAY	VR3 (X25-5120,A/5)	Maximize the RF signal amplitude.	①
3	TRACKING BALANCE	LD test disc or LD disc	Connect the oscilloscope to TE(CN6-1) on X32-2350(A/2).	F.No.5000 STILL(still image)	VR4 (X25-5120,A/5)	Make the positive and negative jump pulses equal.	②
4	CD FOCUS BALANCE	CD test disc	Connect the oscilloscope to RF(CN6-6) on X32-2350(A/2).	PLAY	VR2 (X25-5120,A/5)	Maximize the RF signal(eye pattern) amplitude.	③

LD test disc:SONY REF5A-12. LD disc: Commercial LD disc(CAV with Digital sound)
 CD test disc:SONY YEDS-18(Type 4)

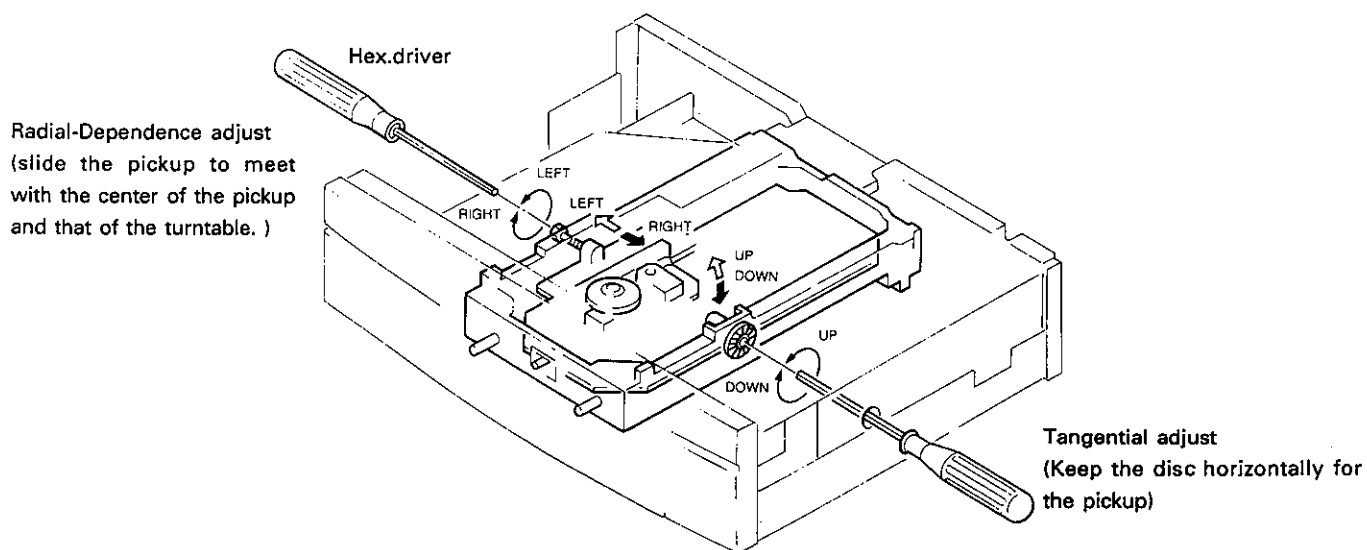


ADJUSTMENT

MECHANISM ADJUSTMENT

NO.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG.
1	TANGENTIAL	CD test disc	Connect the oscilloscope to RF(CN6-6) on X32-2350(A/2).	PLAY	Tangential nut (Turn within ± 4 clicks)	Maximize the RF signal (eye pattern)	
2	R-DEPENDENCE	CD test disc	Connect the oscilloscope to E and F(CN8-1,2) on X25-5120 (A/5).	PLAY	R-dep.nut	Lissajons' figure = 45°	

CD test disc: SONY YEDS-18(Type 4)

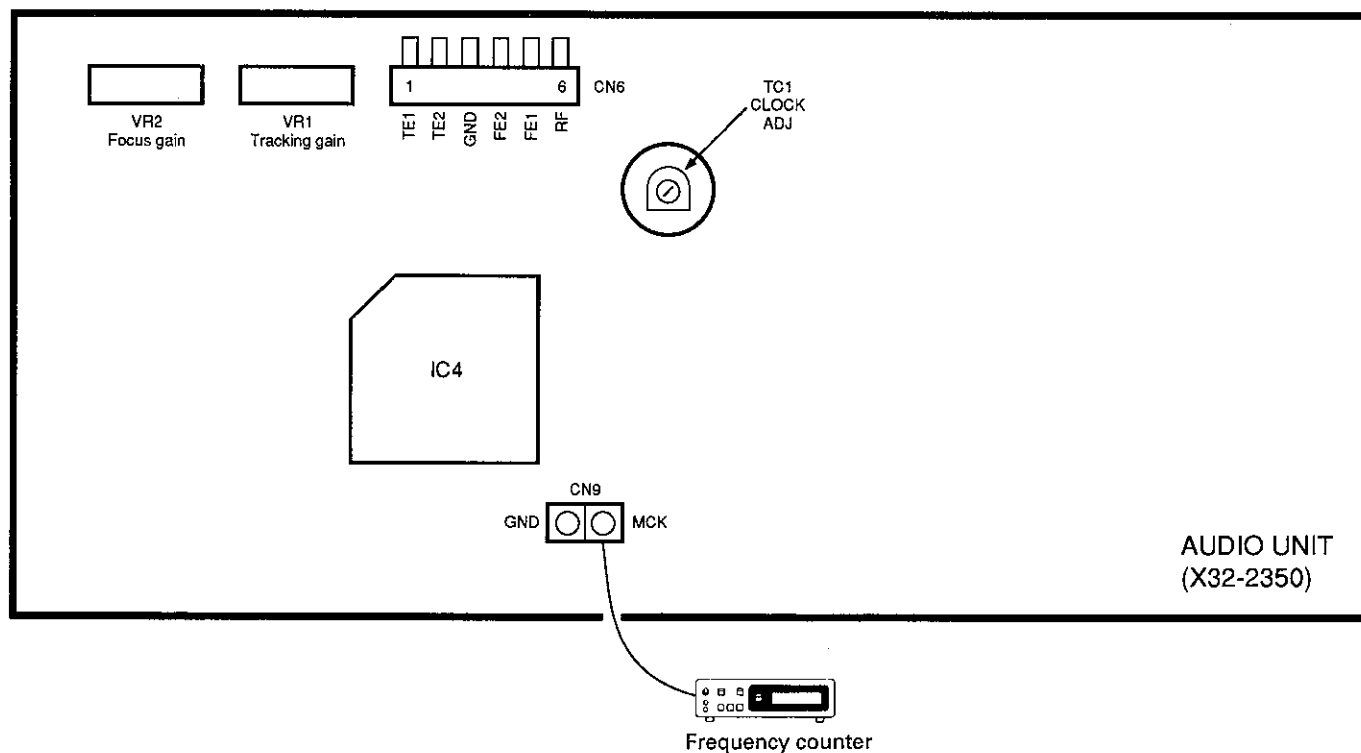


ADJUSTMENT

AUDIO UNIT (X32-2350)

NO.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG
1	FOCUS GAIN	CD test disc Apply signal (1.0kHz/200mVp-p) to CN6 pins 4 and 5 on X32-2350 (A/2).	Connect a L.P.F. to CN6 pins 4 and 5 on X32-2350 (A/2), to which connect an oscilloscope or AC voltmeter.	PLAY	VR2 (X32-2350, A/2)	Two VTMs should read the same value.	
2	TRACKING GAIN	CD test disc Apply signal (1.3kHz/200mVp-p) to CN6 pins 1 and 2 on X32-2350 (A/2).	Connect a L.P.F. to CN6 pins 1 and 2 on X32-2350 (A/2), to which connect an oscilloscope or AC voltmeter.	PLAY	VR1 (X32-2350, A/2)	Two VTMs should read the same value.	
3	MASTER CLOCK FREQUENCY	CD disc	Connect a frequency counter to CN9 (MCK) on X32-2350 (A/2).	STOP	TC1 (X32-2350, B/2)	16.93440MHz $\pm$ 50Hz	

CD test disc: SONY YEDS-18 (Type 4) CD disc: Commercial CD disc
 LPF: Around 47k Ω +390pF or so.

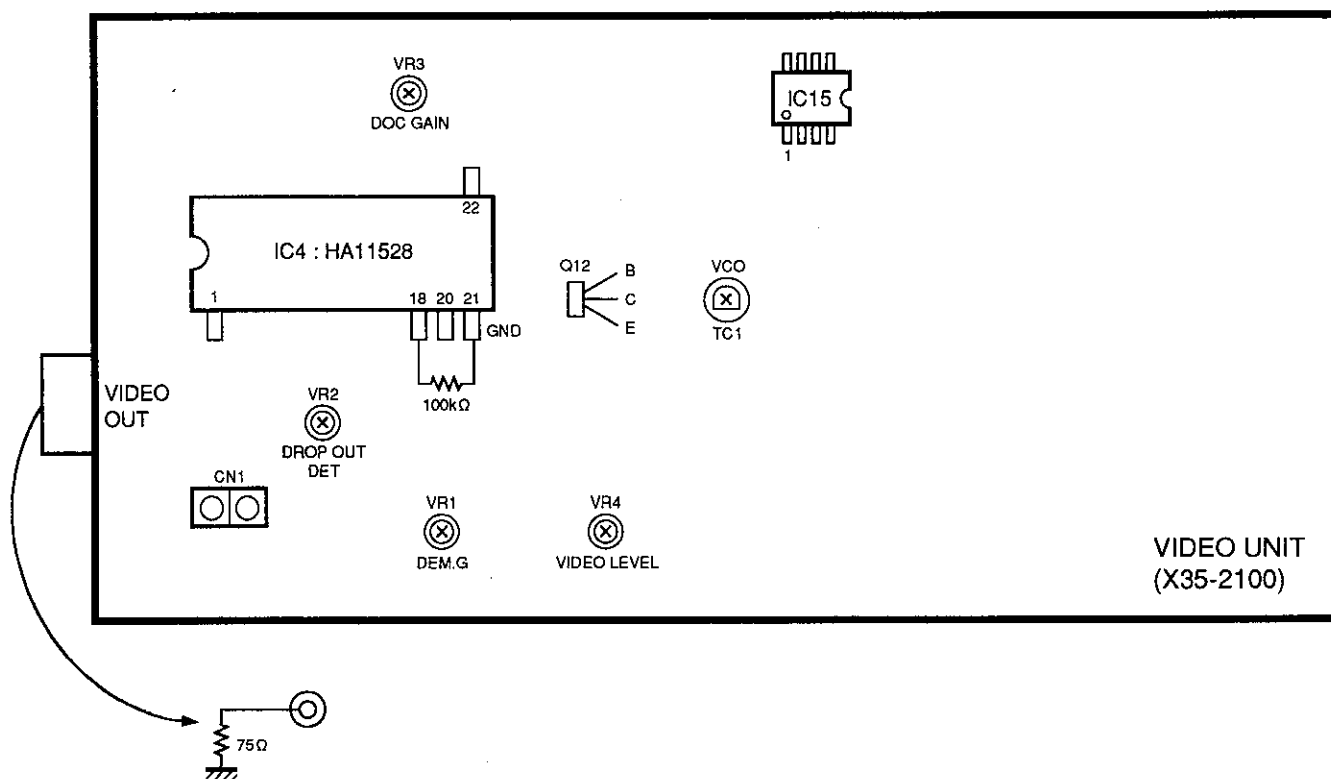


ADJUSTMENT

VIDEO UNIT (X35-2100)

NO.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG.
1	DROP-OUT DETECTION LEVEL	Connect 100k Ω resistor to pin18 and GND of IC4 on X35-2100(B/2). And apply sine-wave(6MHz,0.5Vp-p) to CN1 on X35-2100(B/2).	Connect an oscilloscope to pin 22 of IC4 on X35-2100(B/2).	STOP	VR2 (X35-2100,B/2)	Set the center of waveform from 1.6V to 1.9V D.C.	
2	VCO	LD disc	Connect an oscilloscope to pin 1 of IC15 on X35-2100(B/2).	PLAY	TC1 (X35-2100,B/2)	DC=0V(mean value)	④
3	VIDEO DEMODULATION LEVEL	LD test disc	Connect an oscilloscope to emitter of Q12 on X35-2100(B/2).	F. No. 13000 STILL(still image)	VR1 (X35-2100,B/2)	Set the video amplitude to 1.8Vp-p.	⑤
4	DOC GAIN	LD test disc	Connect an oscilloscope to pin18 and 20 of IC4 on X35-2100(B/2). (CH2: INVERTED)	F. No. 7000 STILL(still image)	VR3 (X35-2100,B/2)	No video signal when add CH1 and CH2 signals.	⑥
5	VIDEO OUTPUT LEVEL	LD test disc	Connect 75 Ω resistor to VIDEO out. Connect an oscilloscope across the resistor.	F. No. 13000 STILL(still image)	VR4 (X35-2100,B/2)	Video signal amplitude:1.0Vp-p.	⑦

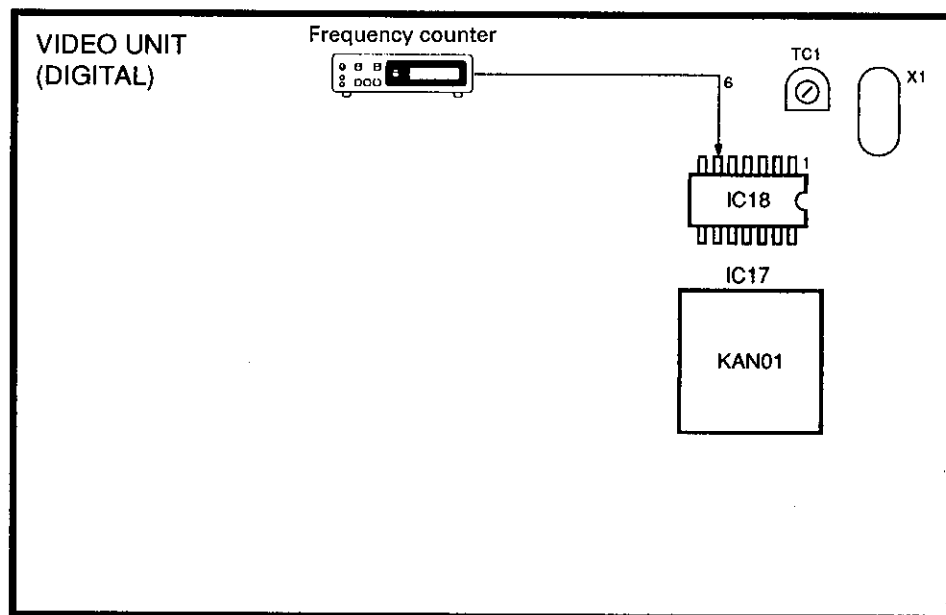
LD test disc: SONY REF5A-12 LD disc: Commerical LD disc(CAV with Digital sound)



ADJUSTMENT

VIDEO UNIT : Digital (X35-2110)

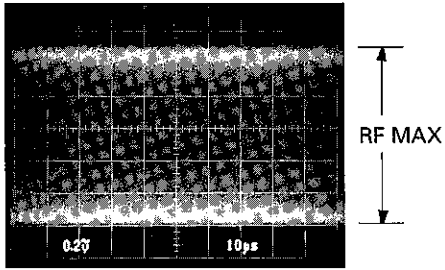
NO.	ITEM	INPUT SETTING	OUTPUT SETTING	PLAYER SETTING	ALIGNMENT POINT	ALIGN FOR	FIG.
1	REFERENCE 8fsc	POWER ON	Connect the frequency counter to pin6 of IC18 on X35-2110.	STOP	TC1 (X35-2110)	28.636360MHz±80Hz	



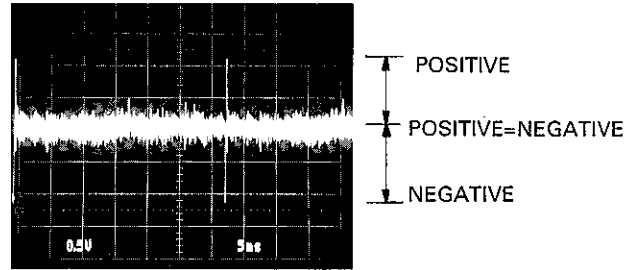
ADJUSTMENT

Waveform

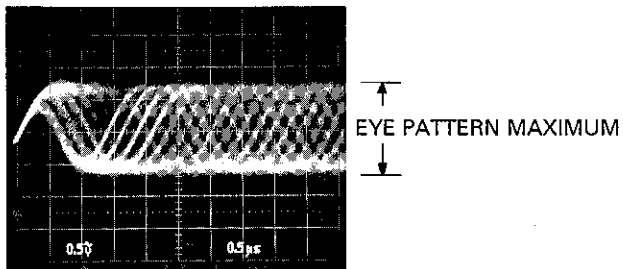
① TILT BALANCE, LD FOCUS BALANCE



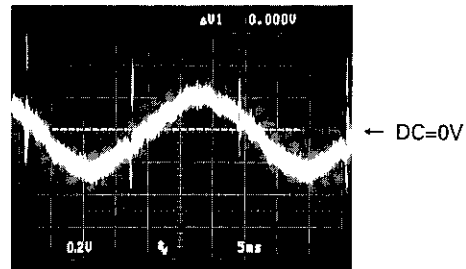
② TRACKING BALANCE



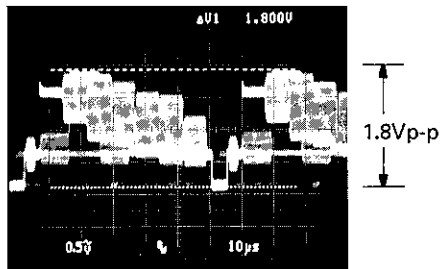
③ CD FOCUS BALANCE



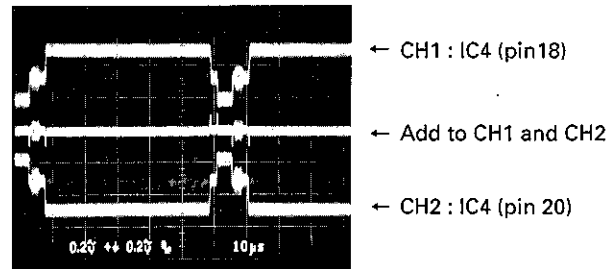
④ VCO



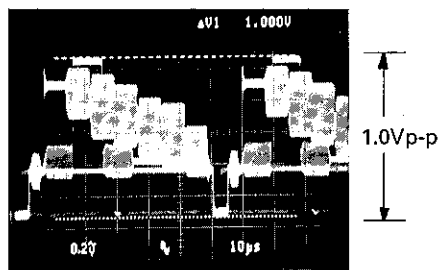
⑤ VIDEO DEMODULATION LEVEL



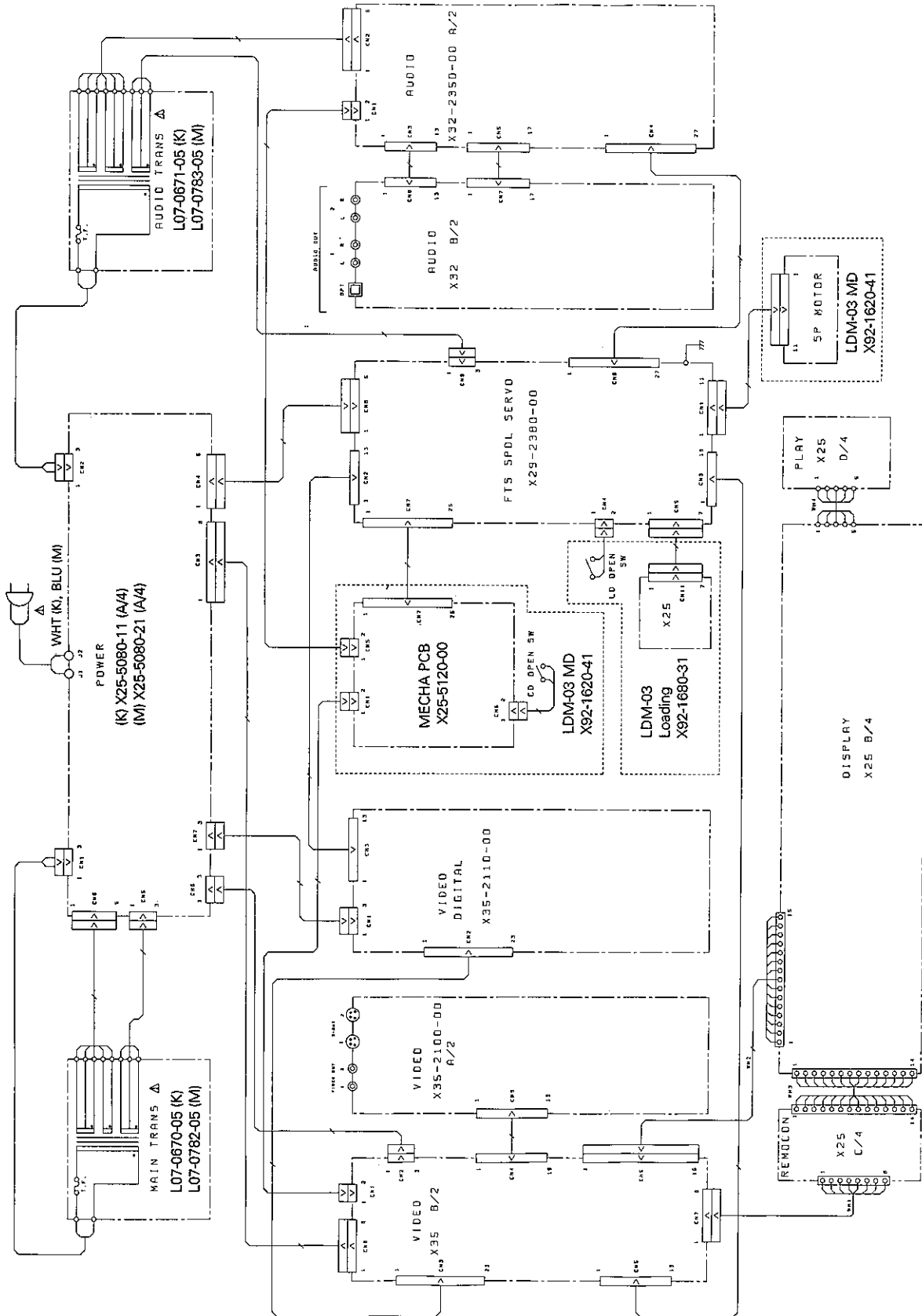
⑥ DOC GAIN



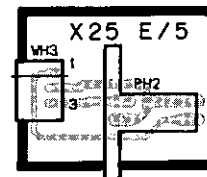
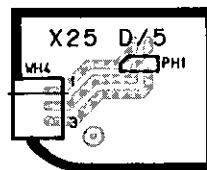
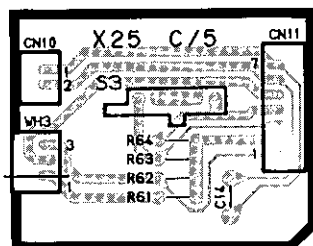
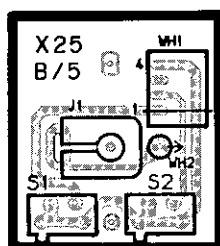
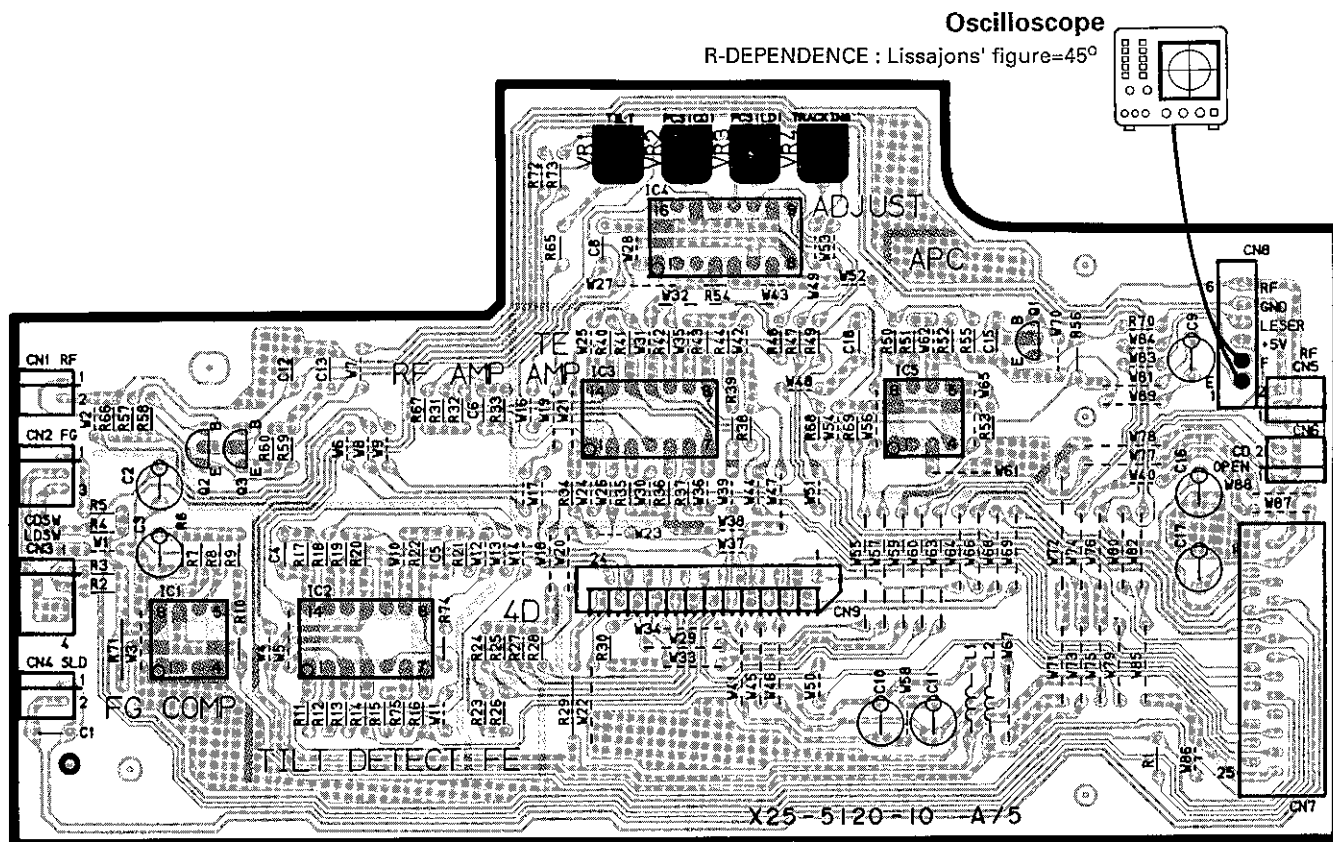
⑦ VIDEO OUTPUT LEVEL



WIRING DIAGRAM

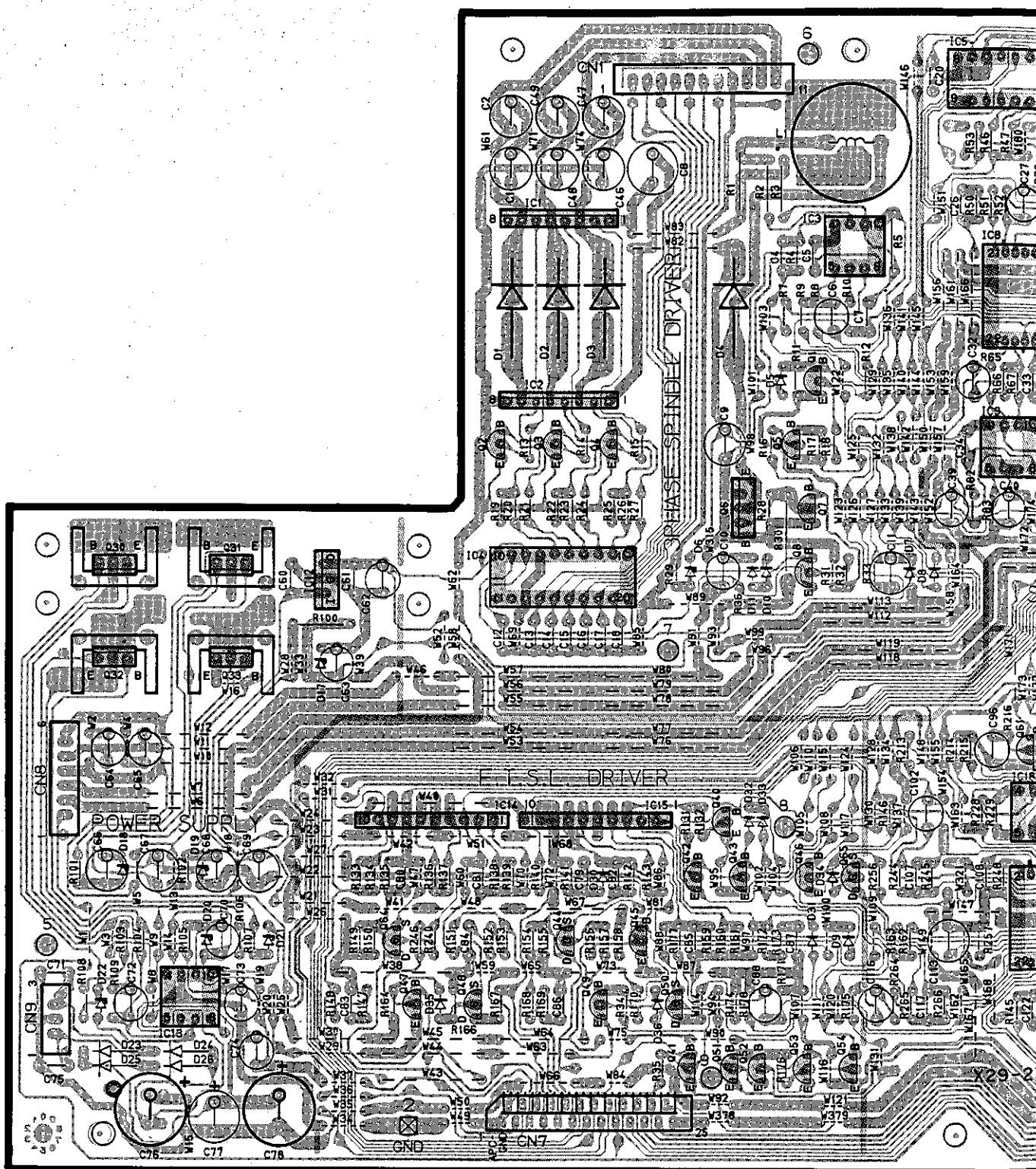


PC BOARD (COMPONENT SIDE VIEW)

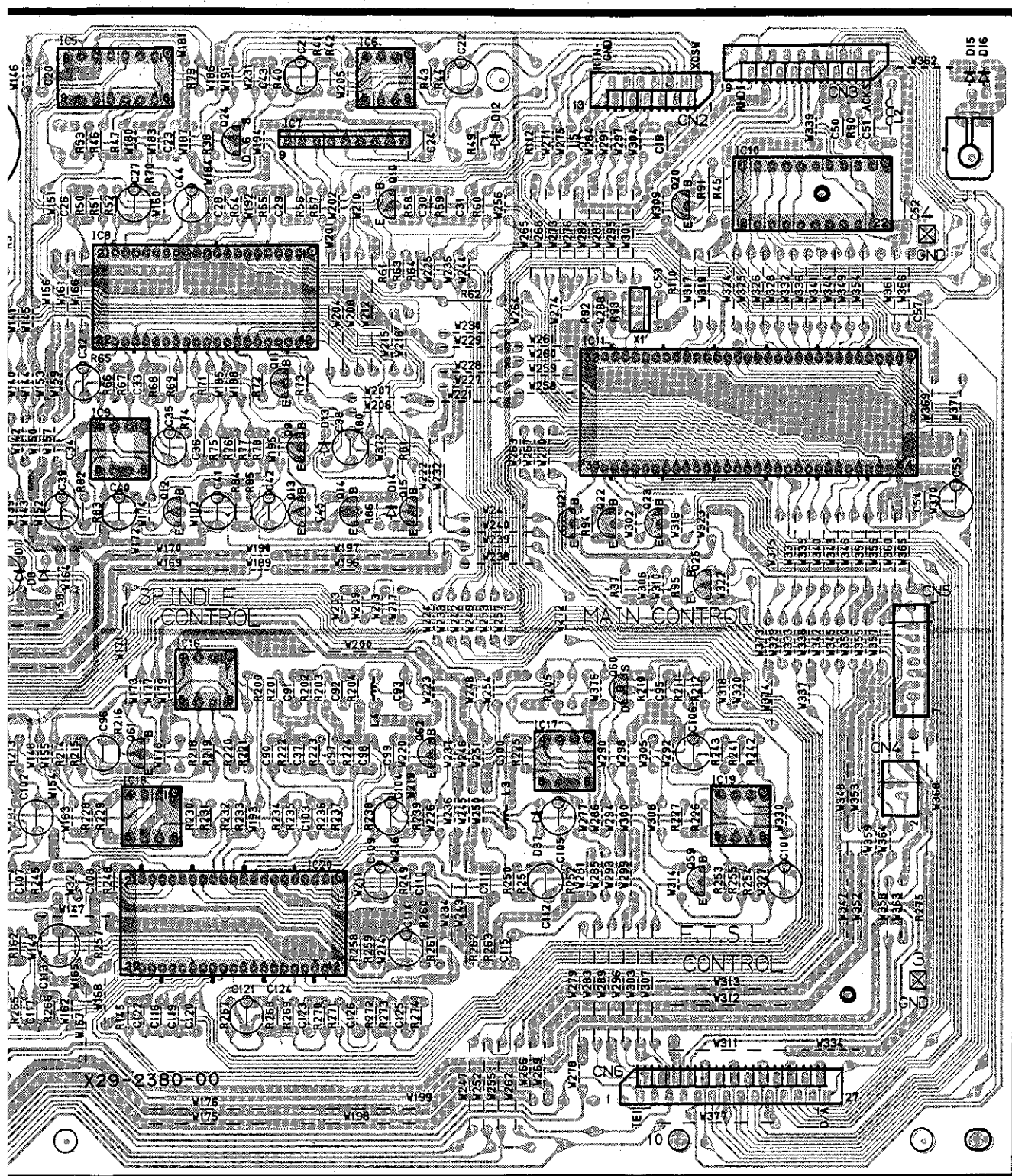


Refer to the schematic diagram for the values of resistors and capacitors.

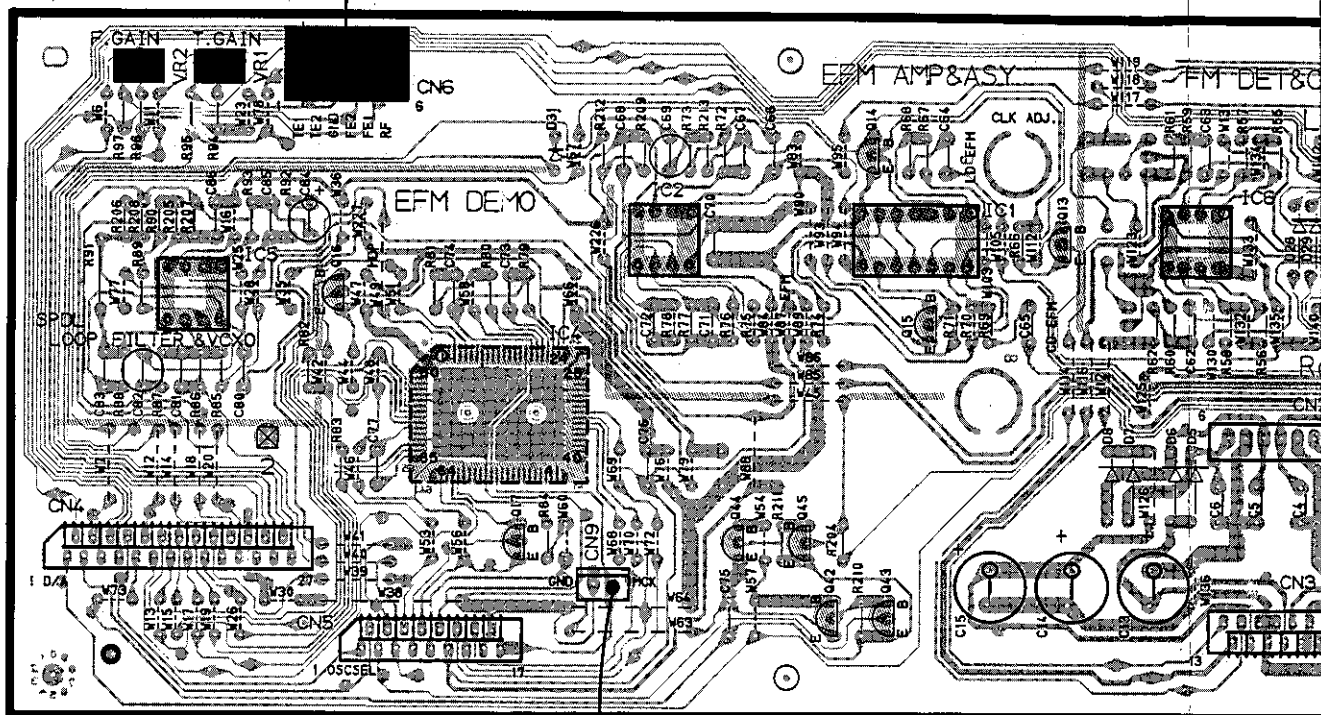
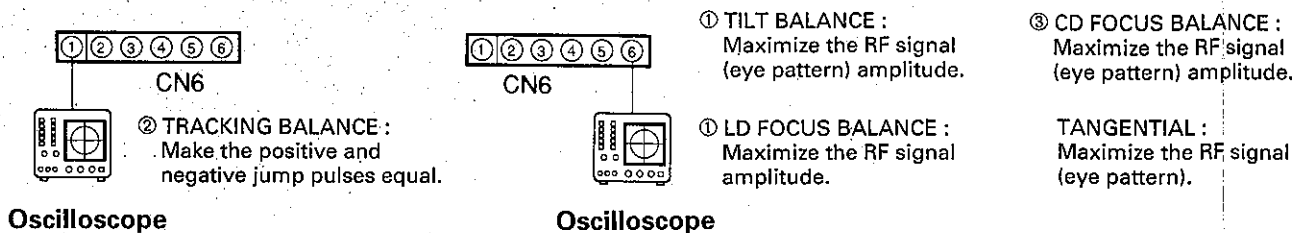
PC BOARD (COMPONENT SIDE VIEW)



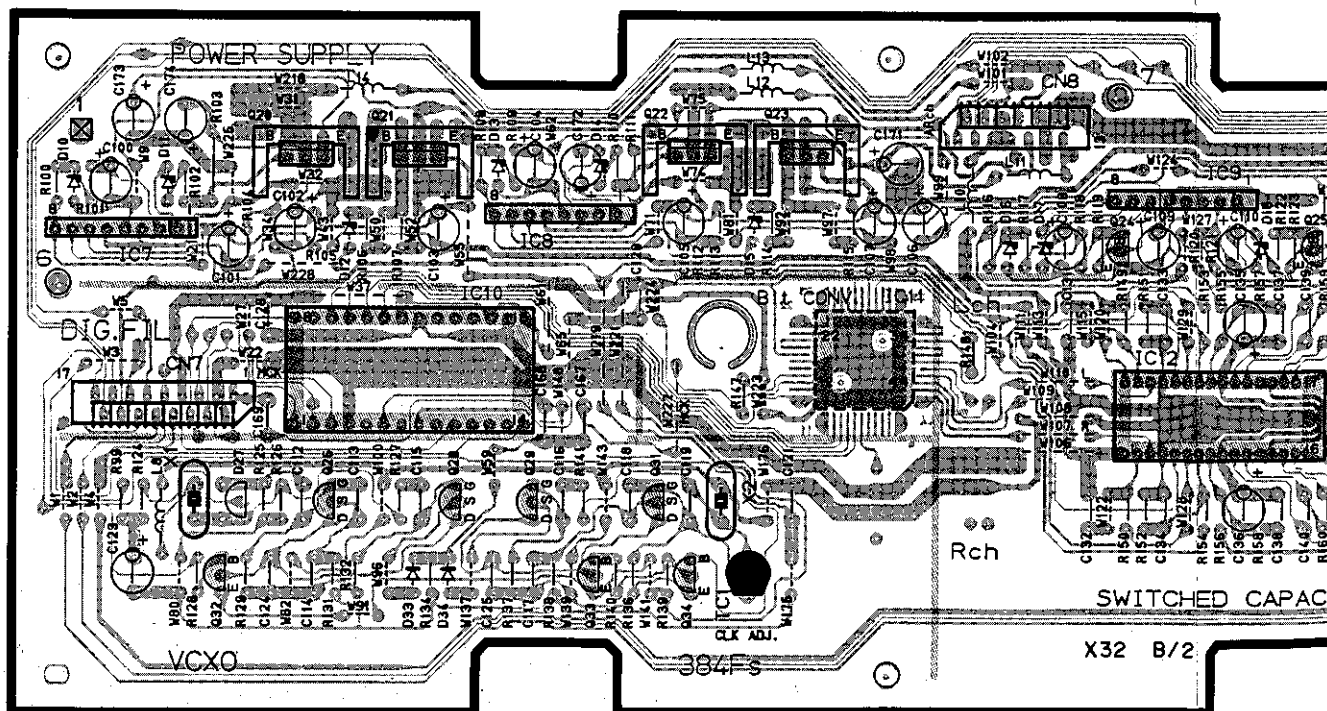
Refer to the schematic diagram for the values of resistors and capacitors.



PC BOARD (COMPONENT SIDE VIEW)

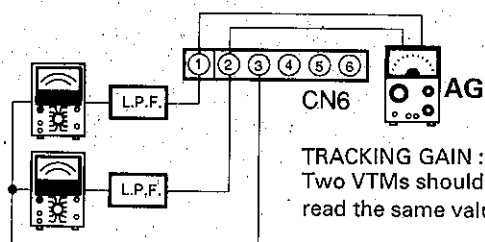


 **Frequency counter**
MASTER CLOCK FREQUENCY : 16.9344MHz ± 50Hz

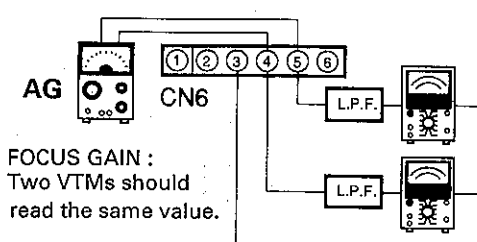


IS BALANCE :
the RF signal
amplitude.

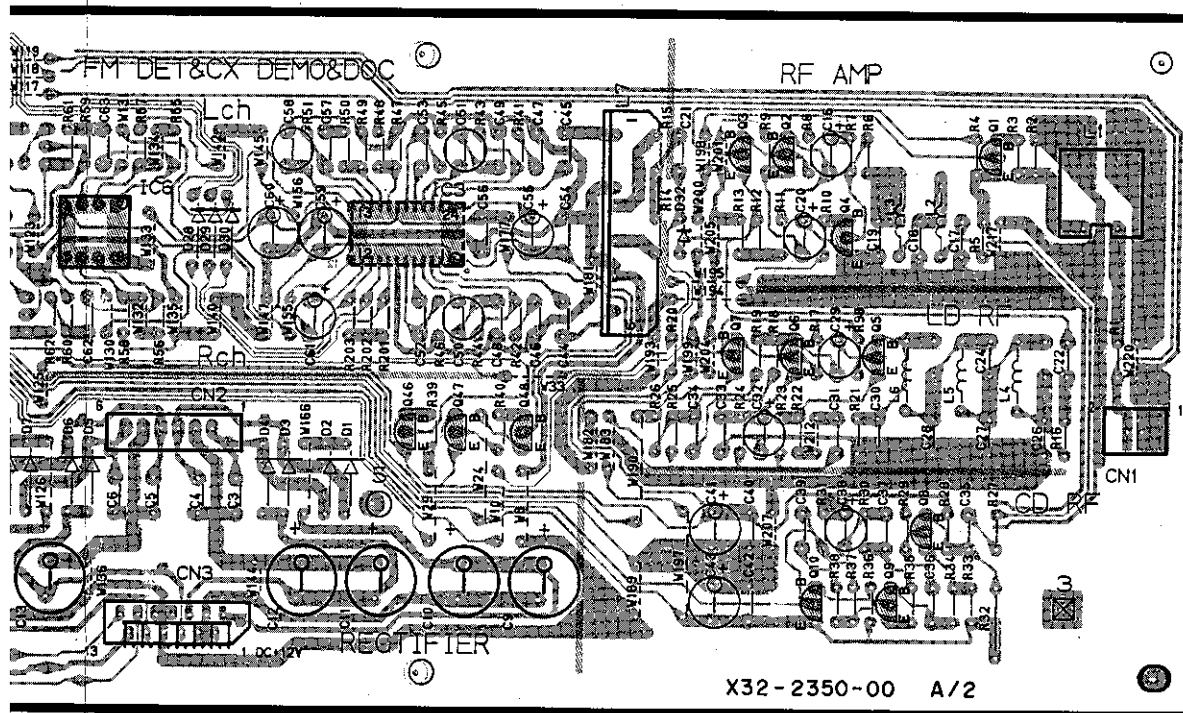
INITIAL :
the RF signal
amplitude.



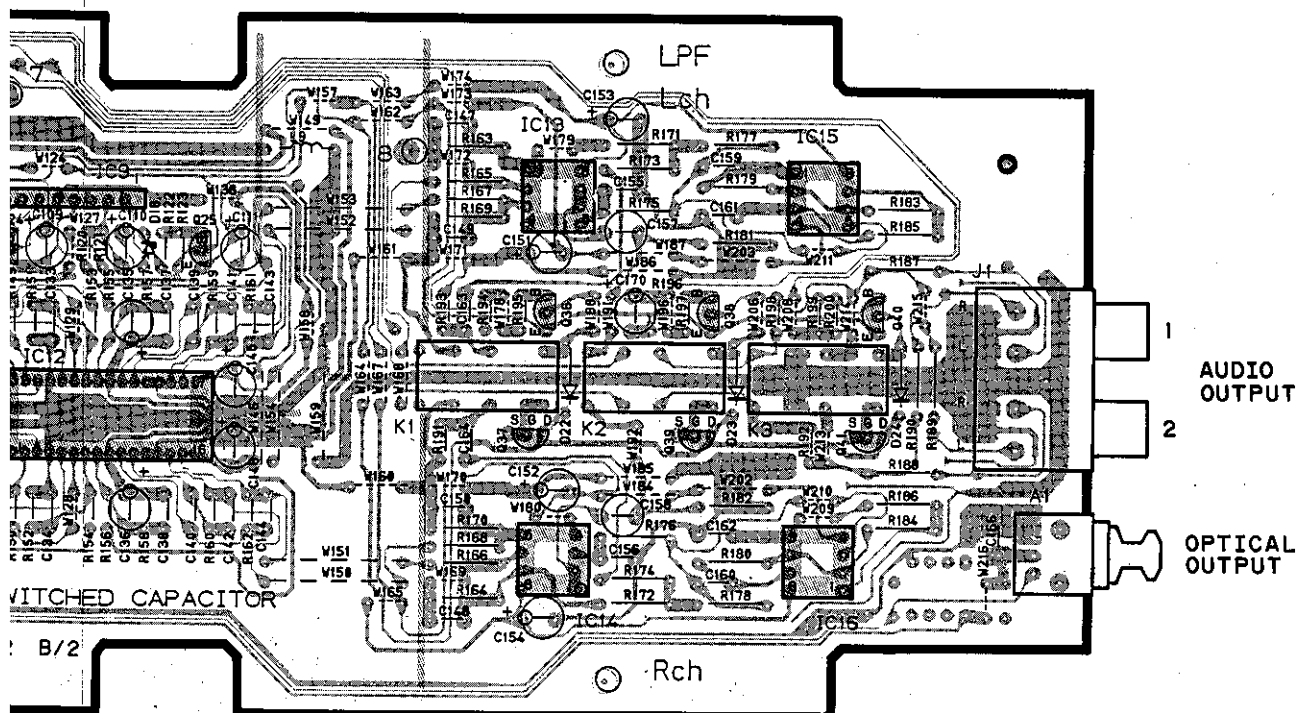
AC voltmeter



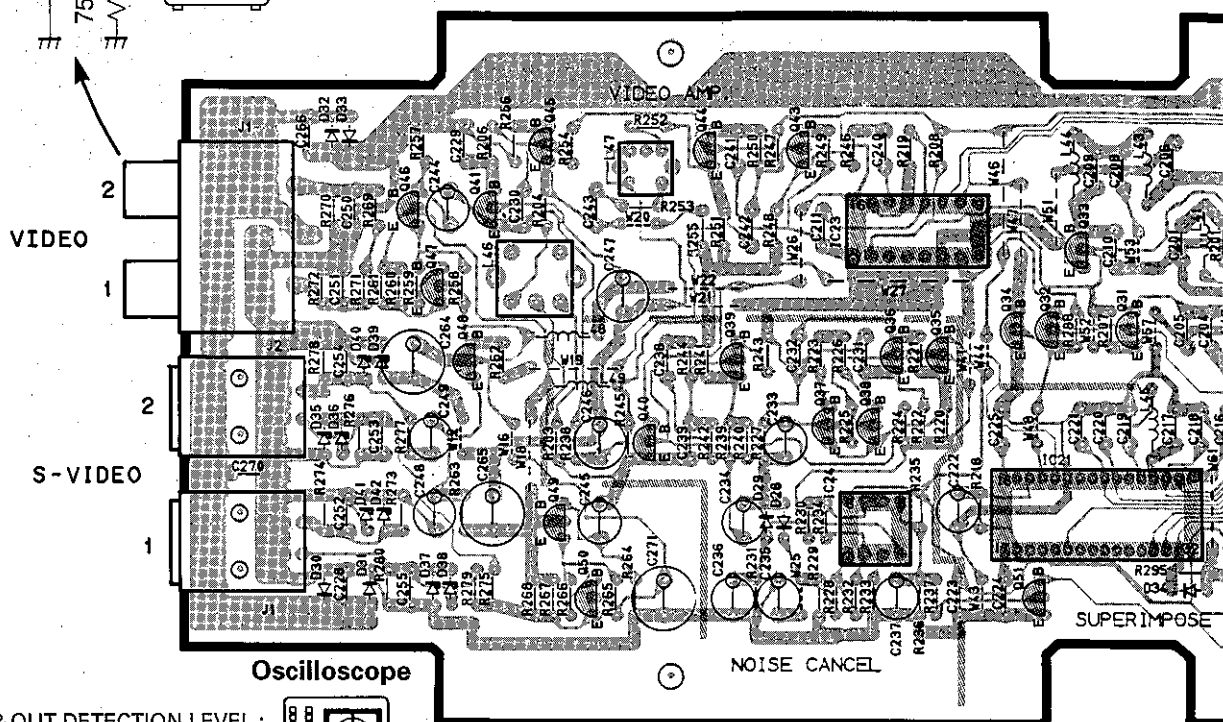
AC voltmeter



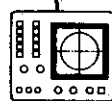
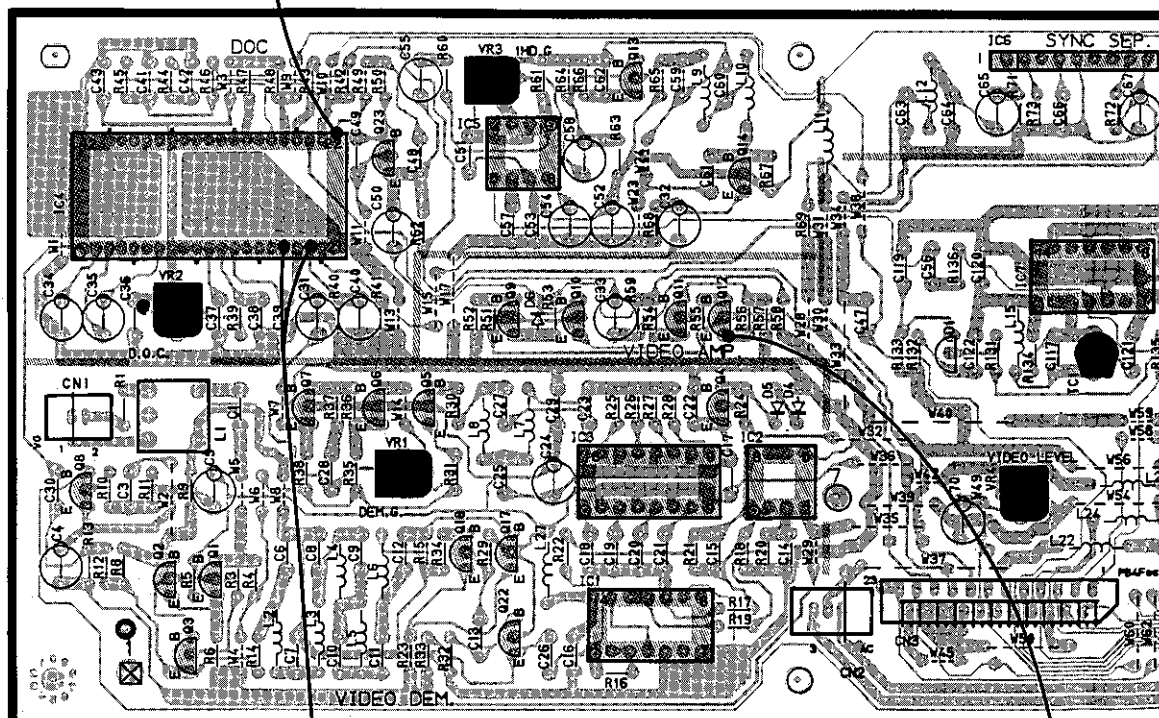
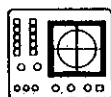
4MHz $\pm$ 50Hz



PC BOARD (COMPONENT SIDE VIEW)

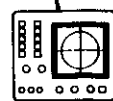


DROP-OUT DETECTION LEVEL :
Set the center of wave-form
from 1.6V to 1.9V DC.

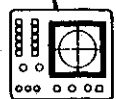
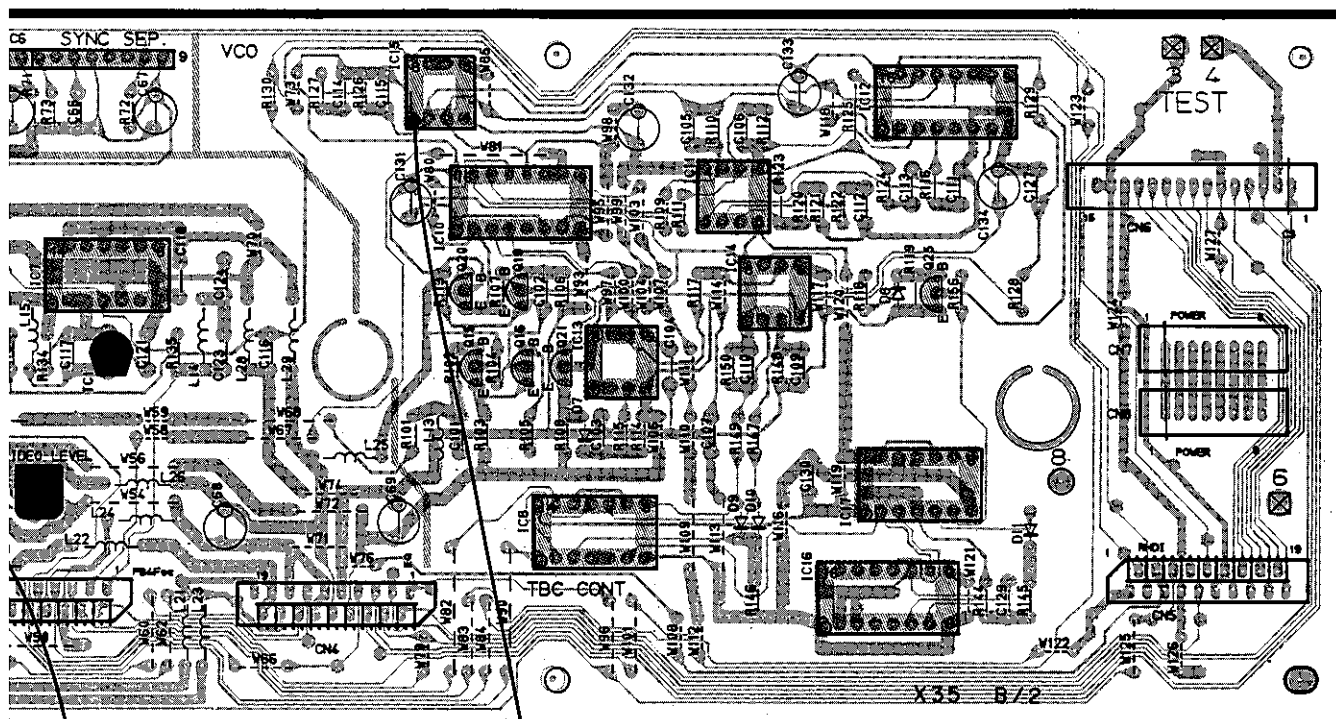
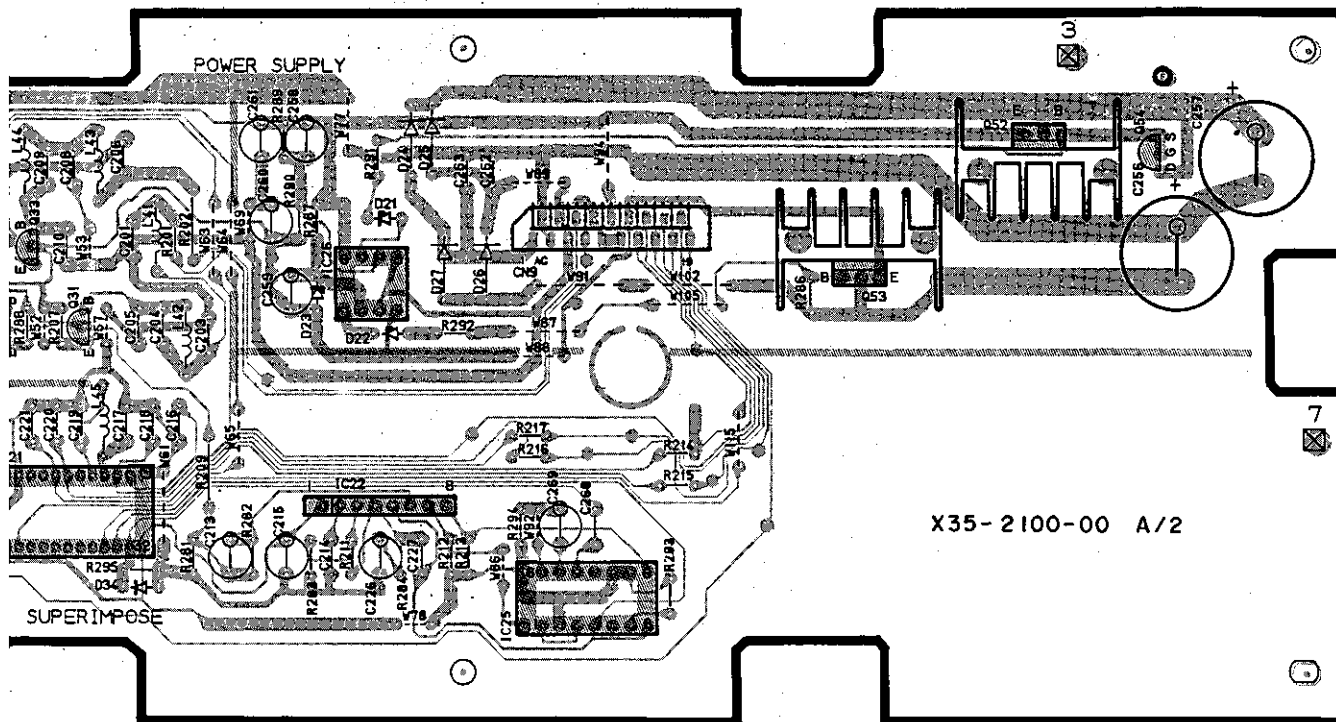


Oscilloscope

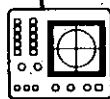
④ DOC GAIN :
No video signal when add CH1 and CH2 signals.



⑤ VIDEO DEMO
Set the video



Oscilloscope



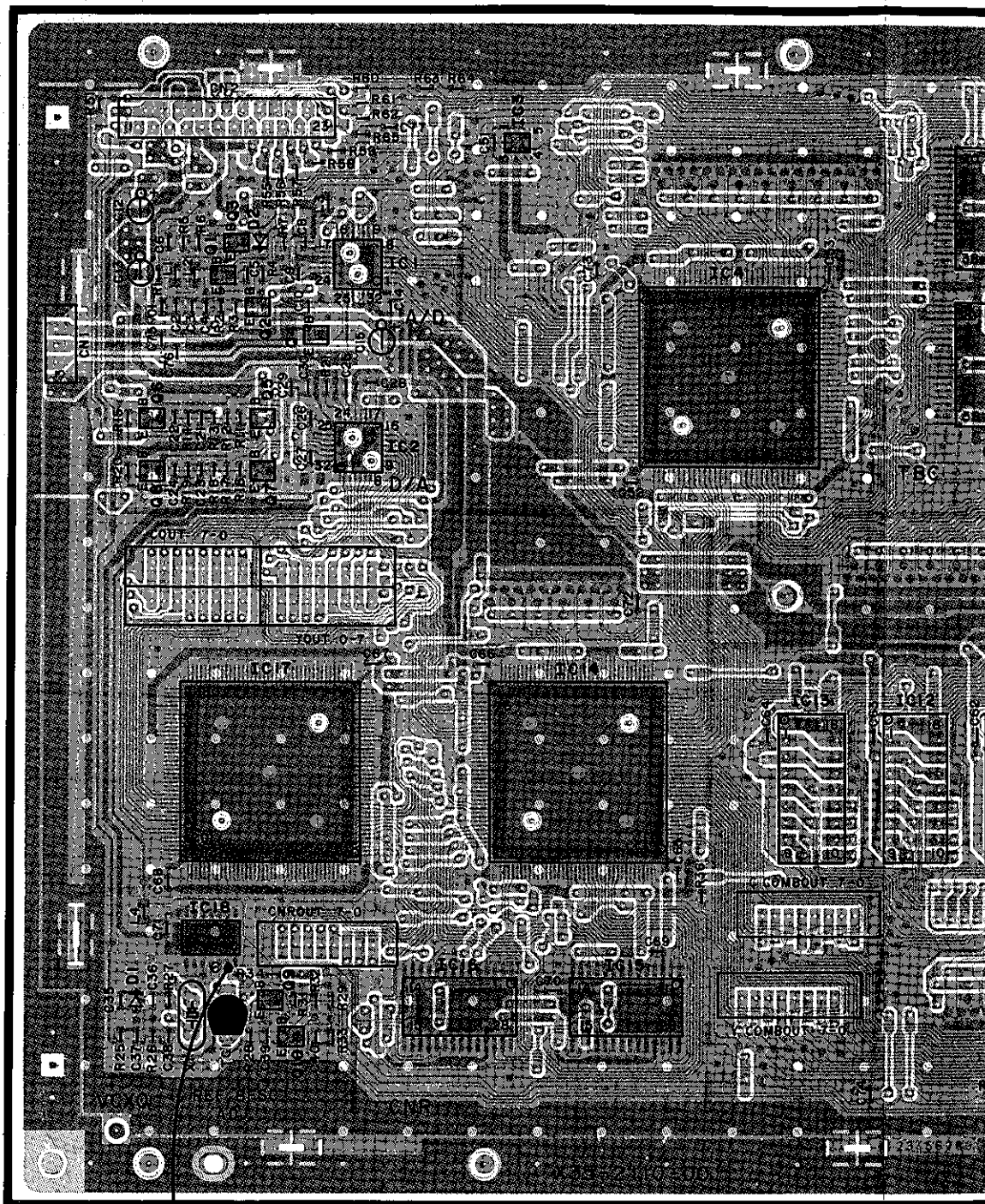
Oscilloscope

④ VCO : DC=0V (mean value).

⑤ VIDEO DEMODULATION LEVEL :
Set the video amplitude to 1.8Vp-p.

Refer to the schematic diagram for the values of resistors and capacitors.

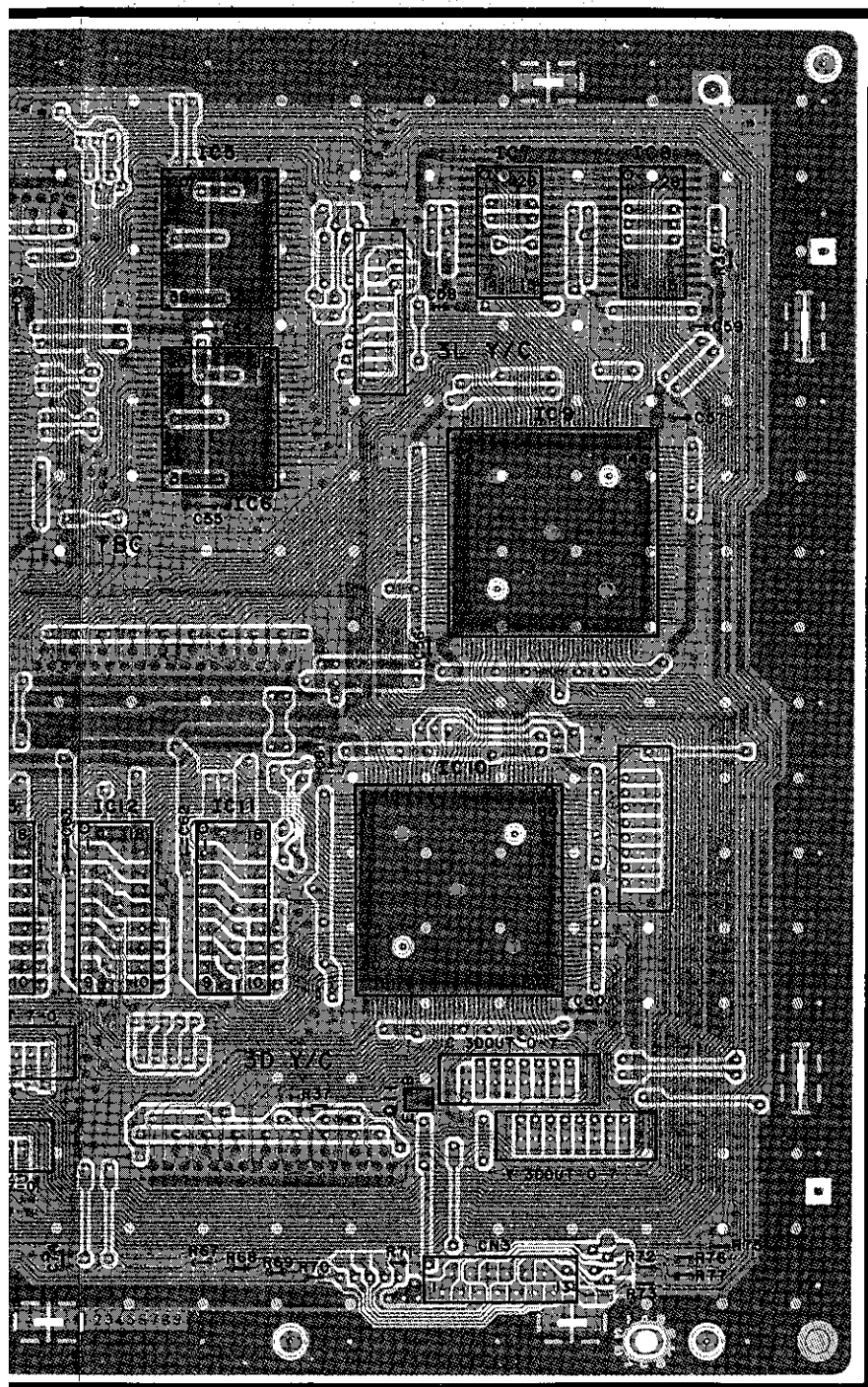
PC BOARD (COMPONENT SIDE VIEW)



Frequency counter

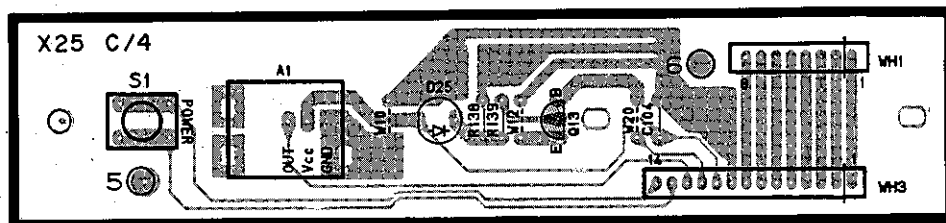
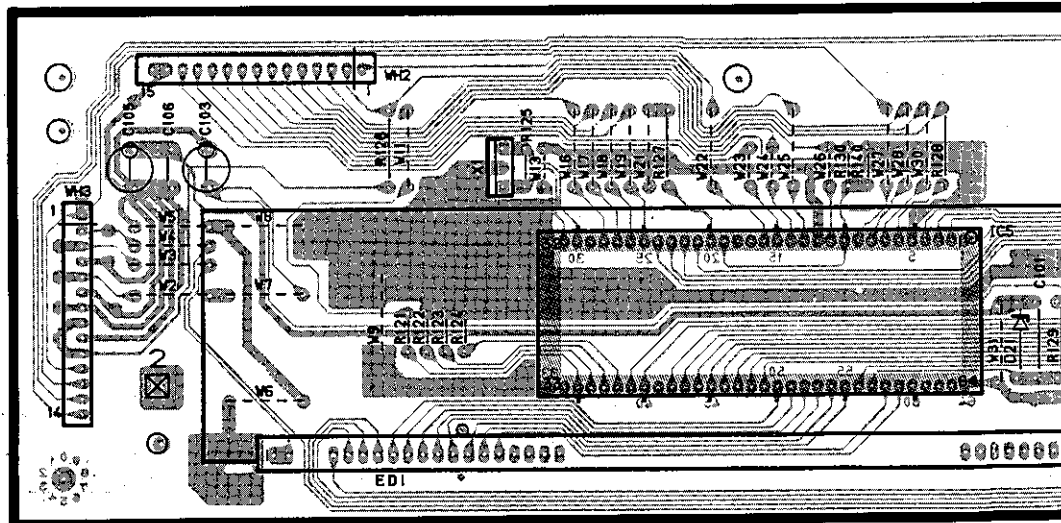
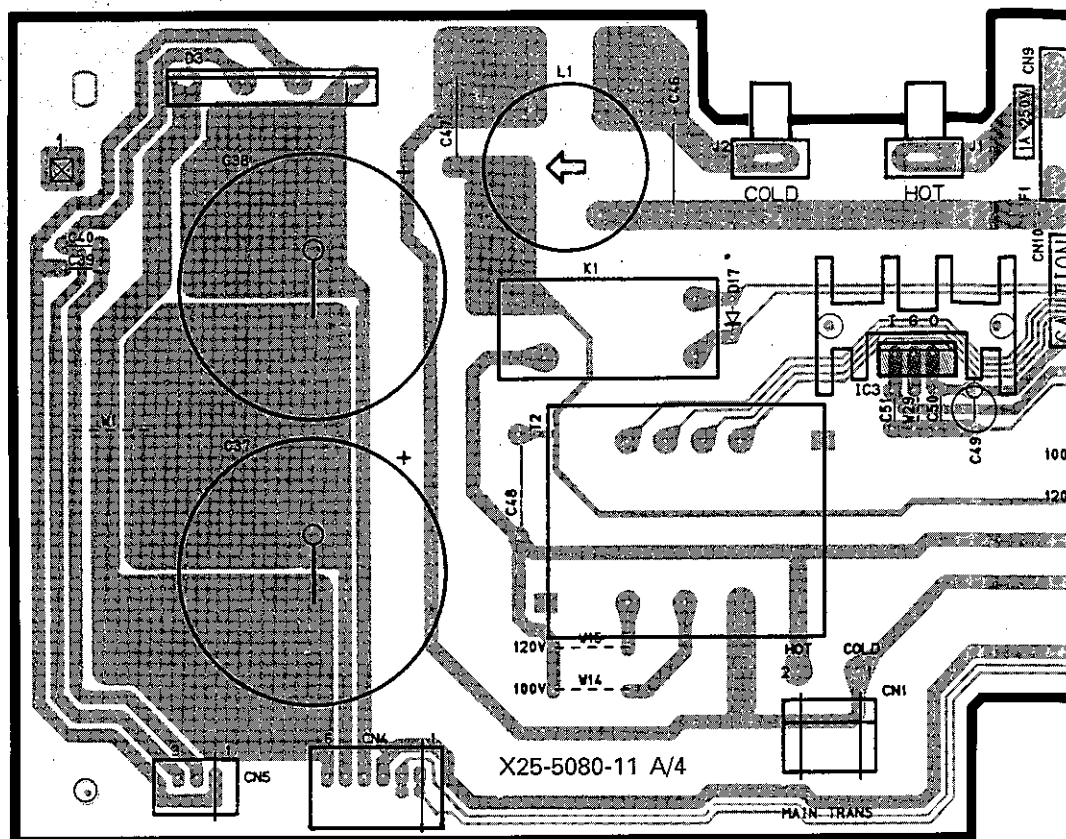
REFERENCE 8fsc : 28.636360MHz $\pm$ 80Hz

Refer

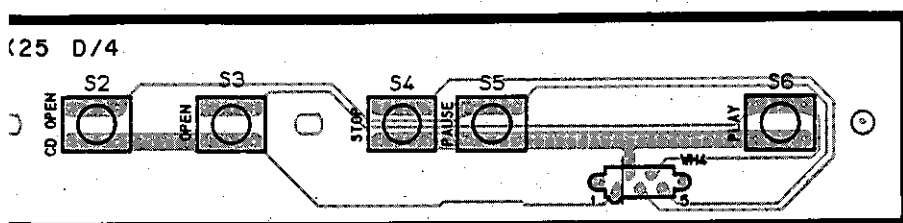
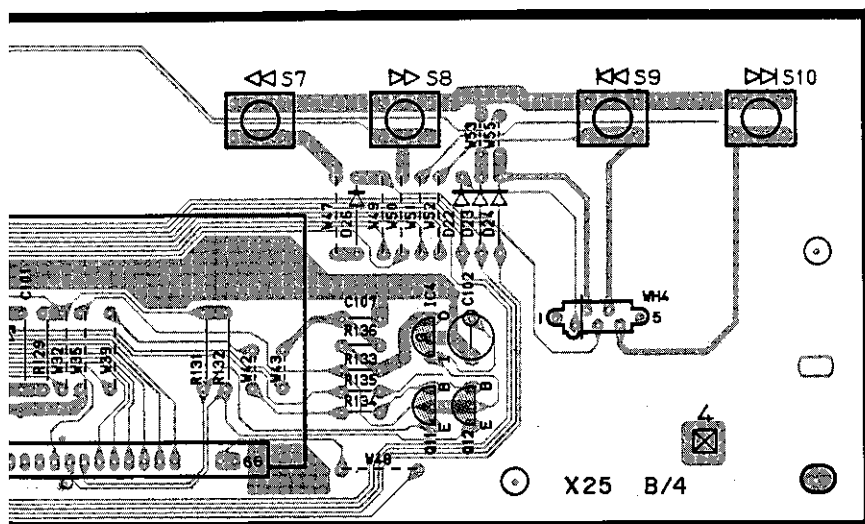
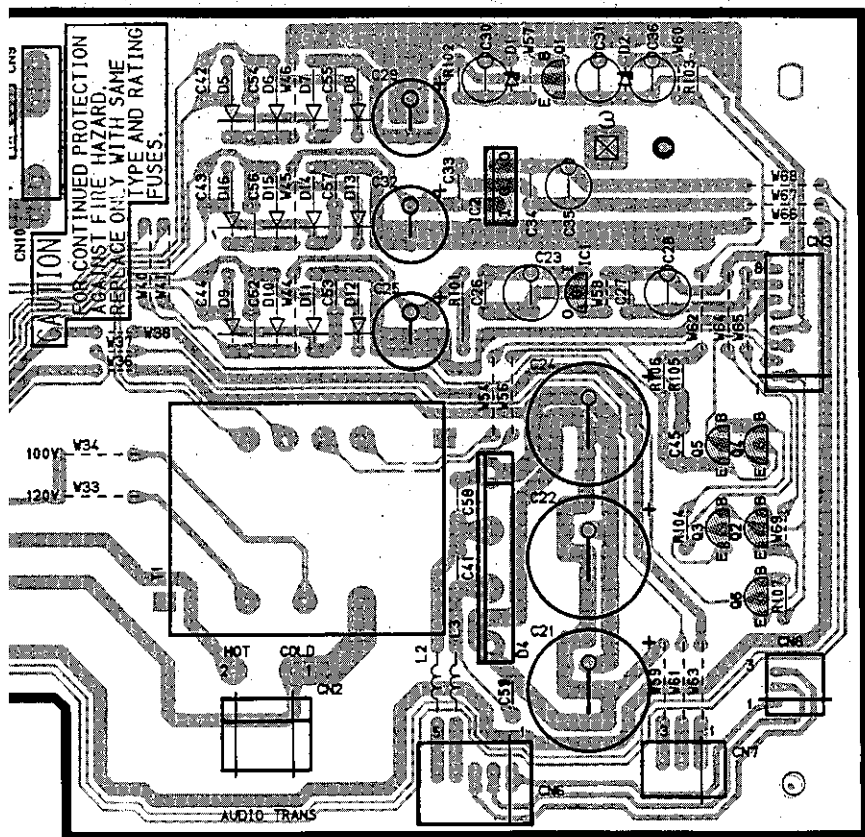


Refer to the schematic diagram for the values of resistors and capacitors.

PC BOARD (COMPONENT SIDE VIEW)



REMOTE
SENSOR



MECHANICAL

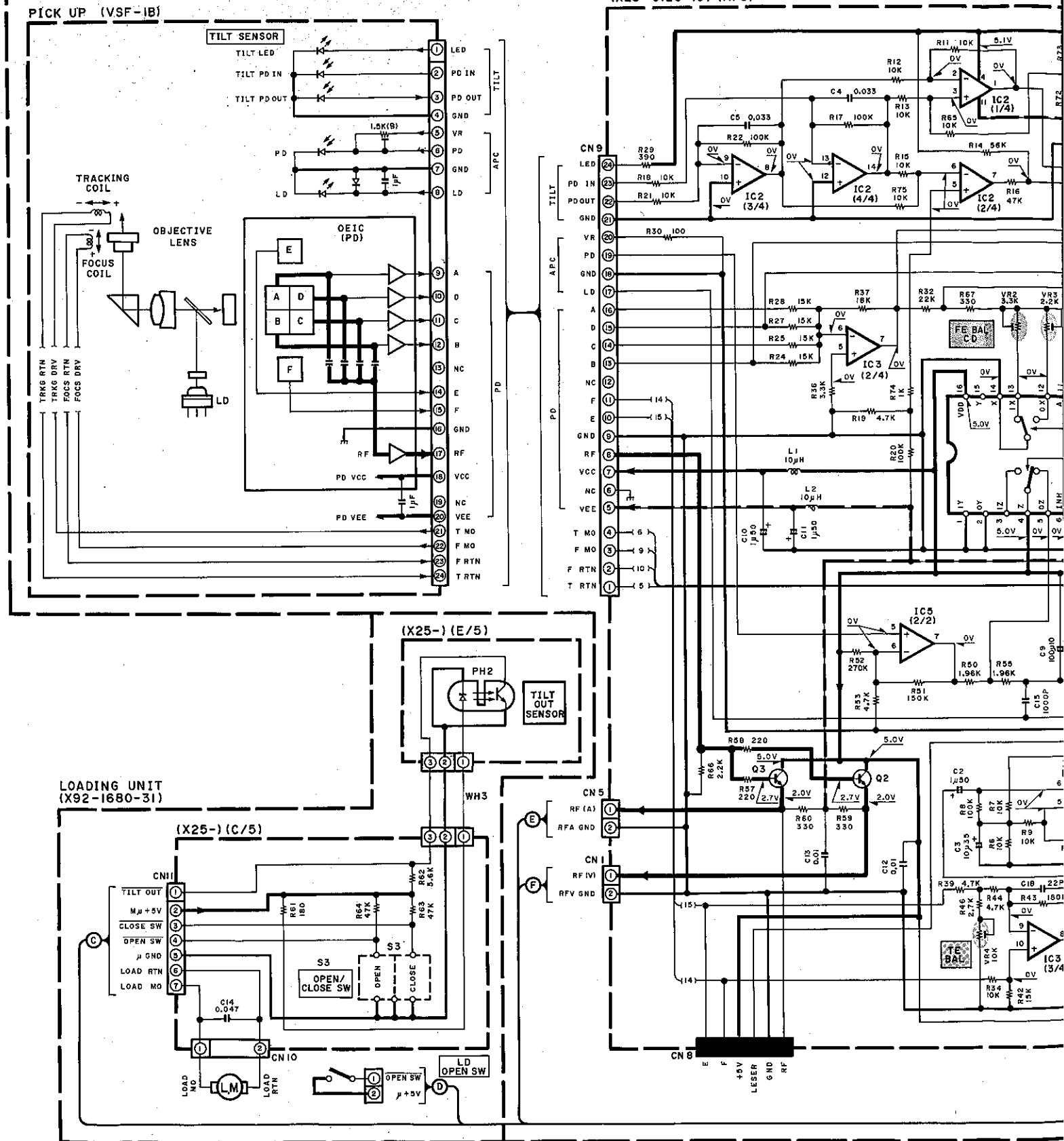
PICK

TRNG RTN
TRNG DRV
FOGS RTN

C1

Refer to the schematic diagram for the values of resistors and capacitors.

ELECTRIC CIRCUIT
(X25-5120-10) (A/5)



CAUTION : For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

- DC voltage or/and u

LVD-Z1(1/7)

Q1 : 2SA1110(R,S)
Q2,3 : 2SC3311A(Q,R) or 2SC2458(Y,GR)

IC1 : BA10393
IC2,3 : NJM2058D or μ PC4574C
IC4 : XRU4053B
IC5 : NJM4565D

— SIGNAL LINE
— GND LINE
— +B LINE
— -B LINE

X29-CN7

2/7

A

DISC MOTOR
(X92-1620-41)

X29-CN1

2/7

B

X29-CN5

2/7

C

X29-CN4

2/7

D

X32-A/2-CN1

3/7

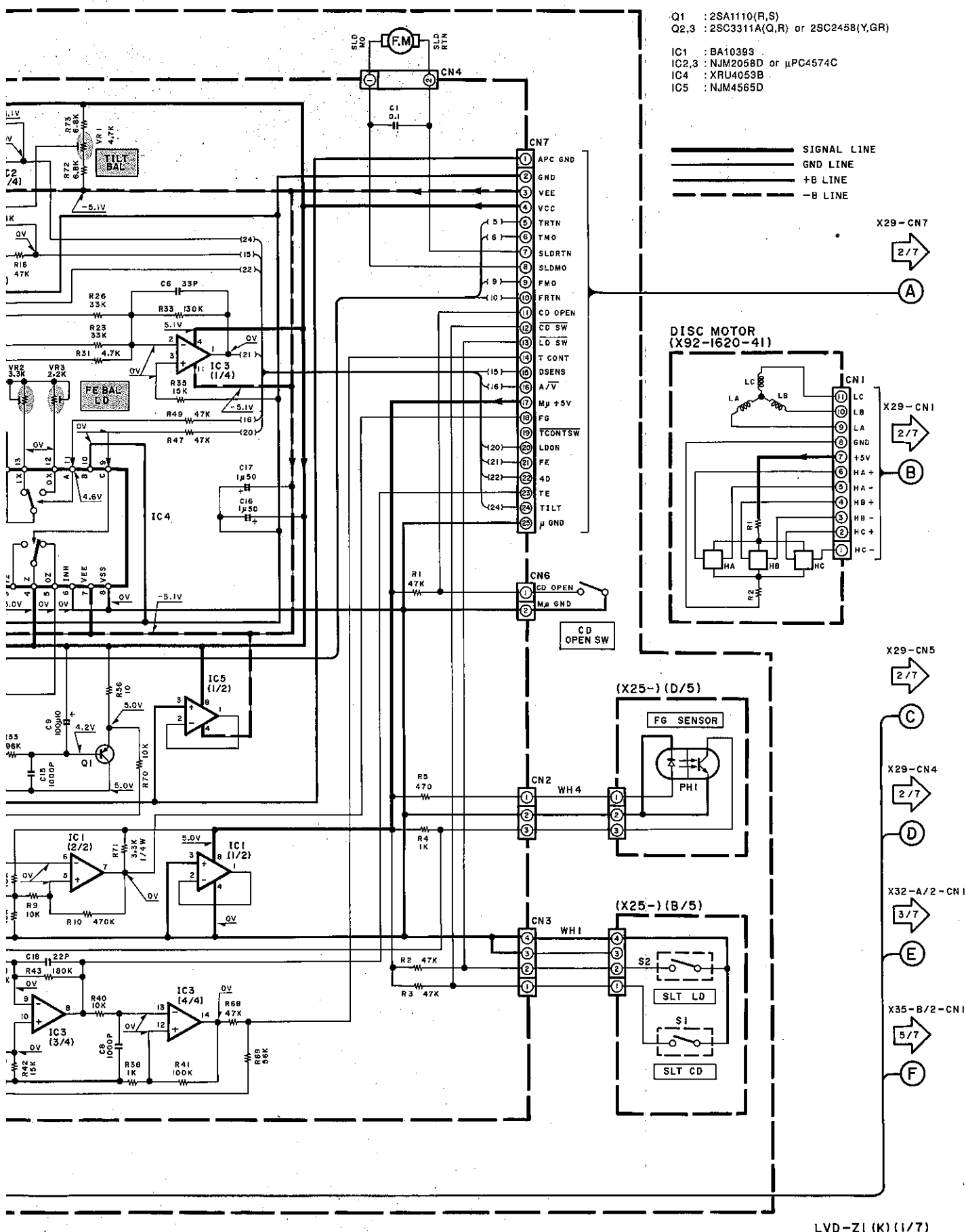
E

X35-B/2-CN1

5/7

F

LVD-Z1 (K) (1/7)



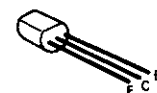
DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

LVD-Z1(1/7)

Q1 : 2SA1110(R,S)
 Q2,3 : 2SC3311A(Q,R) or 2SC2458(Y,GR)

IC1 : BA10393
 IC2,3 : NJM2058D or μ PC4574C
 IC4 : XRU4053B
 IC5 : NJM4565D

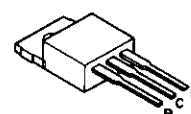
2SA954 2SC3246
 2SA992 2SC3940A
 2SC1923 2SD1302
 2SC2003



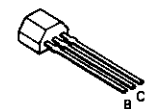
2SA1110
 2SB772
 2SD882



2SC4064



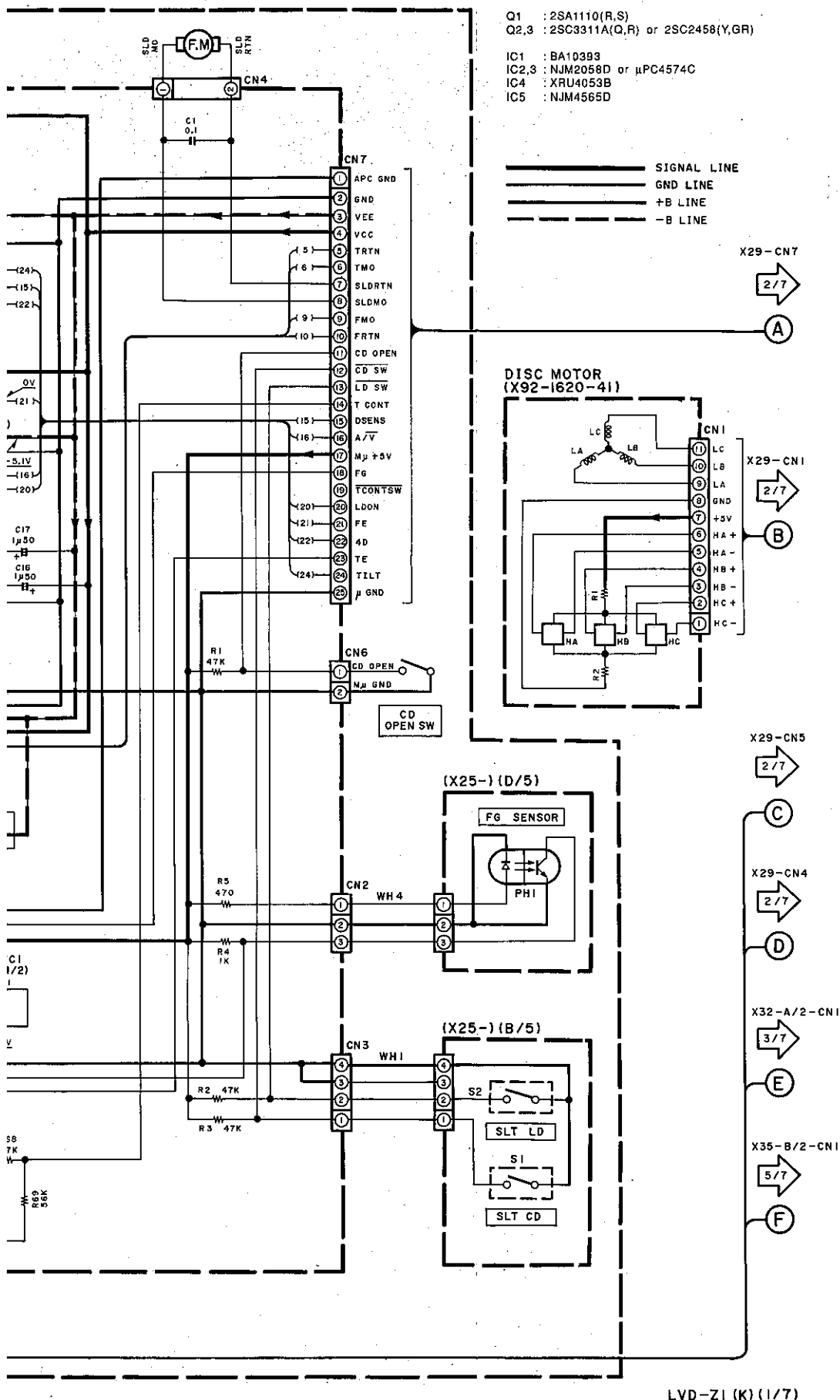
DTA124ES 2SA1048
 DTC124ES 2SC2458
 UN4112



2SA1535A
 2SC3944A



DTC124EK
 2SA1037K
 2SC2412K



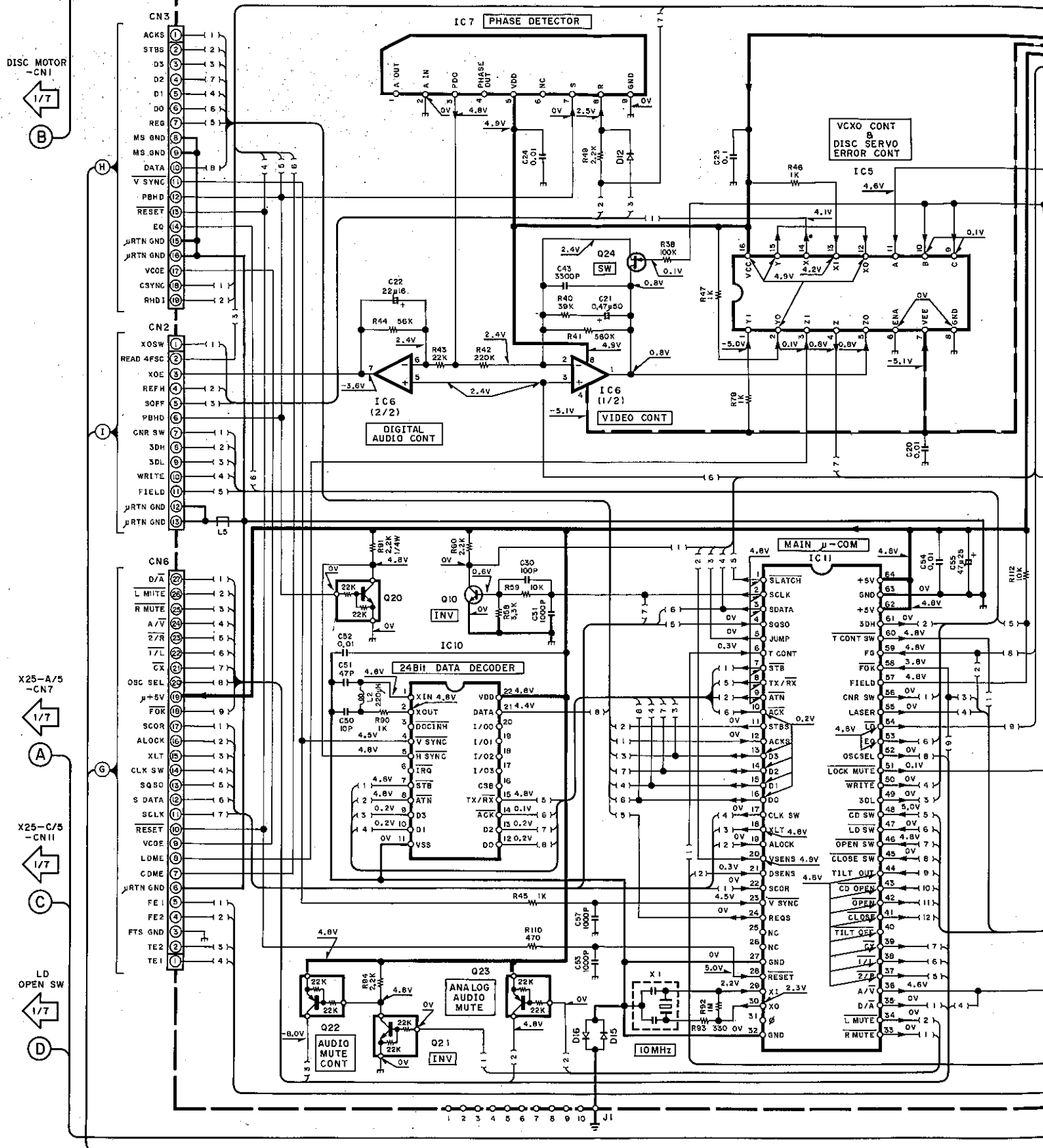
LVD-Z1 (K) (1/7)

a high impedance voltmeter. Values may vary slightly due to variations between individual instruments

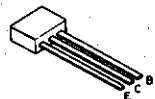
Y22-3110-11

LVD-Z1
KENWOOD

FTS DISC SERVO UNIT (X29-2380-00)



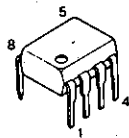
UN4212
2SA1309A
2SC3311A



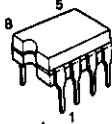
2SB1375
2SB1548
2SD2012
2SD2374



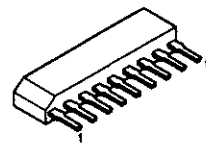
NJM4560D-N
NJM5532D



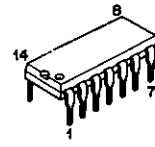
NJM4565D

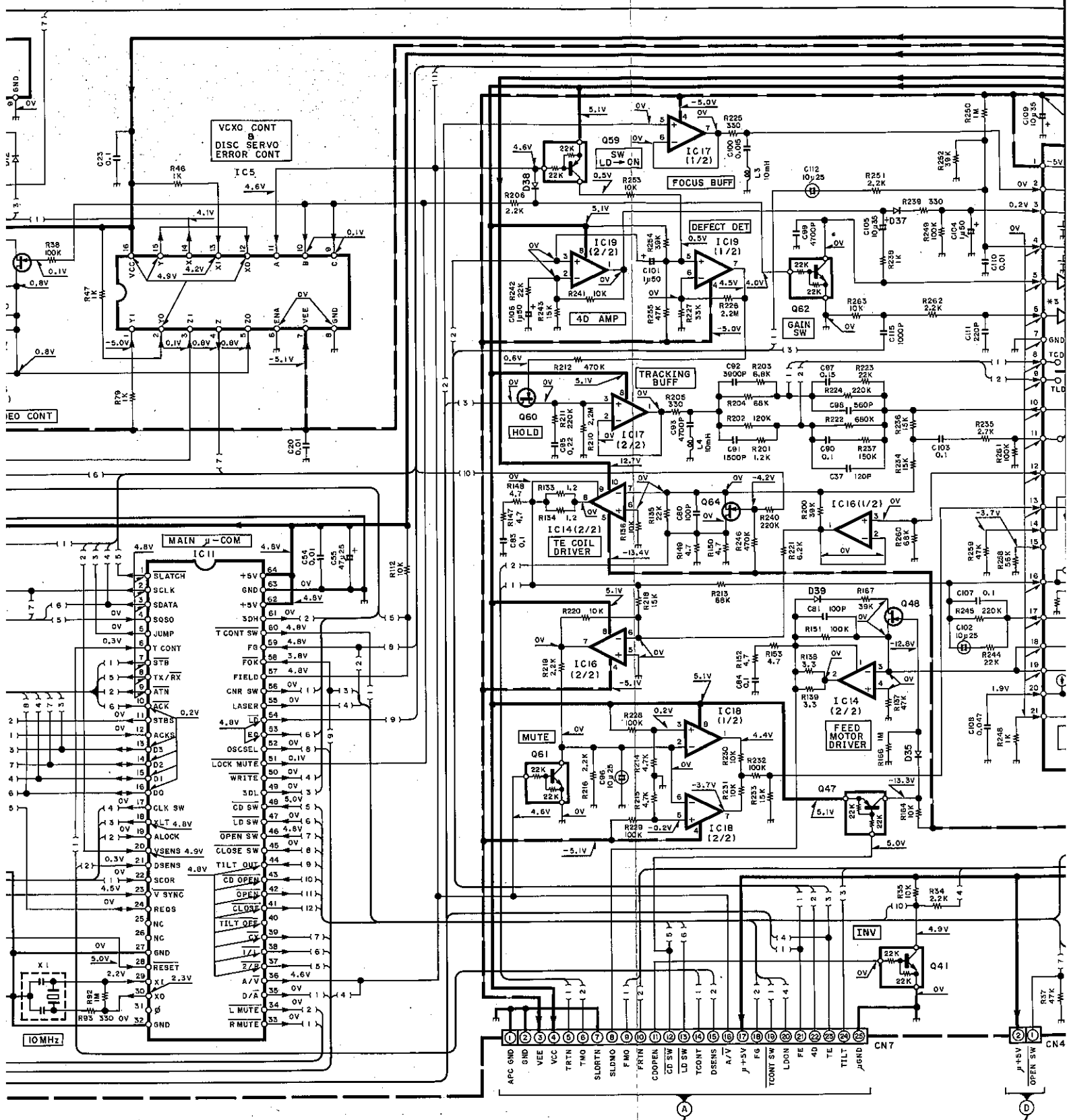


TC5081AP

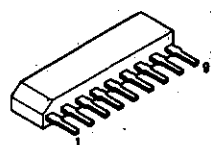


NJM2058D

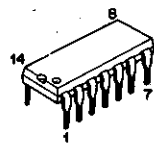




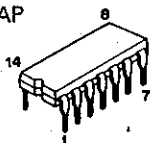
TC5081AP



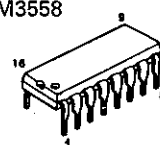
NJM2058D



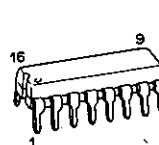
TC74HCU04AP
TC74HC00AP
TC74HC74AP
UPC4574C



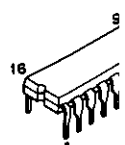
XRU4053B
YM3558

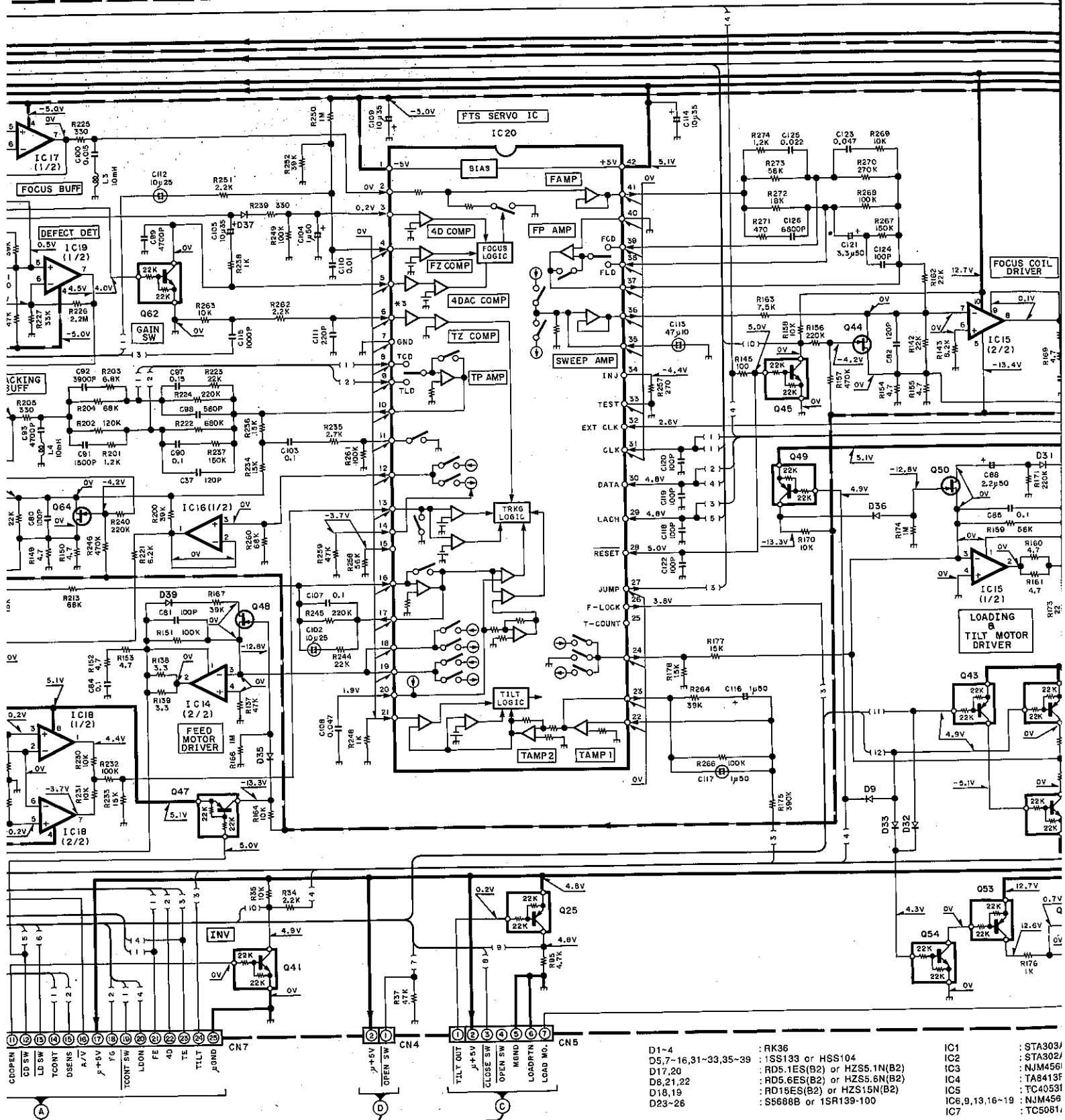


TC74HC123AP



TC4053BP



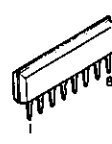
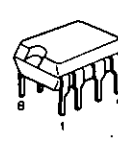
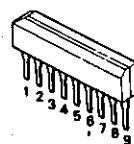
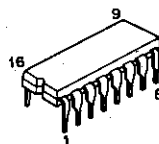
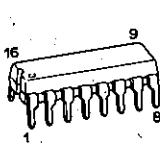
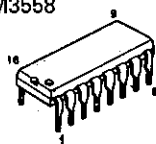
RU4053B
M3558

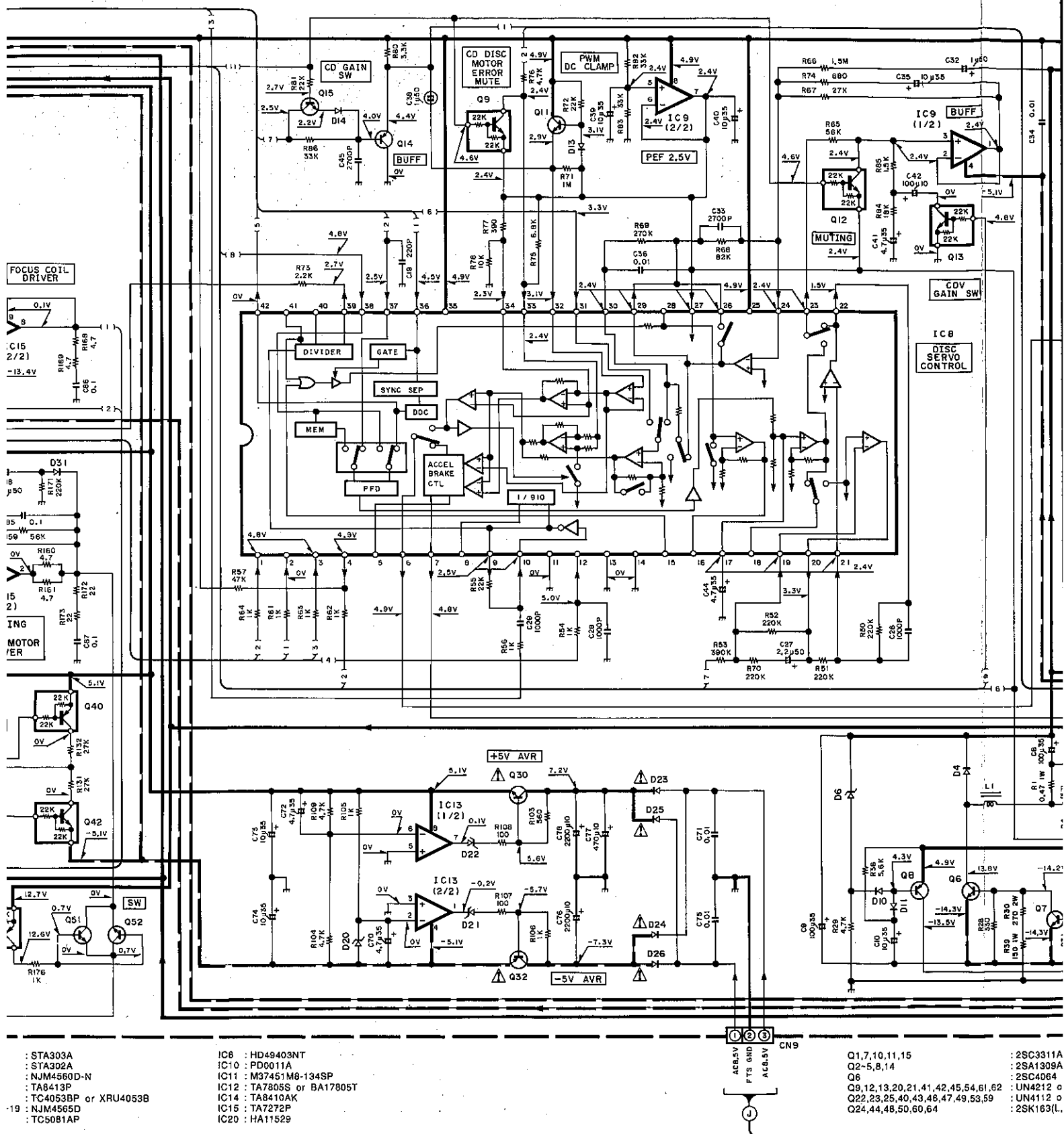
TC74HC123AP

TC4053BP

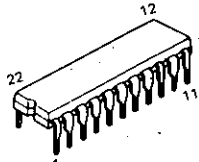
LVA519S

BA10393

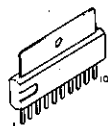
STA302A
STA303A



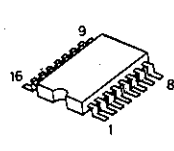
PD0011A



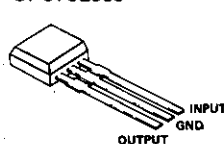
TA8410AK



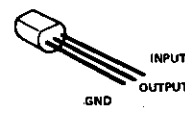
TC74HC4538AF



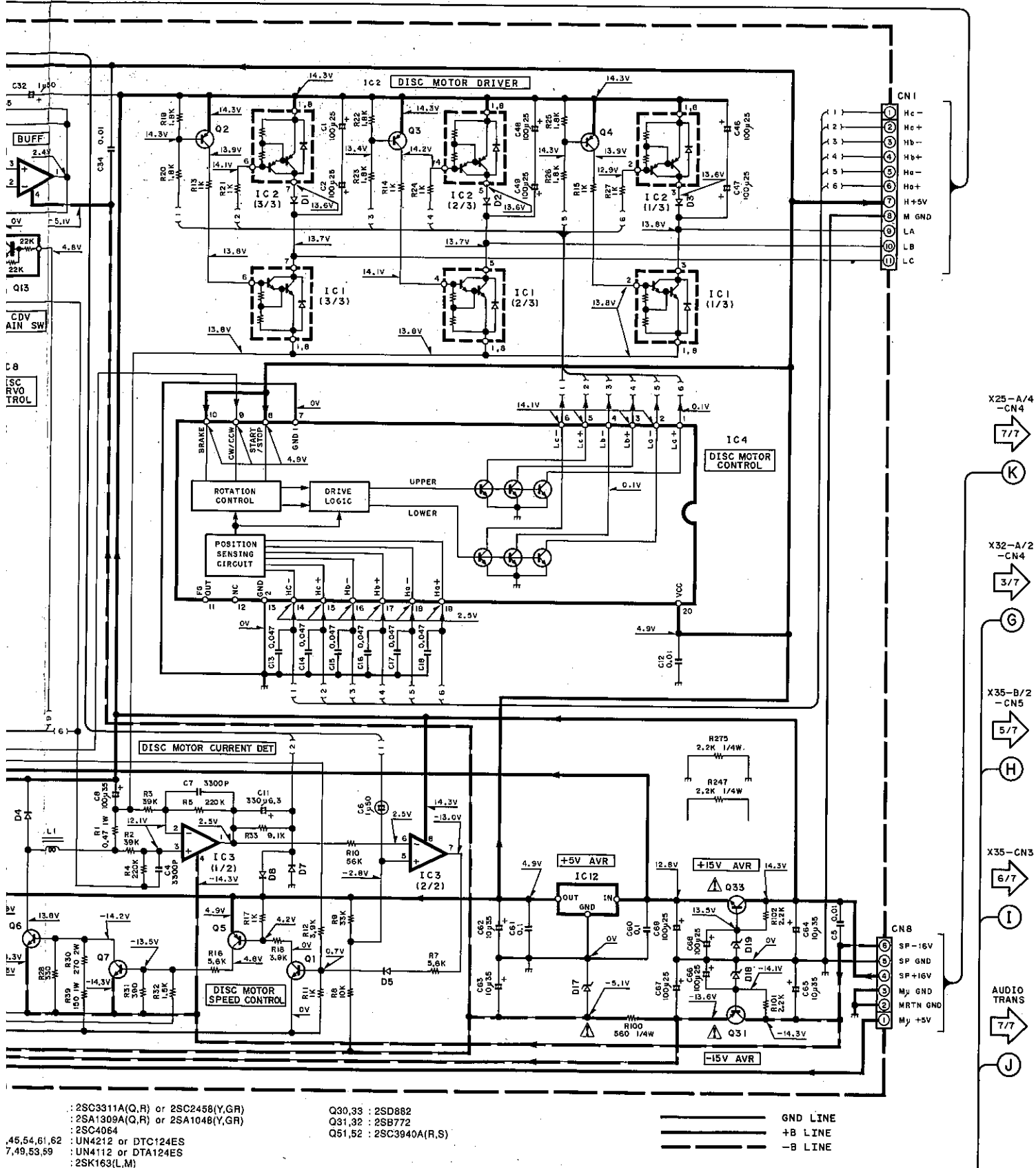
UPC78L05J



PST529C



CAUTION: For contents only with main parts list). Δ Indicate the risk of electric shock. Measurements shall be calculated from the supply to the customer.



LVD-Z1 (K) (2/7)

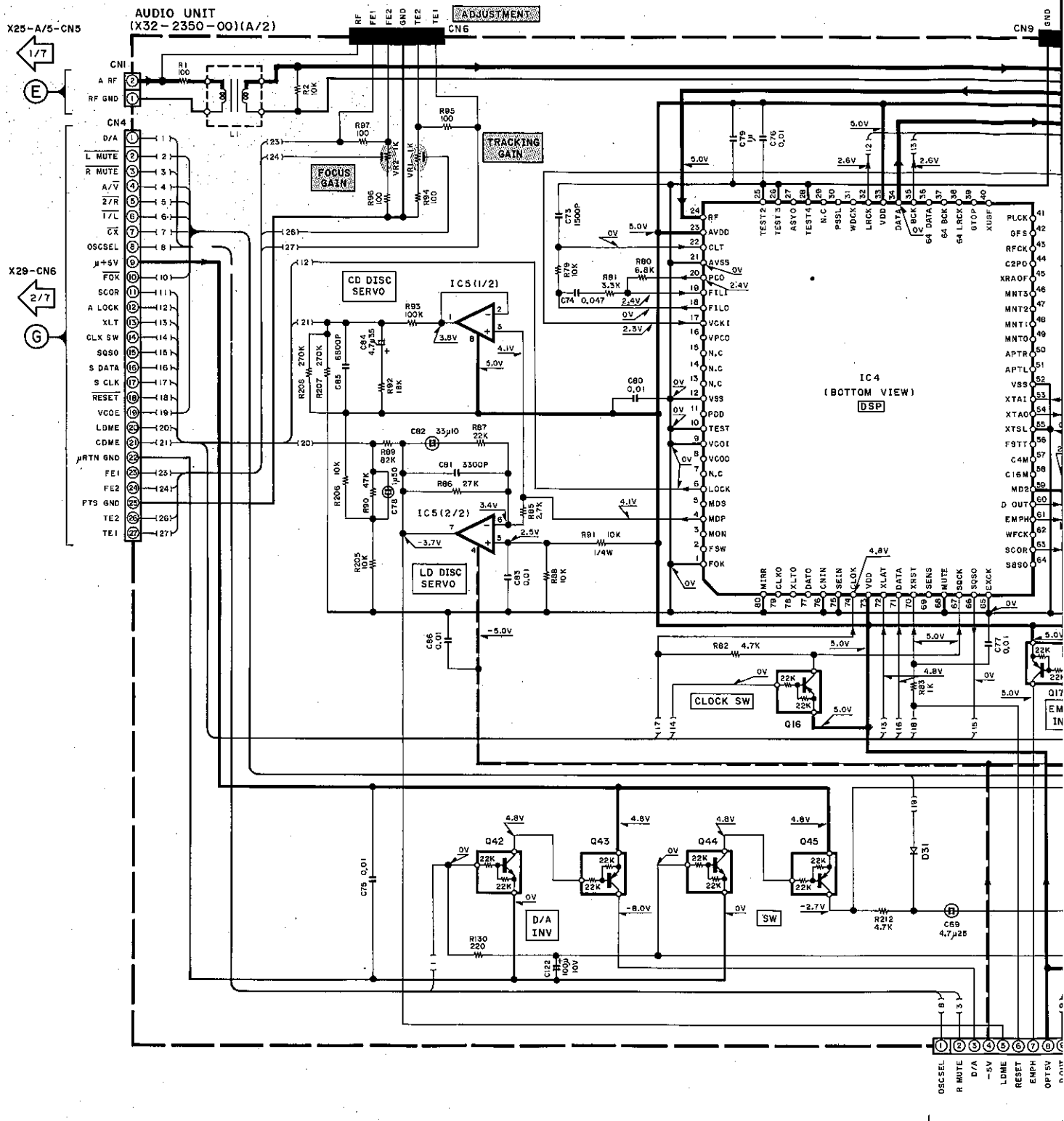
CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). Δ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

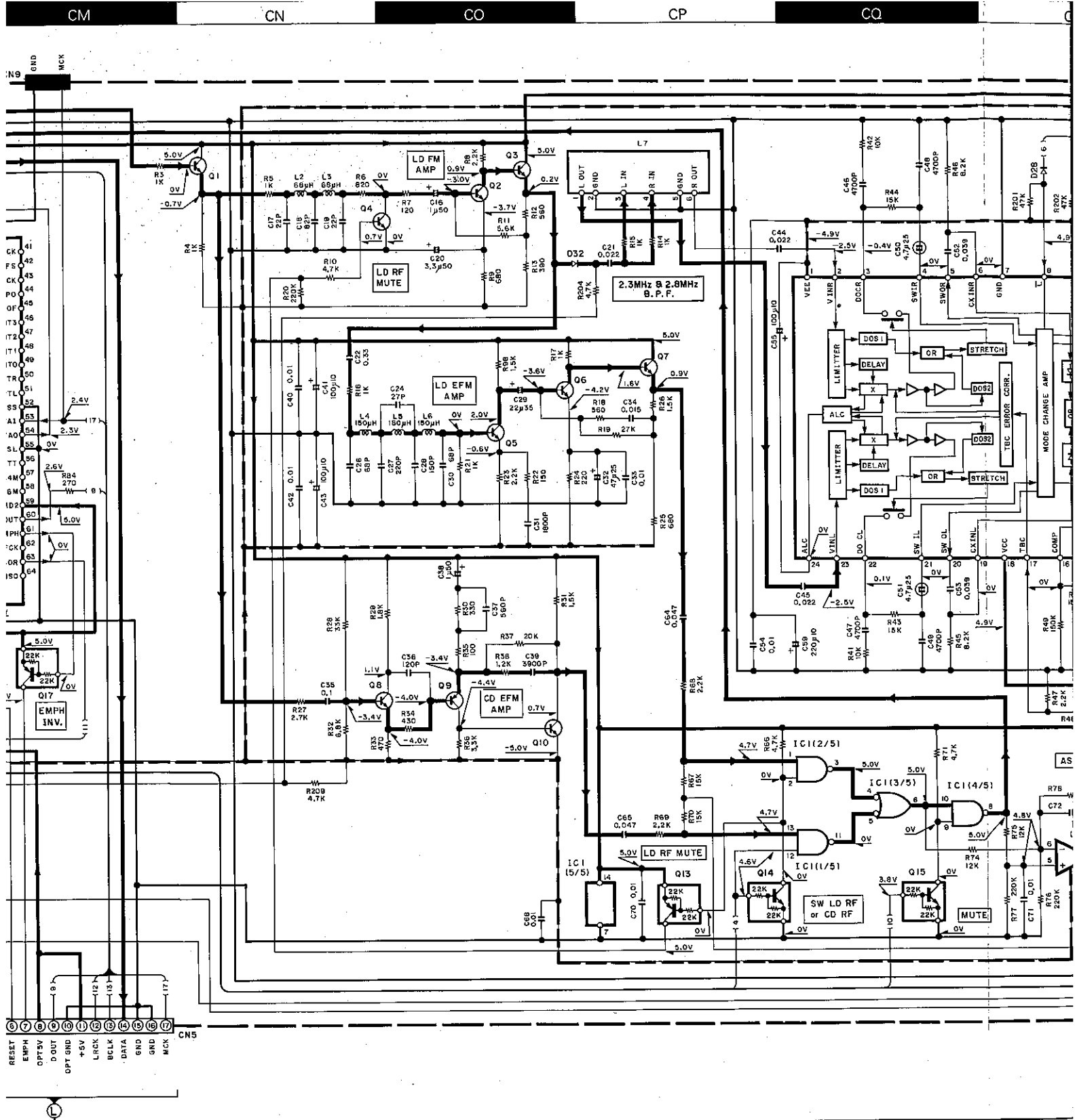
- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

Y22-3110-11

LVD-Z1

KENWOOD

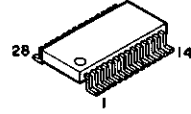
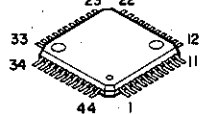
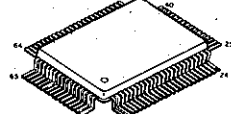
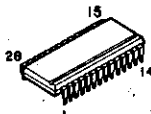




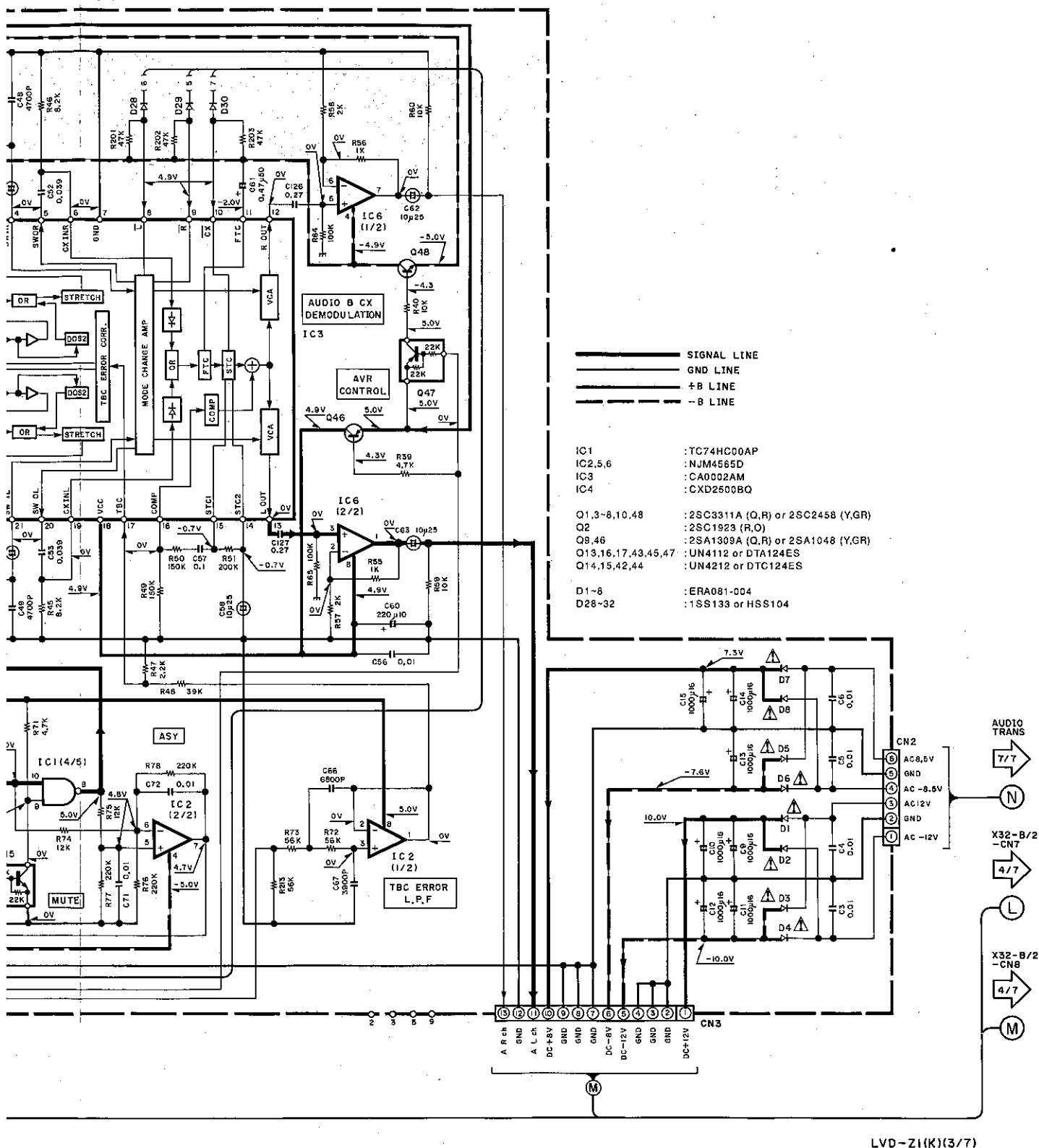
SM5813APT

CXD2500BQ

SAA7350



CAUTION
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CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). Δ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

• DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

Y22-3110-11

LVD-Z1

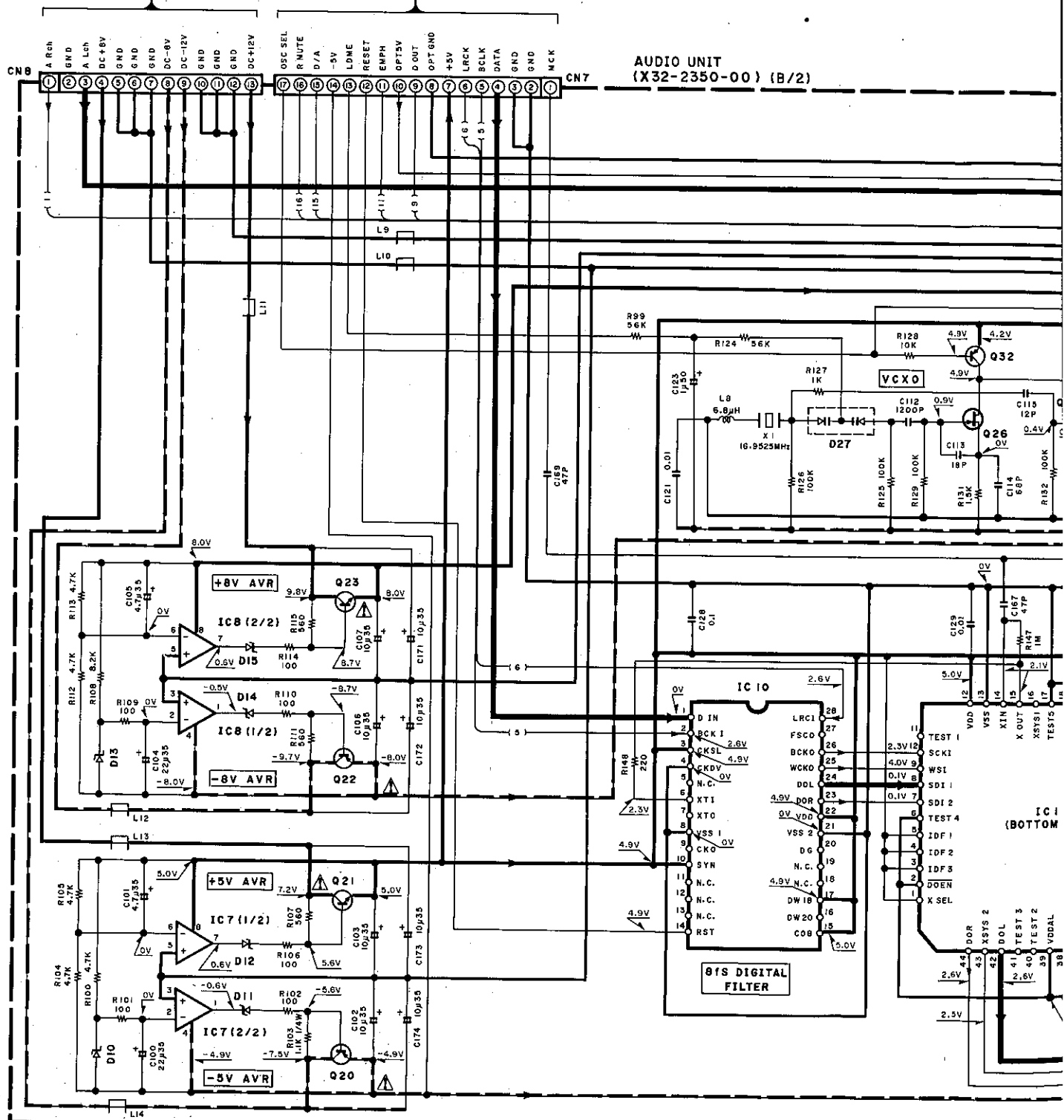
KENWOOD

X32-A/2-CN5



④

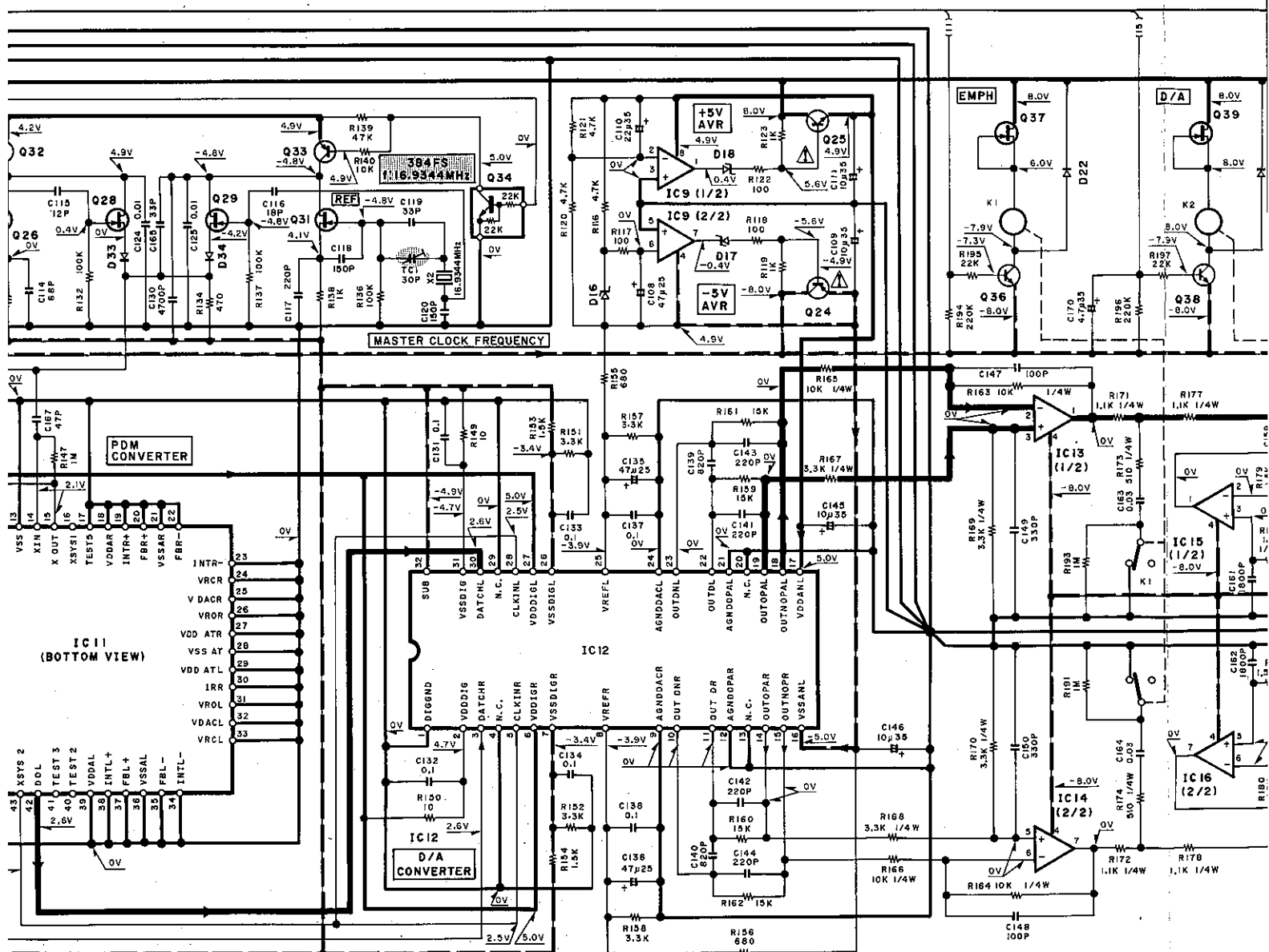
X32-A/2-CN3



——— SIGNAL LINE
 ——— GND LINE
 ——— +B LINE
 ——— -B LINE

IC7-9 : NJM4565L
 IC10 : SM5813APT
 IC11 : SAA7350
 IC12 : TDA1547
 IC13-16 : NJM5532D

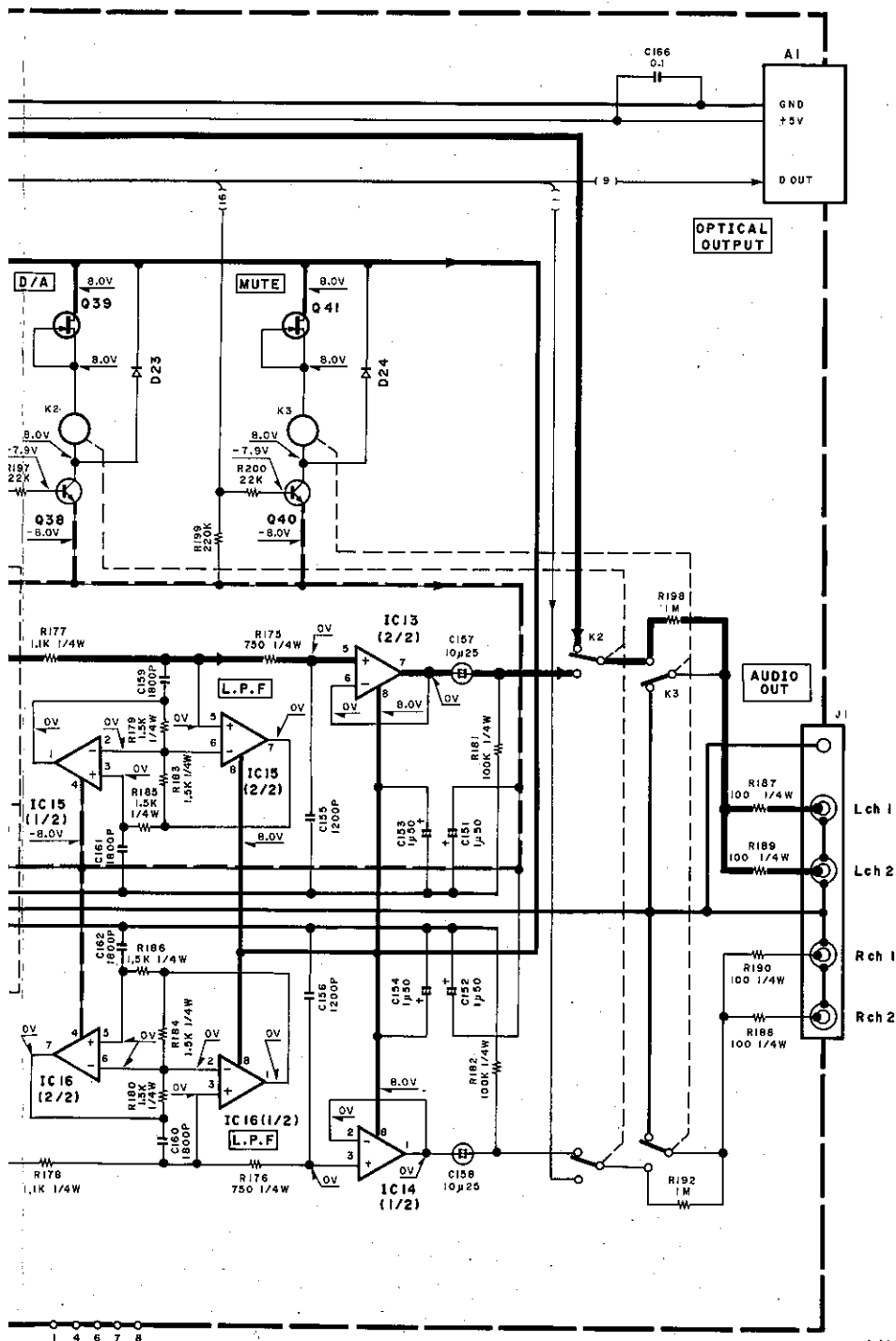
Q20,22 : 2SA1535A
 Q21,23 : 2SC3944A
 Q24 : 2SA954 (L,K)
 Q25 : 2SC2003 (L,K)
 Q26,28,29,31 : 2SK709 (BL,V)
 Q32,33 : 2SA1309A (Q,R) or 2SA1048 (Y,G)
 Q34 : DTC124ES or UN4212
 Q36,38,40 : 2SC3311A (Q,R) or 2SC2458 (Y,G)
 Q37,39,41 : 2SK163 (N)



(R) or 2SA1048 (Y,GR)
UN4212
(R) or 2SC2458 (Y,GR)

D10~12,16~18 : RD5.1JS (B2) or HZS5.1S (B2)
D13~15 : RD8.2JS (B2) or HZS8.2S (B2)
D22~24,33,34 : 1SS133 or HSS104
D27 : 1SV147

A1 : W02-1114-05



- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

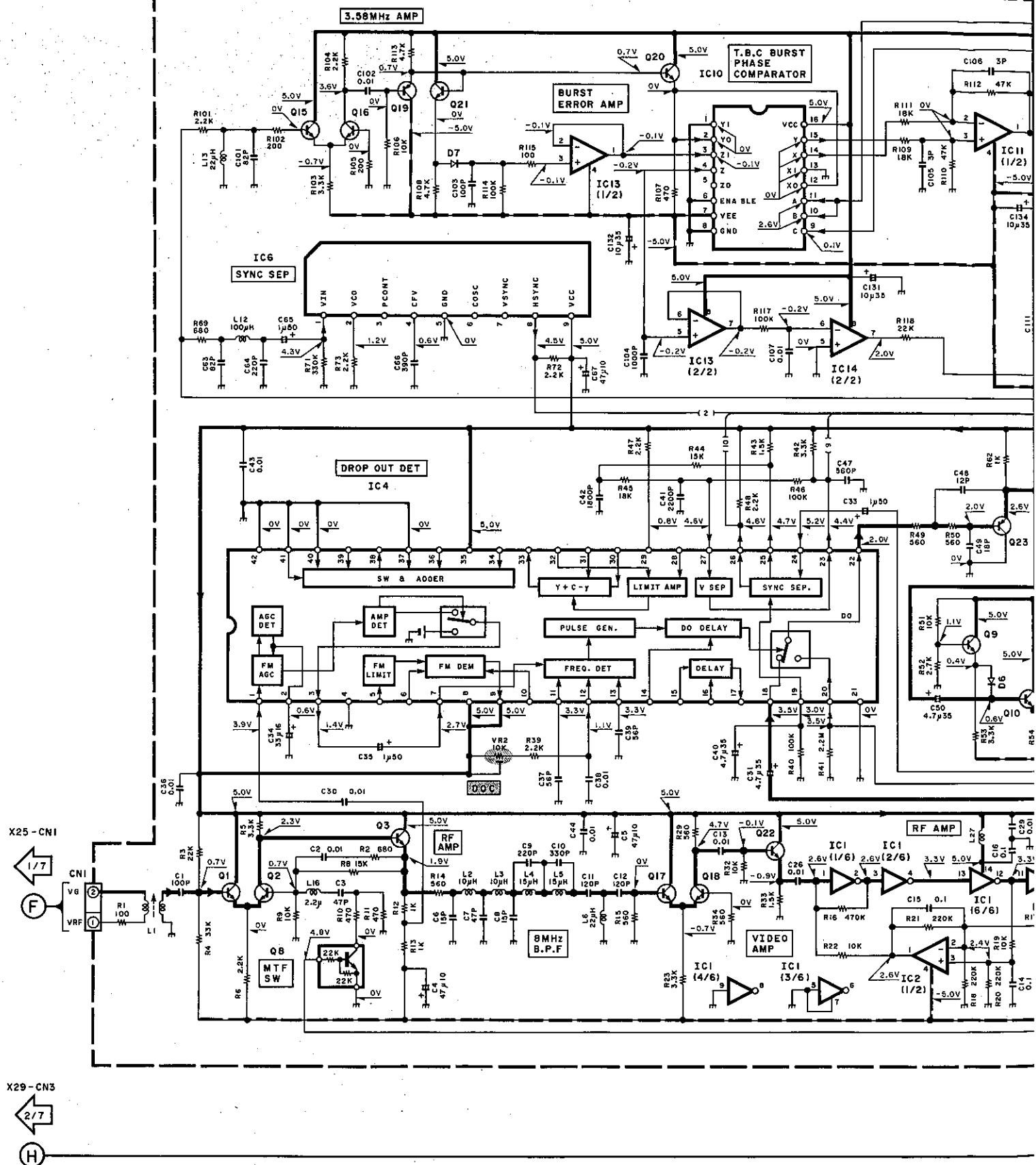
CAUTION : For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). Δ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

LVD-Z1 (K) (4/7)

Y22-3110-11

LVD-Z1
KENWOOD

VIDEO UNIT (X35-2100-00) (B/2)



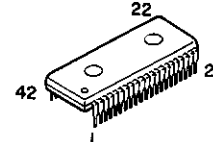
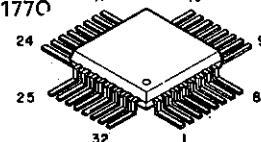
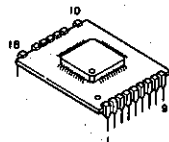
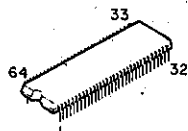
μPD75216ACW-W44

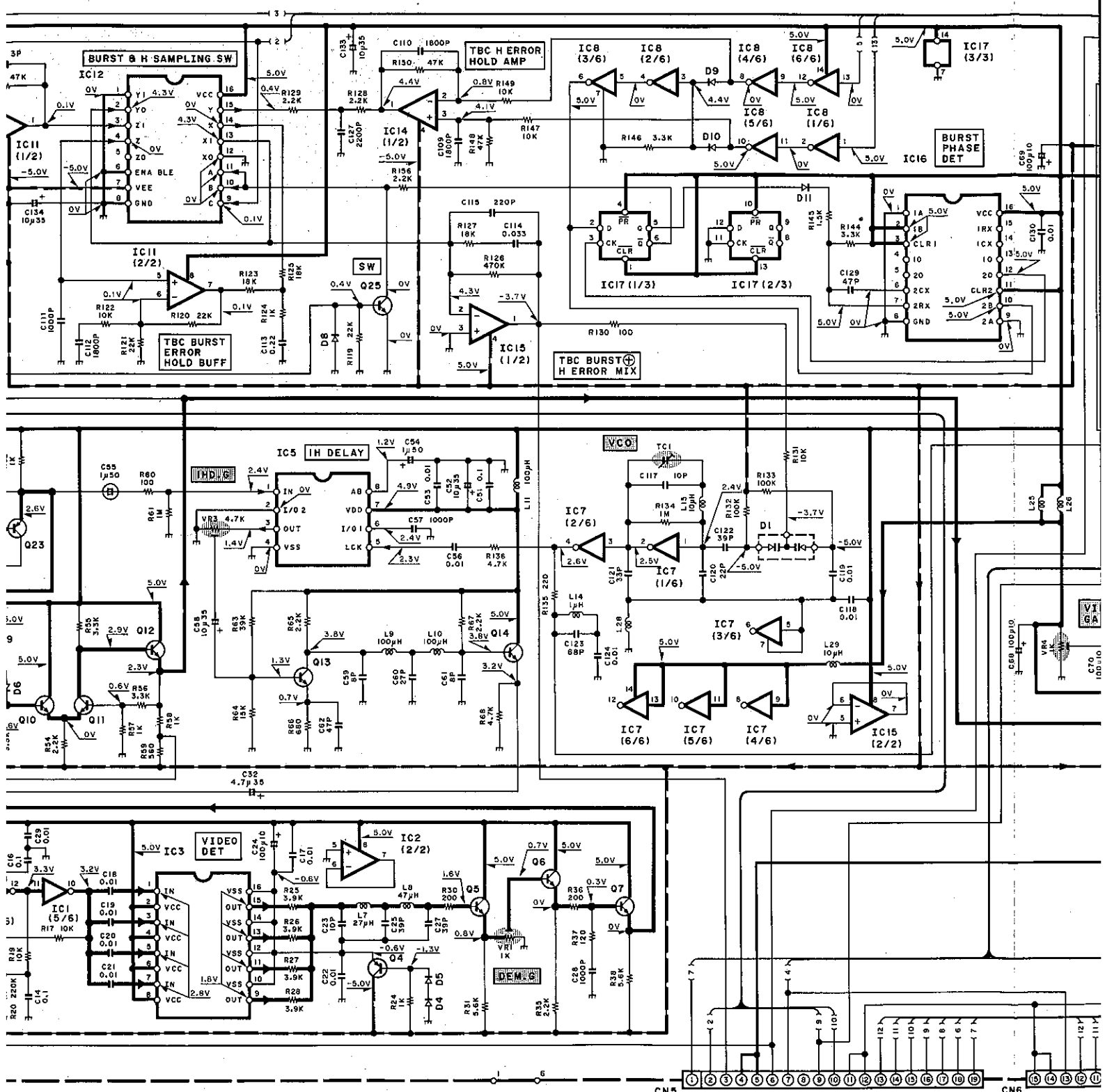
TA78DL05S

TA7805S
UPC2405HFCXD1176Q
CXD1177Q

HA11528

NJM



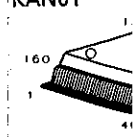
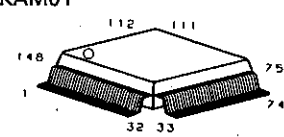
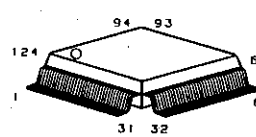
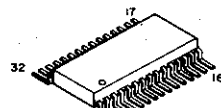
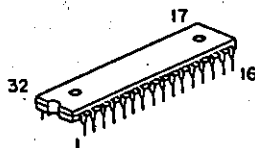
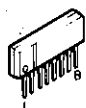


NJM4565L

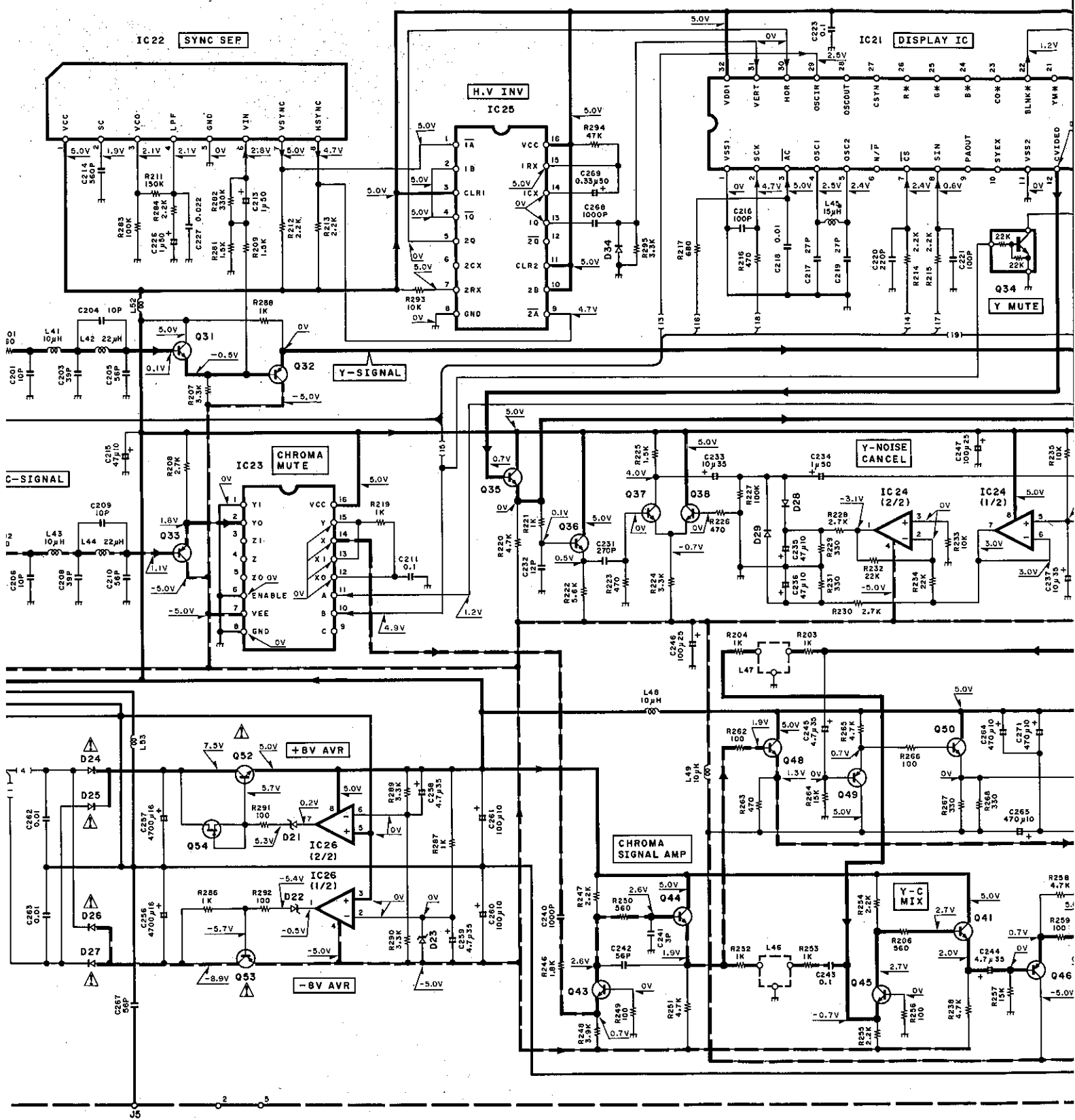
TDA1547

CXK1206AM

KAG03

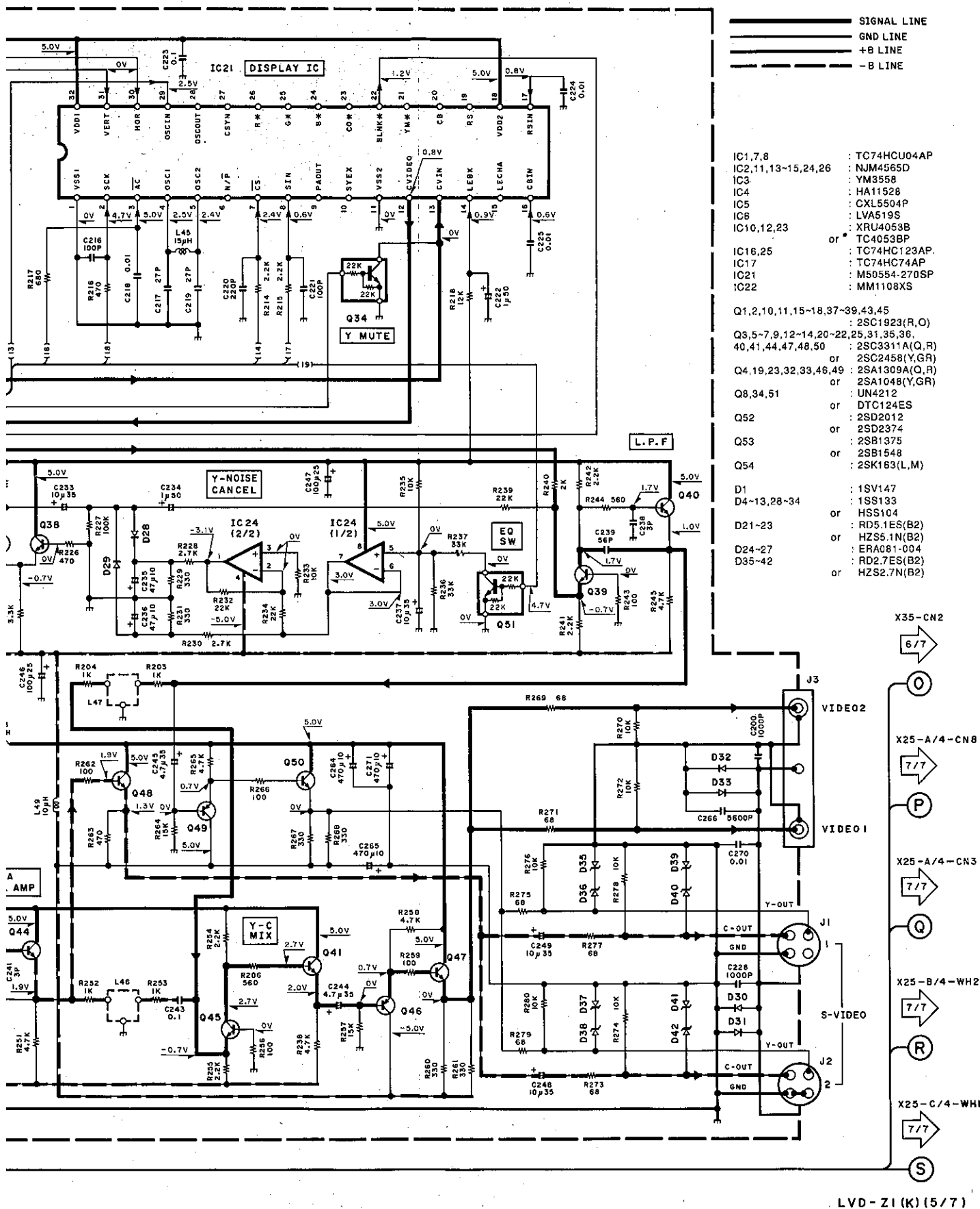
KAG04
KAM01KAG05
KAN01

CAUTION
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CAUTION: For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). Δ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

• DC voltages are as measured with ter. Values may vary slightly d individual instruments or/and un



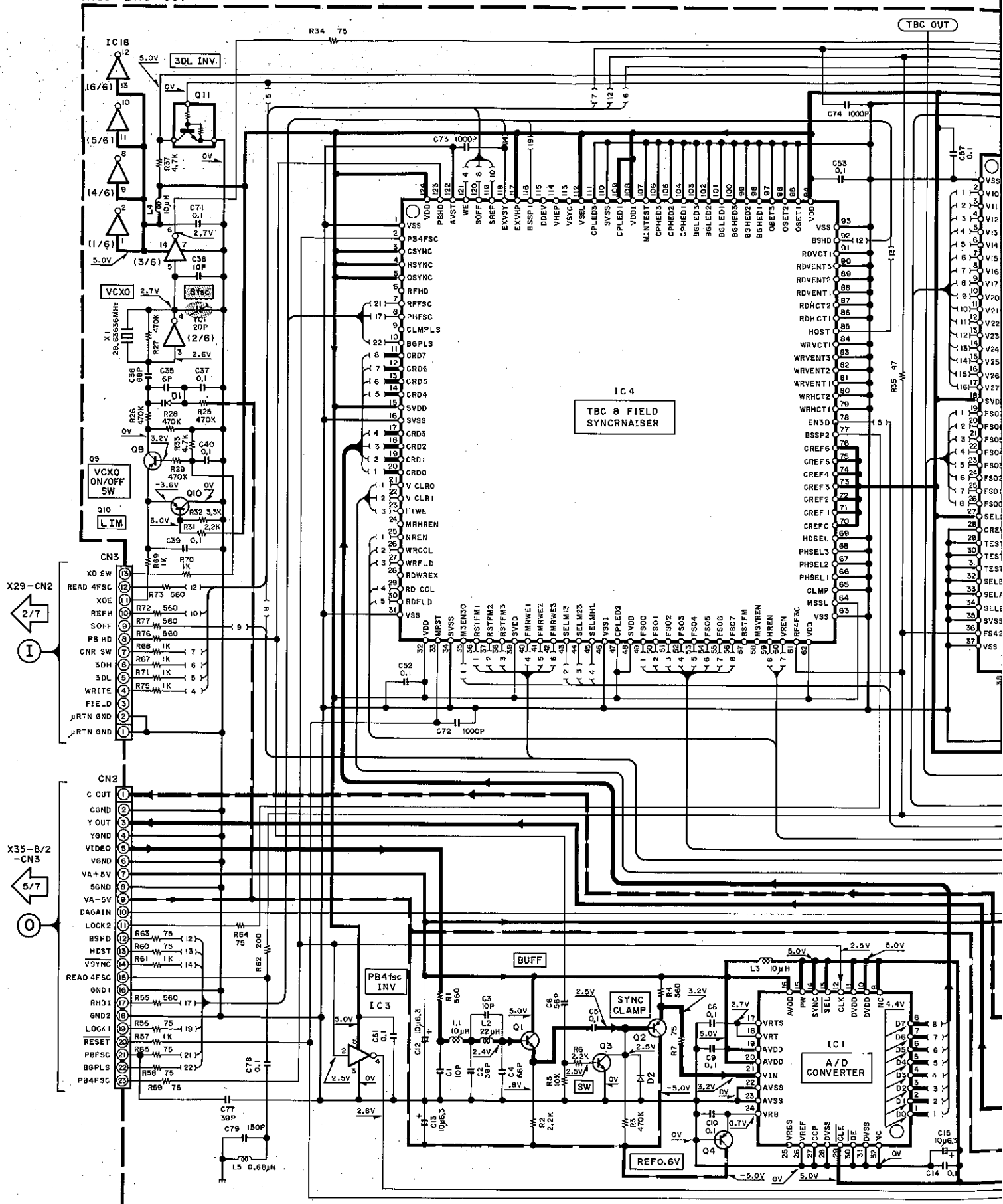
Place safety critical components in the correct positions. To reduce current or resistance measured parts are acceptably in the appliance is returned

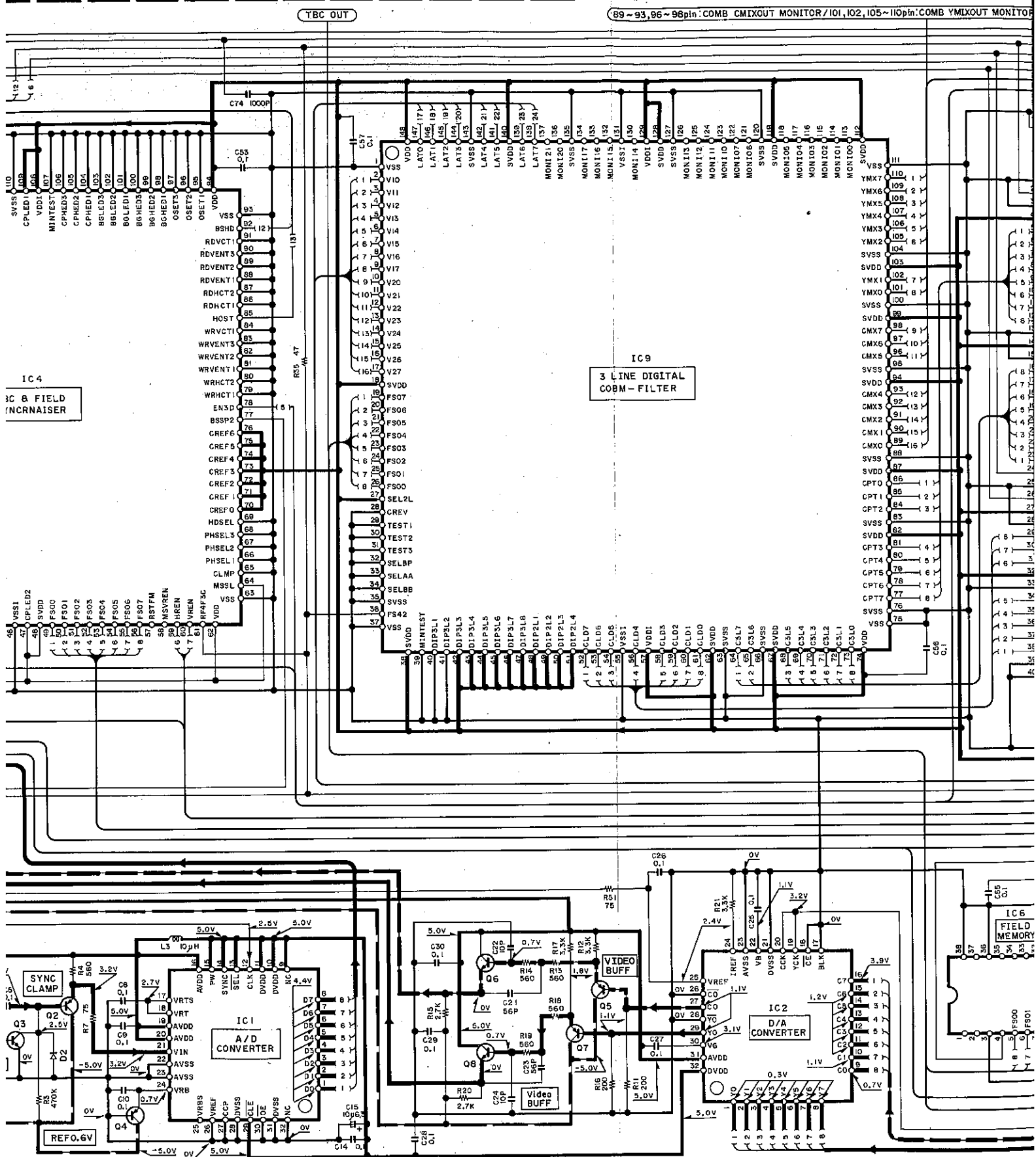
- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

Y22-3110-11

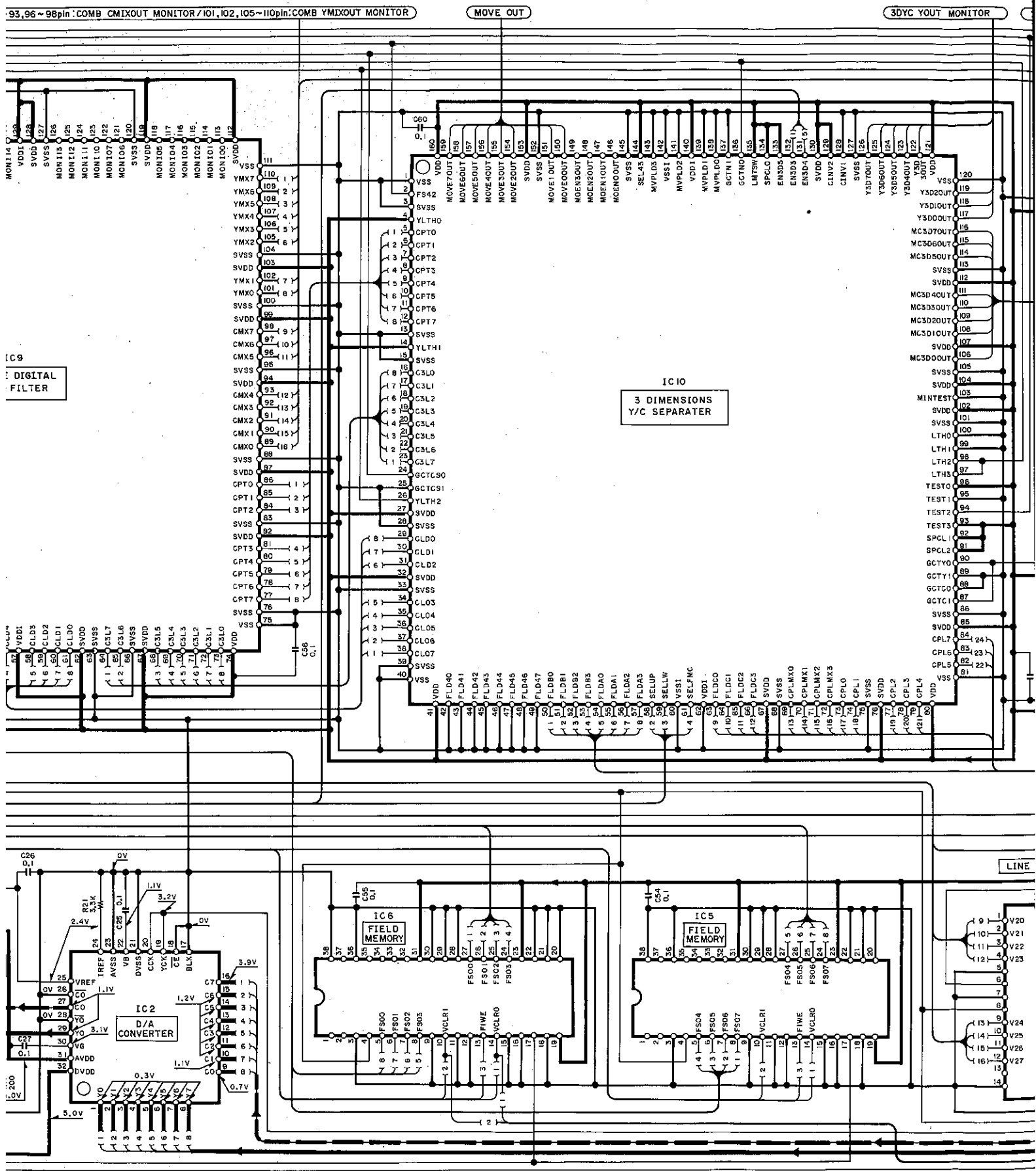
LVD-Z1

KENWOOD

VIDEO UNIT
(X35-2110-00)

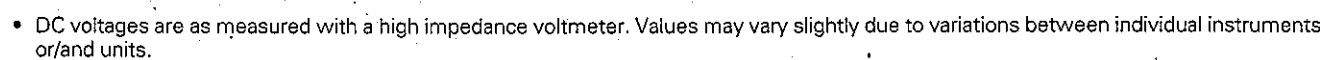


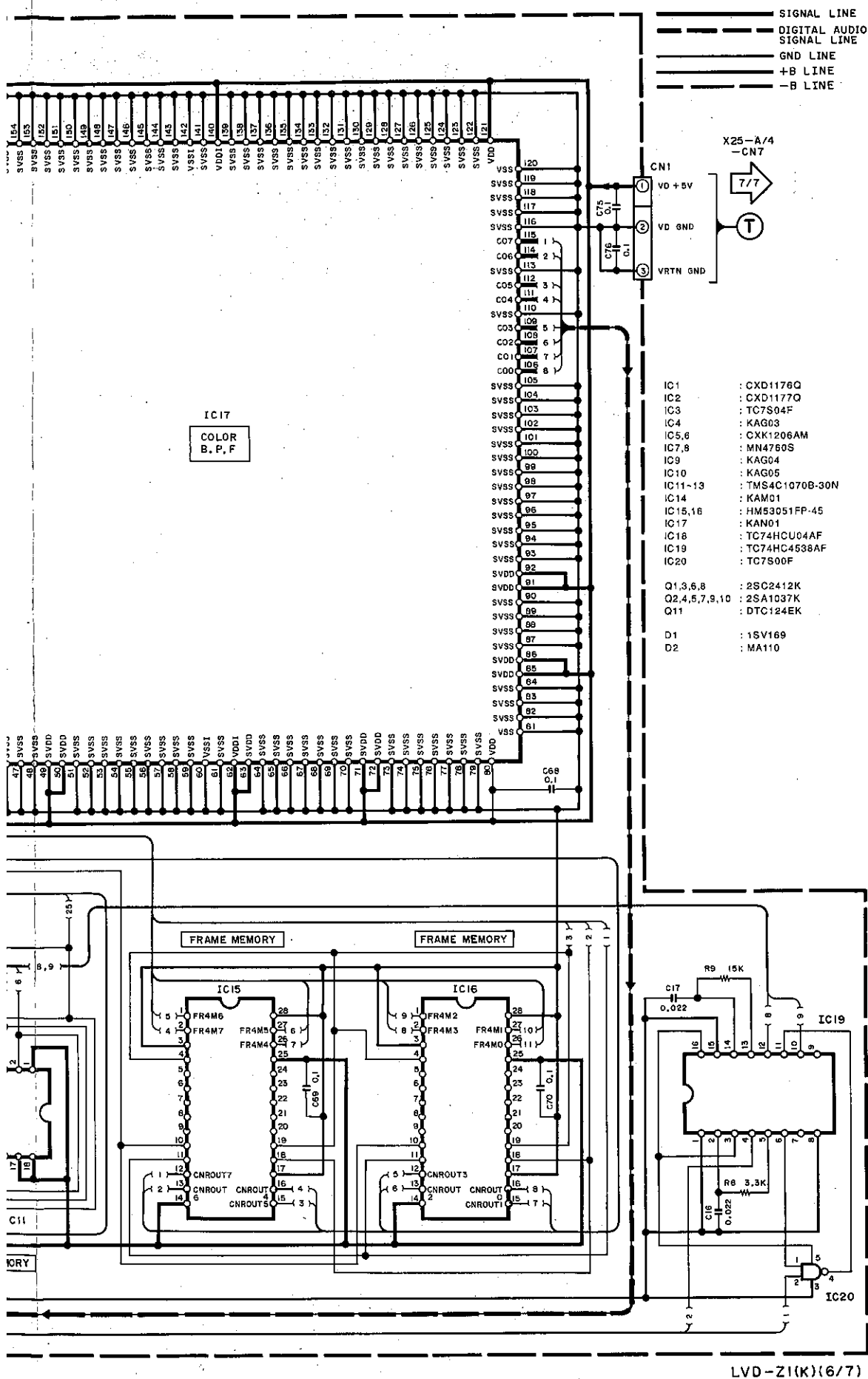
CAUTION : For continued safety, replace safety critical components. Δ Indicates safety critical components. To reduce the risk of fire, out (exposed parts are acceptably insulated from the supply circuit).



CAUTION : For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). Δ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

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Y22-3110-11

LVD-Z1

KENWOOD

X35-B/2
CN2

5/7

P

X35
CN1

6/7

T

X29
CN8

2/7

K

X35-B/2
CN8

5/7

Q

X32-A/2
CN2

3/7

N

X29
CN9

2/7

J

X35-B/2
CN6

5/7

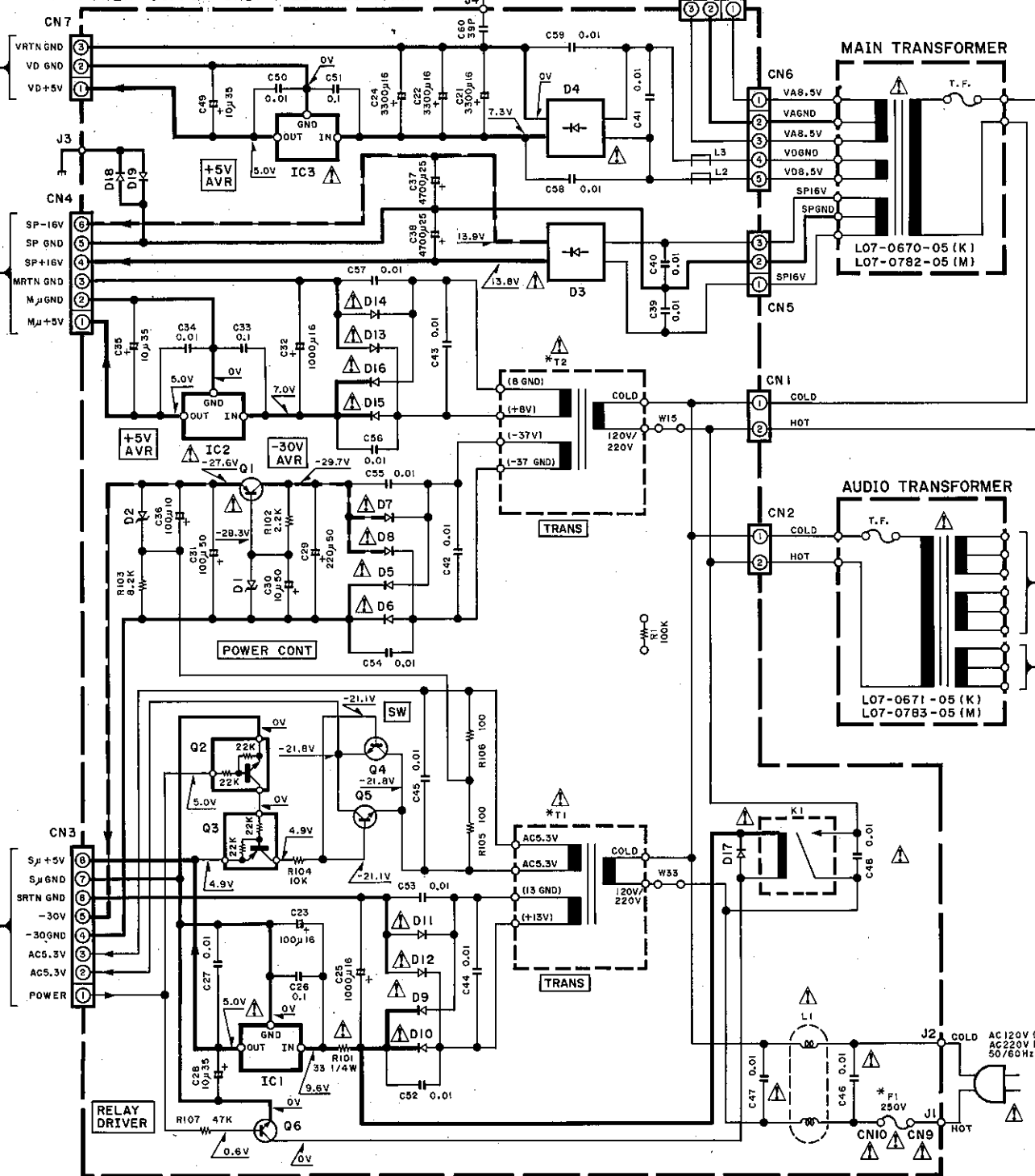
R

X35-B/2
CN7

5/7

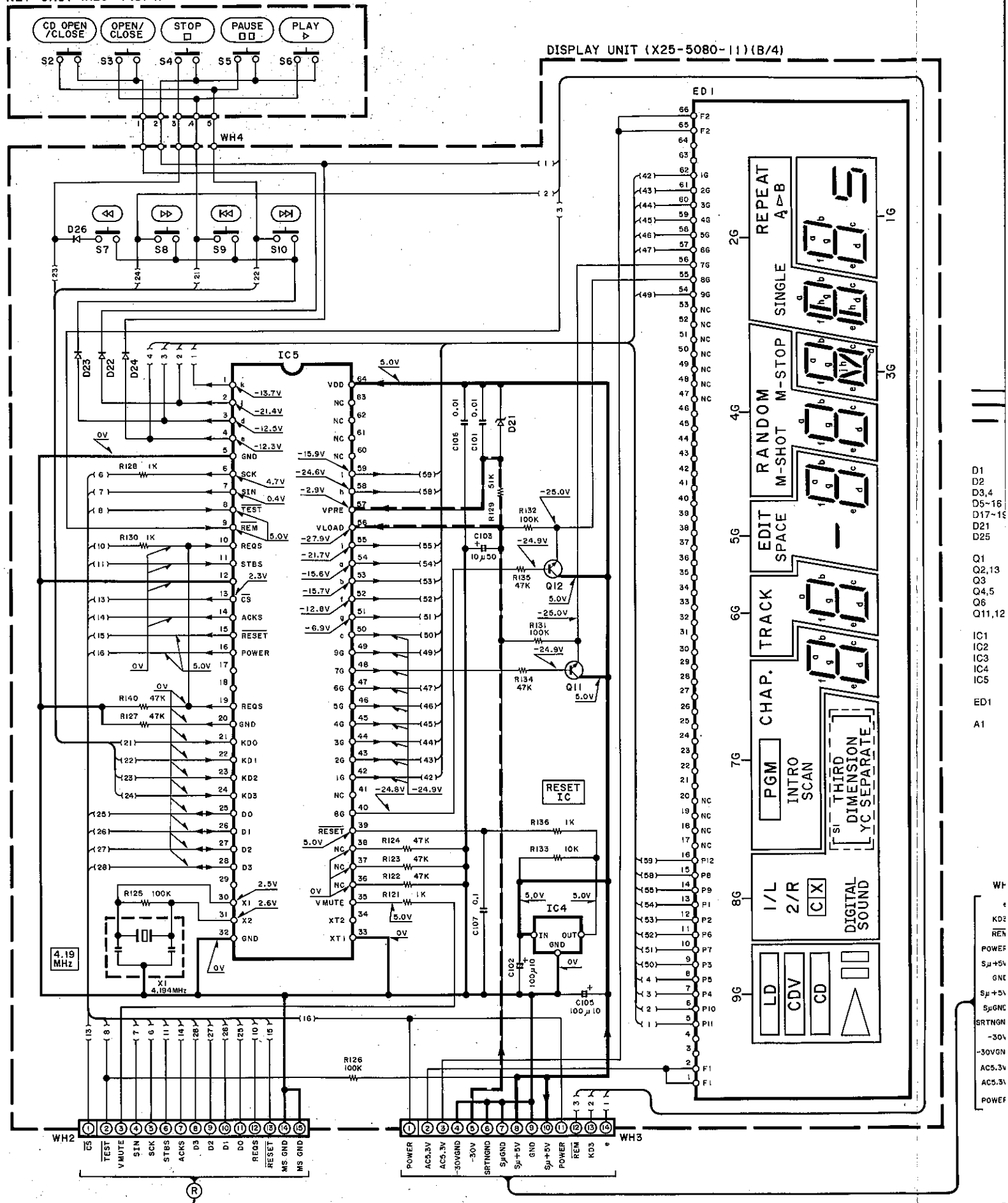
S

POWER SUPPLY UNIT (X25-5080-11)(A/4)



DESTINATION	COUNTRY	ABB.	UNIT NAME	F 1	T 1	T 2
U.S.A.	K	X25-5080-11	F04-1026-05 (250V 1A)	L07-0597-05	L07-0784-05	
GENERAL MARKET	M	X25-5080-21	F05-4016-05 (250V 1400mA)	L07-0598-05	L07-0785-05	

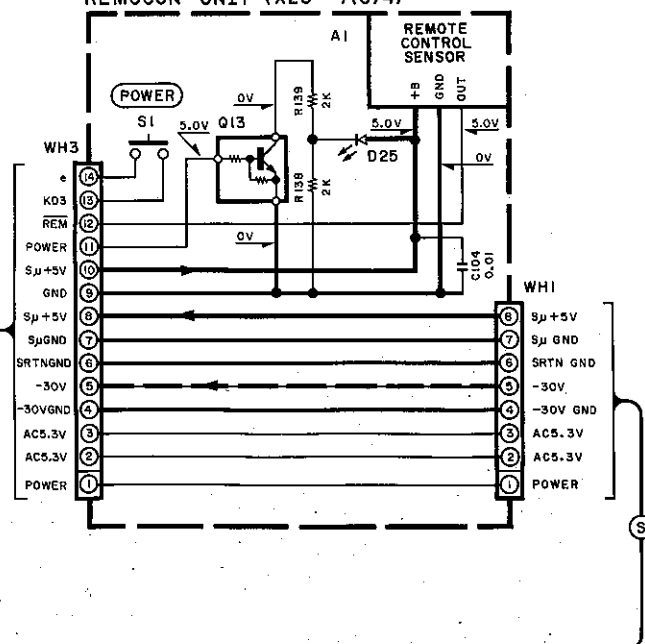
DISPLAY UNIT (X25-5080-11)(B/4)



_____ GND LINE
 _____ +B LINE
 - - - - - -B LINE

D1 : RD30ES(B2) or HZS30N(B2)
 D2 : RD5.1ES(B2) or HZS5.1N(B2)
 D3,4 : D3SBA20F03
 D5~16 : S5688B
 D17~19,22~24,26 : 1SS133 or HSS104
 D21 : RD8.2ES(B2) or HZS8.2N(B2)
 D25 : B30-1290-05
 Q1 : 2SA992(FE)
 Q2,13 : UN4212 or DTC124ES
 Q3 : UN4112 or DTA124ES
 Q4,5 : 2SD1302(S,T)
 Q6 : 2SC3246
 Q11,12 : 2SC3311A(Q,R) or 2SC2458(Y,GR)
 IC1 : μ PC78L05J
 IC2 : TA78DL05S
 IC3 : μ PC2405HF
 IC4 : PST529C
 IC5 : μ PD75216ACW-W44
 ED1 : 9-MT-125GK
 A1 : W02-1129-05

REMOCON UNIT (X25-)(C/4)



LVD-Z1 (K) (7/7)

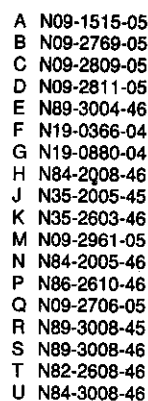
- DC voltages are as measured with a high impedance voltmeter. Values may vary slightly due to variations between individual instruments or/and units.

CAUTION : For continued safety, replace safety critical components only with manufacturer's recommended parts (refer to parts list). Δ Indicates safety critical components. To reduce the risk of electric shock, leakage-current or resistance measurements shall be carried out (exposed parts are acceptably insulated from the supply circuit) before the appliance is returned to the customer.

LVD-Z1
KENWOOD

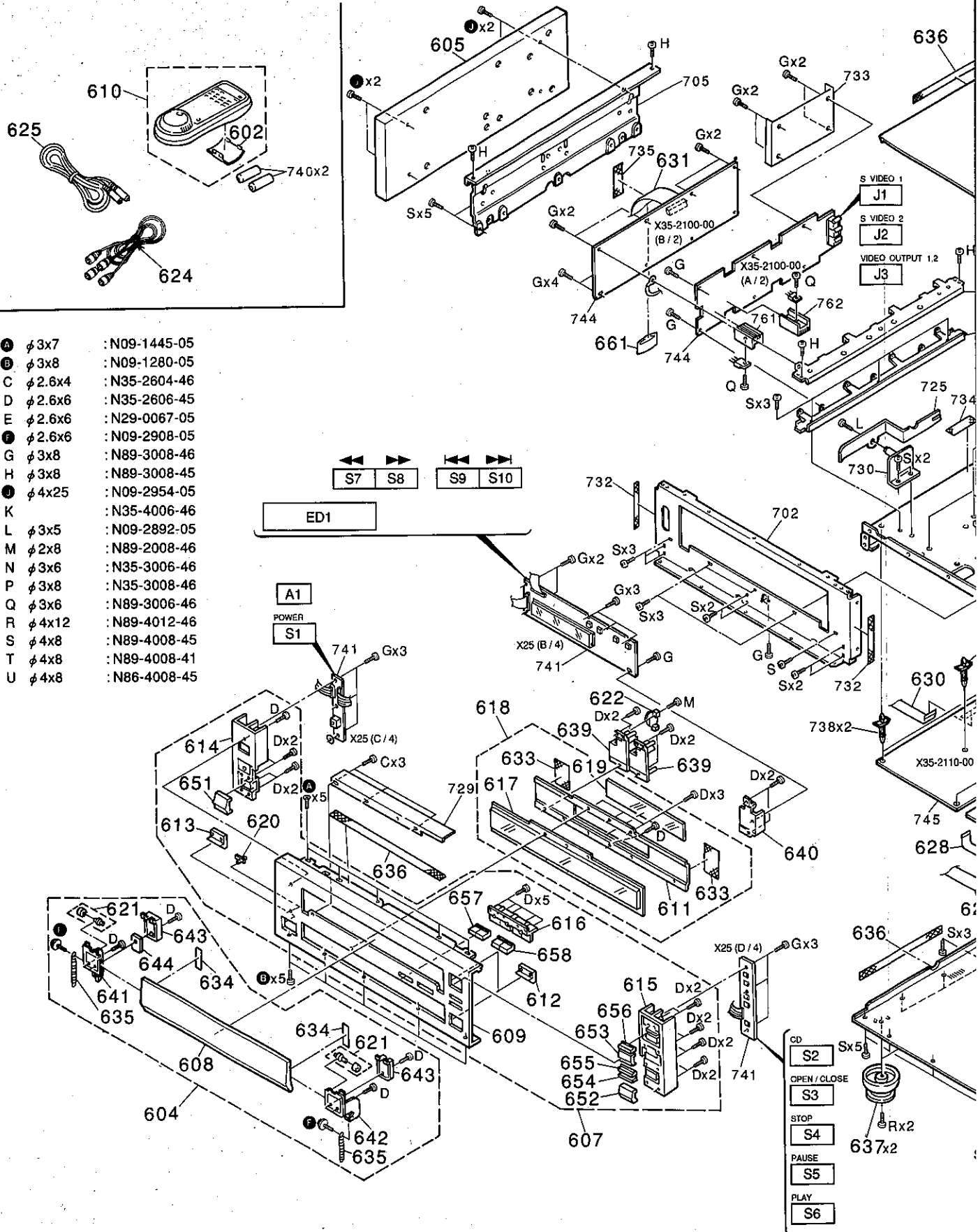
Y22-3110-11

8



LVD-Z1 LV

EXPLODED VIEW



VIEW : UNIT



Parts with the exploded numbers larger than 700 are not supplied.

PARTS LIST

* New Parts
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 Teile ohne Parts No. werden nicht geliefert.

2

Ref. No. 参照番号	Address 位置	Parts No. 部品番号	Description 部品名 / 規格	Desti- nation 仕向
643	3C	J19-3523-14	HOLDER(ROLLER)	
646	1E	J32-0336-04	HEXAGON BUSH(NECHA)	M
647	1F	J42-0194-05	POWER CORD BUSHING	K
647	1F	J42-0195-05	POWER CORD BUSHING	
-		J61-0307-05	WIRE BAND	
651	2C	K29-4484-04	KNOB(POWER)	
652	3D	K29-4485-04	KNOB(PLAY)	
653	3D	K29-4486-04	KNOB(OPEN/CLOSE)	
654	3D	K29-4487-04	KNOB(STOP)	
655	3D	K29-4488-04	KNOB(PAUSE)	
656	3D	K29-4489-04	KNOB(CD)	
657	3D	K29-4490-04	KNOB(SEARCH)	
658	3D	K29-4491-04	KNOB(SKIP)	
659	2E	L07-0670-05	POWER TRANSFORMER	K
659	2E	L07-0782-05	POWER TRANSFORMER	M
660	2E	L07-0671-05	POWER TRANSFORMER	M
660	2E	L07-0783-05	POWER TRANSFORMER	M
661	1D	L92-0036-05	FERRITE CORE	M
A		N09-1445-05	SET SCREW (M3X8)	
B		N09-1280-05	TAPITTE SCREW (3X8)	
C		N35-2604-46	BINDING HEAD MACHINE SCREW	
D		N35-2606-45	BINDING HEAD MACHINE SCREW	
E		N29-0067-05	PUSH RIVET (3.5X4.5)	
F		N09-2908-05	SET SCREW (2.6X6)	
G		N89-3008-46	BINDING HEAD TAPITTE SCREW	
H		N89-3008-45	BINDING HEAD TAPITTE SCREW	
J		N09-2954-05	DRESSED SCREW (4X25, +)	
K		N35-4006-46	BINDING HEAD MACHINE SCREW	
L		N09-2892-05	SENS (MACHINE SCREW)(M3X8)	
M		N89-2008-46	BINDING HEAD TAPITTE SCREW	
N		N35-3006-46	BINDING HEAD MACHINE SCREW	
P		N35-3008-46	BINDING HEAD MACHINE SCREW	
Q		N89-3006-46	BINDING HEAD TAPITTE SCREW	
R		N89-4012-46	BINDING HEAD TAPITTE SCREW	
S		N89-4008-45	BINDING HEAD TAPITTE SCREW	
T		N89-4008-41	BINDING HEAD TAPITTE SCREW	
U		N86-4008-45	BINDING HEAD TAPITTE SCREW	
ELECTRIC UNIT (X25-5080-11)				
D25		B30-1290-05	LED	
C21, 22		CE04KW1C332M	ELECTRO 3300UF 16VW	
C23		CE04KW1C101M	ELECTRO 1000UF 16VW	
C24		CE04KW1C332M	ELECTRO 3300UF 16VW	
C25		CE04KW1C102M	ELECTRO 1000UF 16VW	
C26		CF92FV1H104J	MF 0.10UF J	
C27		CF92FV1H103J	MF 0.010UF J	
C28		CE04KW1V100M	ELECTRO 10UF 35VW	
C29		CE04KW1H221M	ELECTRO 220UF 50VW	
C30		CE04KW1H100M	ELECTRO 10UF 50VW	
C31		CE04KW1H101M	ELECTRO 100UF 50VW	
C32		CE04KW1C102M	ELECTRO 1000UF 16VW	
C33		CF92FV1H104J	MF 0.10UF J	
C34		CF92FV1H103J	MF 0.010UF J	
C35		CE04KW1V100M	ELECTRO 10UF 35VW	
C36		CE04KW1A101M	ELECTRO 100UF 10VW	

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1

Ref. No. 参照番号	Address 位置	Parts No. 部品番号	Description 部品名 / 規格	Desti- nation 仕向
LVD-Z1				
601	1E	A01-2977-02	METALLIC CABINET	
602	1C	A09-0144-08	BATTERY COVER	
604	3C	A21-1821-13	DRESSING PANEL ASSY	
605	1D	A50-0345-03	SLIDE PLATE ASSY(LEFT)	
606	3F	A50-0346-03	SLIDE PLATE ASSY(RIGHT)	
607	3D	A60-0299-32	PANEL ASSY(FRONT)	
608	3C	A21-1820-03	DRESSING PANEL	
609	3D	A60-0300-11	PANEL(FRONT)	
610	1C	A70-0914-05	REMOTE CONTROLLER(RC-LVDZ1)	
611	3D	B03-2788-03	DRESSING PLATE	
612	3D	B03-2795-04	DRESSING PLATE	
613	2C	B03-2799-14	DRESSING PLATE	
614	2C	B07-2227-23	ESCUTCHEON(LEFT)	
615	3D	B07-2228-23	ESCUTCHEON(RIGHT)	
616	3D	B07-2229-04	ESCUTCHEON(CENTER)	
617	2D	B10-1937-03	FRONT GLASS	
618	2D	B10-1943-13	FRONT GLASS ASSY	
619	2D	B11-0255-04	COLOR FILTER	
620	2C	B12-0212-14	INDICATOR	
-		B46-0092-33	WARRANTY CARD	K
-		B46-0197-00	QUESTIONNAIRE CARD	K
-		B60-0962-00	INSTRUCTION MANUAL(ENGLISH)	
621	3C	D14-0327-05	ROLLER ASSY	
622	2D	D39-0309-05	DAMPER	
623	1F	E30-0974-05	AC POWER CORD	K
624	1C	E30-2580-05	AC POWER CORD	M
625	1C	E30-2600-05	CORD WITH PLUG(AUDIO)	
626	3E	E30-2725-05	CORD WITH PLUG(S-VIDEO)	
627	3E	E35-0019-05	FLAT CABLE(27P)	
628	3E	E35-0443-05	FLAT CABLE(19P)	
629	3E	E35-0445-05	FLAT CABLE(13P)	
630	2E	E35-0441-05	FLAT CABLE(23P)	
631	1D	E35-0593-05	FLAT CABLE(19P)	
644	3C	E29-0399-04	CONDUCTIVE RUBBER	
633	2D, 3D	G10-0177-04	NON-MOVEN FABRIC	
634	3C	G11-2157-04	CUSHION	
635	3C	G01-3487-04	EXTENSION SPRING	
636	1E	G10-0176-04	NON-MOVEN FABRIC	
-		H10-5372-01	POLYSTYRENE FOAMED FIXTURE(L)	
-		H10-5373-01	POLYSTYRENE FOAMED FIXTURE(R)	
-		H20-0580-04	PROTECTION COVER(SET)	
-		H25-0232-04	PROTECTION BAG (235X350X0.03)	
-		H25-0695-04	PROTECTION BAG	
-		H50-0451-04	ITEM CARTON CASE	
637	3D, 3E	J02-1080-04	FOOT	
639	3D	J19-3508-14	HOLDER(L)	
640	3D	J19-3507-04	HOLDER(R)	
641	3C	J19-3508-15	HOLDER(L)	
642	3C	J19-3509-13	HOLDER(R)	

L:Scandinavia K:USA P:Canada
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PARTS LIST

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4

Ref. No. 参照番号	Address 位置	New Parts 新部品	Parts No. 部品番号	Description 部品名 / 規格	Destination 仕向
Q3			UN4112	DIGITAL TRANSISTOR	
Q4			2SD1302(S,T)	TRANSISTOR	
Q6			2SC3246	TRANSISTOR	
Q11			2SC2458(Y,GR)	TRANSISTOR	
Q11			2SC3111A(G,R)	TRANSISTOR	
Q13			DT124ES	DIGITAL TRANSISTOR	
Q13			UN4212	DIGITAL TRANSISTOR	
A1	2C		W02-1129-05	ELECTRIC CIRCUIT MODULE	
ELECTRIC UNIT in MECHANISM ASS'Y (X25-5120-10)					
C1			CF92FV1H104J	MF 0.10UF J	
C2			CE04KW1H010M	ELECTRO 1.0UF 50WV	
C3			CE04KW1V100M	ELECTRO 10UF 35WV	
C4			CF92FV1H333J	MF 0.033UF J	
C6			CC45FSL1H330J	CERAMIC 33PF J	
C8			CK45PB1H102K	CERAMIC 1000PF K	
C9			CE04KW1A101M	ELECTRO 100UF 10WV	
C10			CE04KW1H010M	ELECTRO 1.0UF 50WV	
C12			CK45FF1H103Z	CERAMIC 0.010UF Z	
C14			CF92FV1H473J	MF 0.047UF J	
C15			CF92FV1H102J	MF 1000PF J	
C16			CE04KW1H010M	ELECTRO 1.0UF 50WV	
C18			CC45FSL1H220J	CERAMIC 22PF J	
L1			L40-1001-17	SMALL FIXED INDUCTOR(100H,K)	
R00			RN14BK2C1961F	RN 1.96K F 1/8W	
R05			RN14BK2C1961F	RN 1.96K F 1/8W	
VR1			R12-1619-05	TRIMMING POT 4.7K<TILT BALANCE>	
VR2			R12-1618-05	TRIMMING POT 3.3K<FE BALANCE>	
VR4			R12-3685-05	TRIMMING POT 10K<T.BALANCE>	
S1			S40-1139-05	PUSH SWITCH(SLT CD,L,D)	
S3			S64-0001-05	LEVER SWITCH(OPEN/CLOSE)	
PH1			T95-0048-05	OPTO ISOLATOR(EG SENSOR)	
PH2			T95-0108-05	OPTO ISOLATOR(TILT OUT SENSOR)	
IC1			BA10393	IC(DUAL COMPALATOR)	
IC2			NJM2058D	IC(OP AMP X4)	
IC4			UPC4574C	IC(OP AMP X4)	
IC5			XRU4053B	IC(ANALOG MULTIPLEXER)	
			NJM4565D	IC(OP AMP X2)	
Q1			2SA110(R,S)	TRANSISTOR	
Q2			2SC2458(Y,GR)	TRANSISTOR	
Q2			2SC3111A(G,R)	TRANSISTOR	
CONTROL CIRCUIT UNIT (X29-2380-00)					
C1			CE04KW1E101M	ELECTRO 100UF 25WV	
C4			CF92FV1H332J	MF 3300PF J	
C5			CK45FF1H103Z	CERAMIC 0.010UF Z	
C6			CE04KW1H010M	NP-ELEC 1.0UF 50WV	
C7			CF92FV1H332J	MF 3300PF J	
C8			CE04KW1V101M	ELECTRO 100UF 35WV	
C10			CE04KW1V100M	ELECTRO 10UF 35WV	
C11			CE04KW0331M	ELECTRO 330UF 6.3WV	
C12			CK45FF1H103Z	CERAMIC 0.010UF Z	
C13			CK45FF1H473Z	CERAMIC 0.047UF Z	

L:Scandinavia K:USA P:Canada
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Y:AFES(Europe) X:Australia M:Other Areas

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3

Ref. No. 参照番号	Address 位置	New Parts 新部品	Parts No. 部品番号	Description 部品名 / 規格	Destination 仕向
C37		*	C30-3449-05	ELECTRO 4700UF 25WV	
C39			CK45FF1H103Z	CERAMIC 0.010UF Z	
C46			C91-0971-05	FILM 250WV	
C49			CE04KW1V100M	ELECTRO 10UF 35WV	
C50			CF92FV1H103J	MF 0.010UF J	
C51			CF92FV1H104J	MF 0.10UF J	
C52			CK45FF1H103Z	CERAMIC 0.010UF Z	
C60			CC45FSL1H330J	33PF J	
C101			C91-0769-05	CERAMIC 0.01UF K	
C102			CE04KW1A101M	ELECTRO 100UF 10WV	
C103			CE04KW1H100M	ELECTRO 10UF 50WV	
C104			CK45FF1H103Z	CERAMIC 0.010UF Z	
C105			CE04KW1A101M	ELECTRO 100UF 10WV	
C106			CK45FF1H103Z	CERAMIC 0.010UF Z	
C107			CF92FV1H104J	MF 0.10UF J	
F1			F04-1026-05	FUSE (UL) (250V 1A)	K
F1			F05-4016-05	FUSE (SEMKO) (250V T400mA)	M
CN9			J13-0075-05	FUSE CLIP	
L1			L79-0733-05	LINE FILTER	
L2			L92-0018-05	FERRITE CORE	
T1		*	L07-0597-05	POWER TRANSFORMER	K
T1		*	L07-0784-05	POWER TRANSFORMER	M
T2		*	L07-0598-05	POWER TRANSFORMER	K
T2		*	L07-0785-05	POWER TRANSFORMER	M
X1			L78-0267-05	RESONATOR (4.194MHz)	
R101			R014682B330J	FL-PROOF RD 33 J 1/4W	
K1			SS1-1052-05	MAGNETIC RELAY	
S1			S40-1064-05	TACT SWITCH(POWER, OPEN/CLOSE)	
D1			HZS30N(B2)	ZENER DIODE	
D1			R030ES(B2)	ZENER DIODE	
D2			HZS5-1N(B2)	ZENER DIODE	
D2			R05-1ES(B2)	ZENER DIODE	
D3			D35BA20F03	DIODE	
D5			SS688B	DIODE	
D17			HSS104	DIODE	
D17			1S5133	DIODE	
D21			HZS8-2N(B2)	ZENER DIODE	
D21			R08-2ES(B2)	ZENER DIODE	
D22			HSS104	DIODE	
D22			1S5133	DIODE	
D26			HSS104	DIODE	
D26			1S5133	DIODE	
ED1			9-WT-125GK	INDICATOR TUBE	
IC1		*	UPC78L05J	IC(VOLTAJE REGULATOR/ +5V)	
IC2		*	TA789L05S	IC(VOLTAJE REGULATOR/ +5V)	
IC3			UPC2405HF	IC(VOLTAJE REGULATOR/ +5V)	
IC4			PST529C	IC(SYSTEM RESET)	
IC5		*	UPD75216ACN-W44	IC(MICROPROCESSOR)	
Q1			2SA992(R,E)	TRANSISTOR	
Q2			DT124ES	DIGITAL TRANSISTOR	
Q2			UN4212	DIGITAL TRANSISTOR	
Q3			DTA124ES	DIGITAL TRANSISTOR	

L:Scandinavia K:USA P:Canada
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Y:AFES(Europe) X:Australia M:Other Areas

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PARTS LIST

* New Parts

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Teile ohne Parts No. werden nicht geliefert.

5

Ref. No. 参照番号	Address 位置	Parts No. 部品番号	Description 部品名 / 規格	Desti- nation 仕向
C19		C045FSL1H221J	CERAMIC	
C20		CX45FF1H103Z	220PF J	
C21		C004KW1H010M	0.010UF Z	
C22		C004KW1H010M	0.47UF 50WV	
C23		C004KW1H010M	220UF 16WV	
		C004KW1H010M	0.10UF J	
C24		CX45FF1H103Z	0.010UF Z	
C26		C004KW1H010M	1000PF J	
C27		C004KW1H010M	2.2UF 50WV	
C28	29	CX45FB1H101J	1000PF K	
C30		C004KW1H010M	100PF J	
C31		CX45FB1H101J	1000PF K	
C32		C004KW1H010M	1.0UF 50WV	
C33		C004KW1H010M	2700PF J	
C34		CX45FF1H103Z	0.010UF Z	
C35		C004KW1H010M	10UF 35WV	
C36		C004KW1H010M	0.010UF J	
C37		C004KW1H010M	120PF J	
C38		C004KW1H010M	1.0UF 50WV	
C39	40	C004KW1H010M	10UF 35WV	
C41		C004KW1H010M	4.7UF 35WV	
C42		C004KW1H010M	100UF 10WV	
C43		C004KW1H010M	3500PF J	
C44		C004KW1H010M	4.7UF 35WV	
C45		C004KW1H010M	2700PF J	
C46	49	C004KW1H010M	100UF 25WV	
C50		C004KW1H010M	10PF D	
C51		C004KW1H010M	47PF J	
C52		C004KW1H010M	0.010UF Z	
C53		C004KW1H010M	1000PF K	
C54		C004KW1H010M	0.010UF Z	
C55		C004KW1H010M	47UF 25WV	
C57		C004KW1H010M	1000PF K	
C60	61	C004KW1H010M	0.10UF J	
C62	65	C004KW1H010M	10UF 35WV	
C66	69	C004KW1H010M	100UF 25WV	
C70		C004KW1H010M	4.7UF 35WV	
C71		C004KW1H010M	0.010UF Z	
C72		C004KW1H010M	4.7UF 35WV	
C73	74	C004KW1H010M	10UF 35WV	
C75		C004KW1H010M	0.010UF Z	
C76		C004KW1H010M	2200UF 10WV	
C77		C004KW1H010M	4700UF 10WV	
C78		C004KW1H010M	2200UF 10WV	
C80	81	C004KW1H010M	100PF J	
C82		C004KW1H010M	120PF J	
C83	87	C004KW1H010M	0.10UF J	
C88		C004KW1H010M	2.2UF 50WV	
C90		C004KW1H010M	0.10UF J	
C91		C004KW1H010M	1500PF J	
C92		C004KW1H010M	3900PF J	
C93		C004KW1H010M	4700PF J	
C95		C004KW1H010M	0.22UF J	
C96		C004KW1H010M	10UF 25WV	
C97		C004KW1H010M	0.15UF J	
C98		C004KW1H010M	560PF K	

LScandinavia

KUSA

PCanada

T:England

E:Europe

M:Other Areas

Y:AFES(Europe)

X:Australia

Y:PX(Far East, Hawaii)

LScandinavia

KUSA

PCanada

T:England

E:Europe

M:Other Areas

Y:AFES(Europe)

X:Australia

Y:PX(Far East, Hawaii)

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6

Ref. No. 参照番号	Address 位置	Parts No. 部品番号	Description 部品名 / 規格	Desti- nation 仕向
C99		C004KW1H010M	MF	
C100		C004KW1H010M	4700PF J	
C101		C004KW1H010M	0.015UF J	
C102		C004KW1H010M	1.0UF 50WV	
C103		C004KW1H010M	100UF 25WV	
		C004KW1H010M	0.10UF J	
C104		C004KW1H010M	1.0UF 50WV	
C105		C004KW1H010M	100UF 35WV	
C106		C004KW1H010M	1.0UF 50WV	
C107		C004KW1H010M	0.10UF J	
C108		C004KW1H010M	0.047UF J	
C109		C004KW1H010M	10UF 35WV	
C110		C004KW1H010M	0.010UF J	
C111		C004KW1H010M	220PF J	
C112		C004KW1H010M	10UF 25WV	
C113		C004KW1H010M	47UF 10WV	
C114		C004KW1H010M	10UF 35WV	
C115		C004KW1H010M	1000PF J	
C116		C004KW1H010M	1.0UF 50WV	
C117		C004KW1H010M	1.0UF 50WV	
C118-120		C004KW1H010M	100PF J	
C121		C004KW1H010M	ELECTR0	
C122		C004KW1H010M	CERAMIC	
C123		C004KW1H010M	0.047UF J	
C124		C004KW1H010M	100PF J	
C125		C004KW1H010M	0.022UF J	
C126		C004KW1H010M	6800PF J	
L1		L33-0363-05	CHOKE COIL	
L2		L40-2211-17	SMALL FIXED INDUCTOR(220UH, K)	
L3	4	L40-1031-46	SMALL FIXED INDUCTOR(10mH, K)	
L5		L92-0021-05	FERRITE CORE	
X1		L78-0280-05	REGULATOR (10.000MHz)	
R1		RS14KB3AR47J	FL-PROOF RS 0.47 J 1W	
R30		RS14KB30271J	FL-PROOF RS 270 J 2W	
R39		RS14KB3A151J	FL-PROOF RS 150 J 1W	
R100		RD14CB2E561J	FL-PROOF RD 560 J 1/4W	
D1	-4	RK36	DIODE	
D5		HSS104	DIODE	
D5		HSS133	DIODE	
D6		HSS.6N(B2)	ZENER DIODE	
D6		HSS.6ES(B2)	ZENER DIODE	
D7	-16	HSS104	DIODE	
D7	-16	HSS133	DIODE	
D17		HSS.1N(B2)	ZENER DIODE	
D17		HSS.1ES(B2)	ZENER DIODE	
D18	19	HSS15N(B2)	ZENER DIODE	
D18	19	RD15ES(B2)	ZENER DIODE	
D20		HSS.1N(B2)	ZENER DIODE	
D20		HSS.1ES(B2)	ZENER DIODE	
D21	22	HSS.6N(B2)	ZENER DIODE	
D21	22	HSS.6ES(B2)	ZENER DIODE	
D23	-26	S5688B	DIODE	
D23	-26	LSR139-100	DIODE	
D31	-33	HSS104	DIODE	
D31	-33	LSR133	DIODE	

PARTS LIST

* New Parts

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Ref. No. 参照番号	Address 位置	New Parts 新部品	Parts No. 部品番号	Description 部品名 / 規格	Desti- nation 仕向備考
Q43			UN4112	DIGITAL TRANSISTOR	
Q44			2SK163(L, M)	FET	
Q45			DTC124ES	DIGITAL TRANSISTOR	
Q46			UN4212	DIGITAL TRANSISTOR	
Q47			DTA124ES	DIGITAL TRANSISTOR	
Q48			UN4112	DIGITAL TRANSISTOR	
Q49			2SK163(L, M)	FET	
Q49			DTA124ES	DIGITAL TRANSISTOR	
Q49			UN4112	DIGITAL TRANSISTOR	
Q50			2SK163(L, M)	FET	
Q51, 52			2SC3940A(R, S)	TRANSISTOR	
Q53			DTA124ES	DIGITAL TRANSISTOR	
Q54			UN4112	DIGITAL TRANSISTOR	
Q54			DTC124ES	DIGITAL TRANSISTOR	
Q54			UN4212	DIGITAL TRANSISTOR	
Q59			DTA124ES	DIGITAL TRANSISTOR	
Q59			UN4112	DIGITAL TRANSISTOR	
Q60			2SK163(L, M)	FET	
Q61, 62			DTC124ES	DIGITAL TRANSISTOR	
Q61, 62			UN4212	DIGITAL TRANSISTOR	
Q64			2SK163(L, M)	FET	
PROCESSOR UNIT (X32-2350-00)					
C3	-6		CC45FFH103Z	CERAMIC	0.010UF Z
C9	-15		CE04KW1C102M	ELECTRO	1000UF 16WV
C16			CE04KW1H010M	ELECTRO	1.0UF 50WV
C17			CC45FSL1H220J	CERAMIC	22PF J
C18			CC45FSL1H820J	CERAMIC	82PF J
C19			CC45FSL1H220J	CERAMIC	22PF J
C20			CE04KW1H3R3M	ELECTRO	3.3UF 50WV
C21			CF92FV1H223J	MF	0.022UF J
C22			CF92FV1H334J	MF	0.33UF J
C24			CC45FSL1H270J	CERAMIC	27PF J
C26			CC45FSL1H680J	CERAMIC	68PF J
C27			CC45FSL1H221J	CERAMIC	220PF J
C28			CC45FSL1H151J	CERAMIC	150PF J
C29			CE04KW1V220M	ELECTRO	22UF 35WV
C30			CC45FSL1H680J	CERAMIC	68PF J
C31			CF92FV1H182J	MF	1800PF J
C32			CE04KW1E470M	ELECTRO	47UF 25WV
C33			CF92FV1H103J	MF	0.010UF J
C34			CF92FV1H153J	MF	0.015UF J
C35			CF92FV1H104J	MF	0.10UF J
C36			CC45FSL1H121J	CERAMIC	120PF J
C37			CF92FV1H561J	MF	560PF J
C38			CE04KW1H010M	ELECTRO	1.0UF 50WV
C39			CF92FV1H392J	MF	3900PF J
C40			CF92FV1H103J	MF	0.010UF J
C41			CE04KW1A101M	ELECTRO	100UF 10WV
C42			CF92FV1H103J	MF	0.010UF J
C43			CE04KW1A101M	ELECTRO	100UF 10WV
C44, 45			CF92FV1H223J	MF	0.022UF J
C46 - 49			CF92FV1H472J	MF	4700PF J
C50, 51			CE04HW1E4R7M	NP-BLBC	4.7UF 25WV
C52, 53			CF92FV1H393J	MF	0.039UF J

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D35 -39			HSS104	DIODE	
D35 -39			1SS133	DIODE	
IC1			STA303A	IC(TRANSISTOR ARRAY)	
IC2			STA302A	IC(TRANSISTOR ARRAY)	
IC3			NJM45600-N	IC(OP AMP X2)	
IC4			TA8413P	IC(MOTOR CONTROL)	
IC5			TC4053BP	IC(3-INPUT 2CH MPX/DE-MPX)	
IC5			XRU4053B	IC(ANALOG MULTIPLEXER)	
IC6			NJM4565D	IC(OP AMP X2)	
IC7			TC5081AP	IC(PHASE COMPARTOR)	
IC8			HD49403NT	IC(SPINDLE SERV0 CONTROLLER)	
IC9			NJM4565D	IC(OP AMP X2)	
IC10			PD0011A	IC(DECODER)	
IC11			M37451M8-134SP	IC(MICROPROCESSOR)	
IC12			BA17805T	IC(VOLTAGE REGULATOR / +5V)	
IC12			TA7805S	IC(VOLTAGE REGULATOR / +5V)	
IC13			NJM4565D	IC(OP AMP X2)	
IC14			TA8410AK	IC(POWER OP. AMP)	
IC15			TA7272P	IC(OP AMP X2)	
IC16-19			NJM4565D	IC(OP AMP X2)	
IC20			HA11529	IC(CD/LD SERV0 IC)	
Q1			2SC2458(Y, GR)	TRANSISTOR	
Q1			2SC3311A(Q, R)	TRANSISTOR	
Q2 -5			2SA1048(Y, GR)	TRANSISTOR	
Q2 -5			2SA1309A(Q, R)	TRANSISTOR	
Q6			2SC4064	TRANSISTOR	
Q7			2SC2458(Y, GR)	TRANSISTOR	
Q7			2SC3311A(Q, R)	TRANSISTOR	
Q8			2SA1048(Y, GR)	TRANSISTOR	
Q8			2SA1309A(Q, R)	TRANSISTOR	
Q9			DTC124ES	DIGITAL TRANSISTOR	
Q9			UN4212	DIGITAL TRANSISTOR	
Q10, 11			2SC2458(Y, GR)	TRANSISTOR	
Q10, 11			2SC3311A(Q, R)	TRANSISTOR	
Q12, 13			DTC124ES	DIGITAL TRANSISTOR	
Q12, 13			UN4212	DIGITAL TRANSISTOR	
Q14			2SA1048(Y, GR)	TRANSISTOR	
Q14			2SA1309A(Q, R)	TRANSISTOR	
Q15			2SC2458(Y, GR)	TRANSISTOR	
Q15			2SC3311A(Q, R)	TRANSISTOR	
Q20, 21			DTC124ES	DIGITAL TRANSISTOR	
Q20, 21			UN4212	DIGITAL TRANSISTOR	
Q22, 23			DTA124ES	DIGITAL TRANSISTOR	
Q22, 23			UN4112	DIGITAL TRANSISTOR	
Q24			2SK163(L, M)	FET	
Q25			DTA124ES	DIGITAL TRANSISTOR	
Q25			UN4112	DIGITAL TRANSISTOR	
Q30			2SD882	TRANSISTOR	
Q31, 32			2SD772	TRANSISTOR	
Q33			2SD882	TRANSISTOR	
Q40			DTA124ES	DIGITAL TRANSISTOR	
Q40			UN4112	DIGITAL TRANSISTOR	
Q41, 42			DTC124ES	DIGITAL TRANSISTOR	
Q41, 42			UN4212	DIGITAL TRANSISTOR	
Q43			DTA124ES	DIGITAL TRANSISTOR	

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Ref. No. 参照番号	Address 位置	Parts No. 部品番号	Description 部品名 / 規格	Desti- nation 仕
C54		CF92FV1H103J	0.010UF J	
C55		CE04KW1A101M	100UF 10WV	
C56		CF92FV1H103J	0.010UF J	
C57		CF92FV1H104J	0.010UF J	
C58		CE04KW1E100N	100UF 25WV	
C59, 60		CE04KW1A221M	220UF 10WV	
C61		CE04KW1HR47M	0.47UF 50WV	
C62, 63		CE04KW1E100N	100UF 25WV	
C64, 65		CF92FV1H473J	0.047UF J	
C66		CF92FV1H682J	6800PF J	
C67		CF92FV1H392J	3900PF J	
C68		CF92FV1H103J	0.010UF J	
C69 -72		CE04KW1E4R7M	4.7UF 25WV	
C73		CF92FV1H103J	0.010UF J	
C74		CF92FV1H152J	1500PF J	
C75 -77		CF92FV1H473J	0.047UF J	
C78		CF92FV1H103J	0.010UF J	
C79		CE04KW1H010M	1.0UF 50WV	
C80		CF92FV1H105J	1.0UF J	
C81		CF92FV1H103J	0.010UF J	
C82		CF92FV1H332J	3300PF J	
C83		CE04KW1A330M	330UF 10WV	
C84		CF92FV1H103J	0.010UF J	
C85		CE04KW1V4R7M	4.7UF 35WV	
C86		CF92FV1H682J	6800PF J	
C87		CF92FV1H103J	0.010UF J	
C88		CE04KW1V220M	22UF 35WV	
C89		CE04KW1V4R7M	4.7UF 35WV	
C90		CE04KW1V100M	100UF 35WV	
C91		CE04KW1V4R7M	4.7UF 35WV	
C92		CE04KW1V100M	100UF 35WV	
C93		CE04KW1V220M	22UF 35WV	
C94		CE04KW1V4R7M	4.7UF 35WV	
C95		CE04KW1V100M	100UF 35WV	
C96		CE04KW1V220M	22UF 35WV	
C97		CE04KW1V100M	100UF 35WV	
C98		CE04KW1E4R7M	4.7UF 25WV	
C99		CE04KW1V100M	100UF 35WV	
C100		CE04KW1V220M	22UF 35WV	
C101		CE04KW1V100M	100UF 35WV	
C102, 103		CE04KW1V100M	100UF 35WV	
C104		CE04KW1V220M	22UF 35WV	
C105		CE04KW1V4R7M	4.7UF 35WV	
C106, 107		CE04KW1V100M	100UF 35WV	
C108		CE04KW1E4R7M	4.7UF 25WV	
C109		CE04KW1V100M	100UF 35WV	
C110		CE04KW1V220M	22UF 35WV	
C111		CE04KW1V100M	100UF 35WV	
C112		CF92FV1H122J	1200PF J	
C113		CE04FSL1H180J	18PF J	
C114		CE04FSL1H180J	18PF J	
C115		CE04FSL1H120J	12PF J	
C116		CE04FSL1H180J	18PF J	
C117		CE04FCH1H221J	220PF J	
C118		CE04FCH1H151J	150PF J	
C119		CE04FCH1H330J	33PF J	
C120		CE04FCH1H151J	150PF J	
C121		CK45FF1H103Z	0.010UF Z	
C122		CE04KW1A101M	100UF 10WV	
C123		CE04KW1H010M	1.0UF 50WV	
C124, 125		CK45FF1H103Z	0.010UF Z	
C126, 127		CF92FV1H274J	0.27UF J	
C128		CF92FV1H104J	0.10UF J	
C129		CF92FV1H103J	0.010UF J	
C130		CK45FF1H472Z	4700PF Z	
C131-134		CF92FV1H104J	0.10UF J	
C135, 136		CE04KW1E470M	47UF 25WV	

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Ref. No. 参照番号	Address 位置	Parts No. 部品番号	Description 部品名 / 規格	Desti- nation 仕
C137, 138		CF92FV1H104J	0.10UF J	
C139, 140		CF92FV1H821J	820PF J	
C141-144		CF92FV1H221K	220PF K	
C145, 146		CE04KW1V100M	100UF 35WV	
C147, 148		CF92FV1H101K	100PF K	
C149, 150		CF92FV1H331K	330PF K	
C151-154		CE04KW1H010M	1.0UF 50WV	
C155, 156		CF92FV1H122J	1200PF J	
C157, 158		CE04KW1E100M	100UF 25WV	
C159-162		CF92FV1H182J	1800PF J	
C163, 164		CF92FV1H303J	0.030UF J	
C165		CC45FSL1H330J	33PF J	
C166		CF92FV1H104J	0.10UF J	
C167		CC45FSL1H470J	47PF J	
C169		CC45FSL1H470J	47PF J	
C170		CE04KW1V4R7M	4.7UF 35WV	
C171-174		CE04KW1V100M	100UF 35WV	
TC1		C05-0223-05	TRIM CAP 30PF MASTER CLK FQ	
J1	2F	E63-0082-05	PHONE JACK(AUDIO OUTPUT)	
L1		L39-1314-05	MATCHING COIL	
L2		L40-6801-17	SMALL FIXED INDUCTOR(68UH, K)	
L3		L40-1511-17	SMALL FIXED INDUCTOR(150UH, K)	
L4		L40-1811-17	SMALL FIXED INDUCTOR(180UH, K)	
L5		L40-1511-17	SMALL FIXED INDUCTOR(150UH, K)	
L6		L40-1511-17	SMALL FIXED INDUCTOR(150UH, K)	
L7		L79-0797-05	LC FILTER	
L8		L40-6891-17	SMALL FIXED INDUCTOR(6.8UH, K)	
L9 -14		L92-0018-05	FERRITE CORE	
X1		L77-1129-05	CRYSTAL RESONATOR(16.9525MHZ)	
X2		L77-2117-05	CRYSTAL RESONATOR(16.954400H)	
R101		RN148K2C1000F	RN 100.0 F 1/6W	
R109		RN148K2C1000F	RN 100.0 F 1/6W	
R117		RN148K2C1000F	RN 100.0 F 1/6W	
VR1, 2		R12-1084-05	TRIMMING POT 1K TRACKING, FOCUS	
X1 -3		S51-2089-05	MAGNETIC RELAY	
Δ D1 -8		ERA081-004	DIODE	
D10 -12		HZSS.1S(B2)	ZENER DIODE	
D10 -12		RD5.1JS(B2)	ZENER DIODE	
D13 -15		HZSS.2S(B2)	ZENER DIODE	
D13 -15		RD8.2JS(B2)	ZENER DIODE	
D16 -18		HZSS.1S(B2)	ZENER DIODE	
D16 -18		RD5.1JS(B2)	ZENER DIODE	
D22 -24		HSS104	DIODE	
D22 -24		1SS133	DIODE	
D27		1SV147	VARIABLE CAPACITANCE DIODE	
D28 -34		HSS104	DIODE	
D28 -34		1SS133	DIODE	
IC1		TC74HC00AP	IC(QUAD 2-INPUT NAND GATE)	
IC2		NJM4565D	IC(OP AMP X2)	
IC3		CA0002AM	IC(LD AUDIO SYSTEM)	
IC4		CXD2500BQ	IC(DIGITAL SIGNAL PROCESSOR)	
IC5, 6		NJM4565D	IC(OP AMP X2)	
IC7 -9		NJM4565L	IC(OP AMP X2)	
IC10		SM5813APT	IC(DIGITAL FILTER)	

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IC11		*	SAAT350	IC(DAC)		
IC12		*	TA1547	IC(OP AMP X2)		
IC13-16			NJN55320	TRANSISTOR		
Q1			2SC2458(Y,GR)	TRANSISTOR		
Q2			2SC3311A(Q,R)	TRANSISTOR		
Q3			2SC1923(R,Ø)	TRANSISTOR		
Q4			2SC2458(Y,GR)	TRANSISTOR		
Q5			2SC3311A(Q,R)	TRANSISTOR		
Q6			2SA1048(Y,GR)	TRANSISTOR		
Q7			2SA1309A(Q,R)	TRANSISTOR		
Q8			2SC2458(Y,GR)	TRANSISTOR		
Q9			2SC3311A(Q,R)	TRANSISTOR		
Q10			DTA124ES	DIGITAL TRANSISTOR		
Q11			DTA124ES	DIGITAL TRANSISTOR		
Q12			DTA124ES	DIGITAL TRANSISTOR		
Q13			DTA124ES	DIGITAL TRANSISTOR		
Q14			DTA124ES	DIGITAL TRANSISTOR		
Q15			DTA124ES	DIGITAL TRANSISTOR		
Q16			DTA124ES	DIGITAL TRANSISTOR		
Q17			DTA124ES	DIGITAL TRANSISTOR		
Q18			DTA124ES	DIGITAL TRANSISTOR		
Q19			DTA124ES	DIGITAL TRANSISTOR		
Q20			DTA124ES	DIGITAL TRANSISTOR		
Q21			DTA124ES	DIGITAL TRANSISTOR		
Q22			DTA124ES	DIGITAL TRANSISTOR		
Q23			DTA124ES	DIGITAL TRANSISTOR		
Q24			DTA124ES	DIGITAL TRANSISTOR		
Q25			DTA124ES	DIGITAL TRANSISTOR		
Q26			DTA124ES	DIGITAL TRANSISTOR		
Q27			DTA124ES	DIGITAL TRANSISTOR		
Q28			DTA124ES	DIGITAL TRANSISTOR		
Q29			DTA124ES	DIGITAL TRANSISTOR		
Q30			DTA124ES	DIGITAL TRANSISTOR		
Q31			DTA124ES	DIGITAL TRANSISTOR		
Q32			DTA124ES	DIGITAL TRANSISTOR		
Q33			DTA124ES	DIGITAL TRANSISTOR		
Q34			DTA124ES	DIGITAL TRANSISTOR		
Q35			DTA124ES	DIGITAL TRANSISTOR		
Q36			DTA124ES	DIGITAL TRANSISTOR		
Q37			DTA124ES	DIGITAL TRANSISTOR		
Q38			DTA124ES	DIGITAL TRANSISTOR		
Q39			DTA124ES	DIGITAL TRANSISTOR		
Q40			DTA124ES	DIGITAL TRANSISTOR		
Q41			DTA124ES	DIGITAL TRANSISTOR		
Q42			DTA124ES	DIGITAL TRANSISTOR		
Q43			DTA124ES	DIGITAL TRANSISTOR		
Q44			DTA124ES	DIGITAL TRANSISTOR		
Q45			DTA124ES	DIGITAL TRANSISTOR		
Q46			DTA124ES	DIGITAL TRANSISTOR		
Q47			DTA124ES	DIGITAL TRANSISTOR		
Q48			DTA124ES	DIGITAL TRANSISTOR		

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A1	2F		W02-1114-05	OSCILLATING MODULE(ØPT. OUTPUT)		
VIDEO UNIT (X35-2100-00)						
C1			CC45FSL1H101J	CERAMIC		
C2			CF92FV1H103J	MF		
C3			CC45FSL1H107J	CERAMIC		
C4			CC45FSL1H107J	CERAMIC		
C5			CC45FSL1H107J	CERAMIC		
C6			CC45FSL1H107J	CERAMIC		
C7			CC45FSL1H107J	CERAMIC		
C8			CC45FSL1H107J	CERAMIC		
C9			CC45FSL1H107J	CERAMIC		
C10			CC45FSL1H107J	CERAMIC		
C11			CC45FSL1H107J	CERAMIC		
C12			CC45FSL1H107J	CERAMIC		
C13			CC45FSL1H107J	CERAMIC		
C14			CC45FSL1H107J	CERAMIC		
C15			CC45FSL1H107J	CERAMIC		
C16			CC45FSL1H107J	CERAMIC		
C17			CC45FSL1H107J	CERAMIC		
C18			CC45FSL1H107J	CERAMIC		
C19			CC45FSL1H107J	CERAMIC		
C20			CC45FSL1H107J	CERAMIC		
C21			CC45FSL1H107J	CERAMIC		
C22			CC45FSL1H107J	CERAMIC		
C23			CC45FSL1H107J	CERAMIC		
C24			CC45FSL1H107J	CERAMIC		
C25			CC45FSL1H107J	CERAMIC		
C26			CC45FSL1H107J	CERAMIC		
C27			CC45FSL1H107J	CERAMIC		
C28			CC45FSL1H107J	CERAMIC		
C29			CC45FSL1H107J	CERAMIC		
C30			CC45FSL1H107J	CERAMIC		
C31			CC45FSL1H107J	CERAMIC		
C32			CC45FSL1H107J	CERAMIC		
C33			CC45FSL1H107J	CERAMIC		
C34			CC45FSL1H107J	CERAMIC		
C35			CC45FSL1H107J	CERAMIC		
C36			CC45FSL1H107J	CERAMIC		
C37			CC45FSL1H107J	CERAMIC		
C38			CC45FSL1H107J	CERAMIC		
C39			CC45FSL1H107J	CERAMIC		
C40			CC45FSL1H107J	CERAMIC		
C41			CC45FSL1H107J	CERAMIC		
C42			CC45FSL1H107J	CERAMIC		
C43			CC45FSL1H107J	CERAMIC		
C44			CC45FSL1H107J	CERAMIC		
C45			CC45FSL1H107J	CERAMIC		
C46			CC45FSL1H107J	CERAMIC		
C47			CC45FSL1H107J	CERAMIC		
C48			CC45FSL1H107J	CERAMIC		
C49			CC45FSL1H107J	CERAMIC		
C50			CC45FSL1H107J	CERAMIC		
C51			CC45FSL1H107J	CERAMIC		
C52			CC45FSL1H107J	CERAMIC		
C53			CC45FSL1H107J	CERAMIC		
C54			CC45FSL1H107J	CERAMIC		
C55			CC45FSL1H107J	CERAMIC		
C56			CC45FSL1H107J	CERAMIC		
C57			CC45FSL1H107J	CERAMIC		
C58			CC45FSL1H107J	CERAMIC		
C59			CC45FSL1H107J	CERAMIC		
C60			CC45FSL1H107J	CERAMIC		
C61			CC45FSL1H107J	CERAMIC		
C62			CC45FSL1H107J	CERAMIC		
C63			CC45FSL1H107J	CERAMIC		
C64			CC45FSL1H107J	CERAMIC		
C65			CC45FSL1H107J	CERAMIC		
C66			CC45FSL1H107J	CERAMIC		

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13

Ref. No. 参照番号	Address 位置	Parts No. 部品番号	Description 部品名 / 規格	Re- marks 備考
C67		CE04KW1A470M	ELECTR0	
C68 -70		CE04KW1A101M	ELECTR0	
C71		CE04FSL1H103Z	CERAMIC	
C101		CE04FSL1H820J	CERAMIC	
C102		CE04FSL1H103Z	CERAMIC	
C103		CE04FSL1H101J	CERAMIC	
C104		CE04FSL1H102J	CERAMIC	
C105, 106		CE04FSL1H103C	CERAMIC	
C107		CE04FSL1H103J	CERAMIC	
C109, 110		CE04FSL1H182J	CERAMIC	
C111		CE04FSL1H102J	CERAMIC	
C112		CE04FSL1H182J	CERAMIC	
C113		CE04FSL1H224J	CERAMIC	
C114		CE04FSL1H333J	CERAMIC	
C115		CE04FSL1H221J	CERAMIC	
C117		CE04FSL1H100D	CERAMIC	
C118, 119		CE04FSL1H103J	CERAMIC	
C120		CE04FSL1H220J	CERAMIC	
C121		CE04FSL1H330J	CERAMIC	
C122		CE04FSL1H390J	CERAMIC	
C123		CE04FSL1H680J	CERAMIC	
C124		CE04FSL1H103Z	CERAMIC	
C127		CE04FSL1H222J	CERAMIC	
C129		CE04FSL1H470J	CERAMIC	
C130		CE04FSL1H103Z	CERAMIC	
C131-134		CE04KW1V100M	ELECTR0	
C200		CE04FSL1H102J	CERAMIC	
C201		CE04FSL1H100D	CERAMIC	
C203		CE04FSL1H390J	CERAMIC	
C204		CE04FSL1H100D	CERAMIC	
C205		CE04FSL1H560J	CERAMIC	
C206		CE04FSL1H100D	CERAMIC	
C208		CE04FSL1H390J	CERAMIC	
C209		CE04FSL1H100D	CERAMIC	
C210		CE04FSL1H560J	CERAMIC	
C211		CE04FSL1H104J	CERAMIC	
C213		CE04KW1H010M	ELECTR0	
C214		CE04FSL1H561J	CERAMIC	
C215		CE04KW1A470M	ELECTR0	
C216		CE04FSL1H101J	CERAMIC	
C217		CE04FSL1H270J	CERAMIC	
C218		CE04FSL1H103J	CERAMIC	
C219		CE04FSL1H270J	CERAMIC	
C220		CE04FSL1H221J	CERAMIC	
C221		CE04FSL1H101J	CERAMIC	
C222		CE04KW1H010M	ELECTR0	
C223		CE04FSL1H104J	CERAMIC	
C224, 225		CE04FSL1H103Z	CERAMIC	
C226		CE04KW1H010M	ELECTR0	
C227		CE04FSL1H223J	CERAMIC	
C228		CE04FSL1H102J	CERAMIC	
C231		CE04FSL1H271K	CERAMIC	
C232		CE04FSL1H120J	CERAMIC	
C233		CE04KW1V100M	ELECTR0	
C234		CE04KW1H010M	ELECTR0	

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Ref. No. 参照番号	Address 位置	Parts No. 部品番号	Description 部品名 / 規格	Re- marks 備考
C235, 236		CE04KW1A470M	ELECTR0	
C237		CE04KW1V100M	ELECTR0	
C238		CE04FSL1H030C	CERAMIC	
C239		CE04FSL1H560J	CERAMIC	
C240		CE04FSL1H102J	CERAMIC	
C241		CE04FSL1H030C	CERAMIC	
C242		CE04FSL1H560J	CERAMIC	
C243		CE04FSL1H104J	CERAMIC	
C244, 245		CE04KW1V47M	ELECTR0	
C246, 247		CE04KW1E101M	ELECTR0	
C248, 249		CE04KW1V100M	ELECTR0	
C256, 257		CE04KW1C472M	ELECTR0	
C258, 259		CE04KW1V47M	ELECTR0	
C260, 261		CE04KW1A101M	ELECTR0	
C262, 263		CE04FSL1H103Z	CERAMIC	
C264, 265		CE04KW1A471M	ELECTR0	
C266		CE04FSL1H562J	CERAMIC	
C267		CE04FSL1H560J	CERAMIC	
C268		CE04FSL1H102J	CERAMIC	
C269		CE04KW1HR33M	ELECTR0	
C270		CE04FSL1H103J	CERAMIC	
C271		CE04KW1A471M	ELECTR0	
TC1		C05-0302-05	TRIMMER CAPACITOR(11PF)<VCO>	
J1, 2	1D	556-0010-05	CYLINDRICAL RECTANGLE(S-VIBRO)	
J3	1D	E63-0079-05	PHONO JACK(VIDEO OUT)	
L1		L39-1315-05	MATCHING COIL	
L2, 3		L40-1001-17	SMALL FIXED INDUCTOR(100H,K)	
L4, 5		L40-1501-17	SMALL FIXED INDUCTOR(150H,K)	
L6		L40-2201-17	SMALL FIXED INDUCTOR(220H,K)	
L7		L40-2701-17	SMALL FIXED INDUCTOR(270H,K)	
L8		L40-4701-17	SMALL FIXED INDUCTOR(470H,K)	
L9, -12		L40-1011-17	SMALL FIXED INDUCTOR(100H,K)	
L13		L40-2201-17	SMALL FIXED INDUCTOR(220H,K)	
L14		L40-1091-17	SMALL FIXED INDUCTOR(109H,K)	
L15		L40-1001-17	SMALL FIXED INDUCTOR(100H,K)	
L16		L40-2291-17	SMALL FIXED INDUCTOR(2.20H,K)	
L21, -23		L92-0018-05	FERRITE CORE	
L25, -28		L92-0018-05	FERRITE CORE	
L29		L40-1001-17	SMALL FIXED INDUCTOR(100H,K)	
L41		L40-1001-17	SMALL FIXED INDUCTOR(100H,K)	
L42		L40-2201-17	SMALL FIXED INDUCTOR(220H,K)	
L43		L40-1001-17	SMALL FIXED INDUCTOR(100H,K)	
L44		L40-2201-17	SMALL FIXED INDUCTOR(220H,K)	
L45		L40-1501-17	SMALL FIXED INDUCTOR(150H,K)	
L46		L76-0010-05	DELAY LINE	
L47		L79-1207-05	LC FILTER	
L48, 49		L40-1001-17	SMALL FIXED INDUCTOR(100H,K)	
L50 -53		L92-0018-05	FERRITE CORE	
VR1		R12-1616-05	TRIMMING POT 1K<DEM0,LEV>	
VR2		R12-3685-05	TRIMMING POT 10K<DROP-OUT>	
VR3		R12-1619-05	TRIMMING POT 1.7K<DOC GAIN>	
VR4		R12-1616-05	TRIMMING POT 1K<VIDEO LEVEL>	
D1		1SV147	VARIABLE CAPACITANCE DIODE	

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Ref. No. 参照番号	Address 位置	Parts No. 部品番号	Description 部品名 / 規格	Desti- nation 仕	Re- marks 備考
D4 -13		HSS104	DIODE		
D4 -13		ISS133	ZENER DIODE		
D21 -23		HZSS-1N(B2)	ZENER DIODE		
D21 -23		RD5-1BS(B2)	ZENER DIODE		
D24 -27		ERA081-004	DIODE		
D28 -34		HSS104	DIODE		
D28 -34		ISS133	DIODE		
D35 -42		HZSS-7N(B2)	ZENER DIODE		
D35 -42		RD2-7BS(B2)	ZENER DIODE		
IC1		TC74HC004AP	IC(CH08 INVERTER)		
IC2		NJM4565D	IC(OP AMP X2)		
IC3		YM3558	IC(VIDEO FM DETECTOR)		
IC4		HAI1528	IC(VIDEO PROCESSOR)		
IC5		CLX5504P	IC(NTSC CH08-CCD1H DELAYLINE)		
IC6		LVA519S	IC(SYNC SEPARATION)		
IC7 -8		TC74HC004AP	IC(CH08 INVERTER)		
IC10		TC4053BP	IC(3-INPUT 2CH MPX/DE-MPX)		
IC10		XR4053B	IC(ANALOG MULTIPLEXER)		
IC11		NJM4565D	IC(OP AMP X2)		
IC12		TC4053BP	IC(3-INPUT 2CH MPX/DE-MPX)		
IC12		XR4053B	IC(ANALOG MULTIPLEXER)		
IC13-15		NJM4565D	IC(OP AMP X2)		
IC16		TC74HC123AP	IC(MULTIVIBRATOR)		
IC17		TC74HC74P	IC(DUAL D-TYPE FLIP FLOP)		
IC21		MS0554-270SP	IC(CHARACTER GENERATOR)		
IC22		MM108XS	IC(SYNC SEPARATION)		
IC23		TC4053BP	IC(3-INPUT 2CH MPX/DE-MPX)		
IC24		XR4053B	IC(ANALOG MULTIPLEXER)		
IC25		NJM4565D	IC(OP AMP X2)		
IC26		TC74HC123AP	IC(MULTIVIBRATOR)		
Q1 -2		NJM4565D	IC(OP AMP X2)		
Q3		2SC1923(R,0)	TRANSISTOR		
Q3		2SC2458(Y,GR)	TRANSISTOR		
Q4		2SC3311A(Q,R)	TRANSISTOR		
Q5 -7		2SA1309A(Q,R)	TRANSISTOR		
Q5 -7		2SC3311A(Q,R)	TRANSISTOR		
Q8		DT0124ES	DIGITAL TRANSISTOR		
Q9		2SC2458(Y,GR)	TRANSISTOR		
Q9		2SC3311A(Q,R)	TRANSISTOR		
Q10 -11		2SC1923(R,0)	TRANSISTOR		
Q12 -14		2SC2458(Y,GR)	TRANSISTOR		
Q12 -14		2SC3311A(Q,R)	TRANSISTOR		
Q15 -18		2SC1923(R,0)	TRANSISTOR		
Q15 -18		2SA1048(Y,GR)	TRANSISTOR		
Q19		2SA1309A(Q,R)	TRANSISTOR		
Q20 -22		2SC2458(Y,GR)	TRANSISTOR		
Q20 -22		2SC3311A(Q,R)	TRANSISTOR		
Q23		2SA1309A(Q,R)	TRANSISTOR		
Q25		2SC2458(Y,GR)	TRANSISTOR		
Q31		2SC3311A(Q,R)	TRANSISTOR		

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Ref. No. 参照番号	Address 位置	Parts No. 部品番号	Description 部品名 / 規格	Desti- nation 仕	Re- marks 備考
Q32 -33		2SA1048(Y,GR)	TRANSISTOR		
Q32 -33		2SA1309A(Q,R)	DIGITAL TRANSISTOR		
Q34		DT0124ES	DIGITAL TRANSISTOR		
Q34		UN4212	TRANSISTOR		
Q35 -36		2SC2458(Y,GR)	TRANSISTOR		
Q35 -36		2SC3311A(Q,R)	TRANSISTOR		
Q37 -39		2SC1923(R,0)	TRANSISTOR		
Q40 -41		2SC2458(Y,GR)	TRANSISTOR		
Q40 -41		2SC3311A(Q,R)	TRANSISTOR		
Q43		2SC1923(R,0)	TRANSISTOR		
Q44		2SC2458(Y,GR)	TRANSISTOR		
Q44		2SC3311A(Q,R)	TRANSISTOR		
Q45		2SC1923(R,0)	TRANSISTOR		
Q46		2SA1048(Y,GR)	TRANSISTOR		
Q46		2SA1309A(Q,R)	TRANSISTOR		
Q47 -48		2SC2458(Y,GR)	TRANSISTOR		
Q47 -48		2SC3311A(Q,R)	TRANSISTOR		
Q49		2SA1048(Y,GR)	TRANSISTOR		
Q49		2SA1309A(Q,R)	TRANSISTOR		
Q50		2SC2458(Y,GR)	TRANSISTOR		
Q50		2SC3311A(Q,R)	DIGITAL TRANSISTOR		
Q51		DT0124ES	DIGITAL TRANSISTOR		
Q51		UN4212	TRANSISTOR		
Q52		2SD2012	TRANSISTOR		
Q52		2SD2374	TRANSISTOR		
Q53		2SB1375	TRANSISTOR		
Q53		2SB1548	FET		
Q54		2SK163(L,M)			
VIDEO UNIT : Digital (X35-2110-00)					
C1		CC73FSL1H1000	CHIP C	10PF	D
C2		CC73FSL1H390J	CHIP C	39PF	J
C3		CC73FSL1H1000	CHIP C	10PF	D
C4		CC73FSL1H560J	CHIP C	56PF	J
C5		CC73FB1B104K	CHIP C	0.10UF	K
C6		CC73FSL1H560J	CHIP C	56PF	J
C8 -10		CK73FF1B104Z	CHIP C	0.1UF	Z
C12 -13		C90-3209-05	ELECTRO	10UF	6.3WV
C14		CK73FF1B104Z	CHIP C	0.1UF	Z
C15		C90-3209-05	ELECTRO	10UF	6.3WV
C16 -17		CK73FB1H223K	CHIP C	0.022UF	K
C21		CC73FSL1H560J	CHIP C	56PF	J
C22		CC73FSL1H1000	CHIP C	10PF	D
C23		CC73FSL1H560J	CHIP C	56PF	J
C24		CC73FSL1H1000	CHIP C	10PF	D
C25 -30		CK73FF1B104Z	CHIP C	0.1UF	Z
C35		CC73FSL1H0600	CHIP C	68PF	D
C36		CC73FSL1H680J	CHIP C	68PF	J
C37		CC73FF1B104Z	CHIP C	0.1UF	Z
C38		CC73FSL1H1000	CHIP C	10PF	D
C39 -40		CK73FF1B104Z	CHIP C	0.1UF	Z
C51 -71		CK73FF1B104Z	CHIP C	0.1UF	Z
C72 -74		CK73FB1H102K	CHIP C	1000PF	K
C75 -76		CK73FF1B104Z	CHIP C	0.1UF	Z
C77		CC73FSL1H390J	CHIP C	39PF	J

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C78		CK73FE1B104Z	CHIP C 0.1UF Z	
C79		CC73FSL1H1S1J	TRIMMER 20PF(REFERENCE 8fsc)	
C80		C05-0303-05		
L1		L40-1001-31	SMALL FIXED INDUCTOR(10UH,K)	
L2		L40-2201-31	SMALL FIXED INDUCTOR(22UH,K)	
L3		L40-1001-31	SMALL FIXED INDUCTOR(10UH,K)	
L4		L40-1001-31	SMALL FIXED INDUCTOR(10UH,K)	
L5		L40-6881-31	SMALL FIXED INDUCTOR(0.68UH,K)	
LX1		L77-1200-05	CRYSTAL RESONATOR(28.63636MHZ)	
D1		1SV169	VARIABLE CAPACITANCE DIODE	
D2		MA110	DIODE	
IC1		CD11176Q	IC(A/D CONVERTER)	
IC2		CD11177Q	IC(D/A CONVERTER)	
IC3		TC7S04F	IC(2CH NAND GATE)	
IC4		KAG03	CUSTOM IC(TBC, FIELD SYNC.)	
IC5, 6		CKX1206AM	IC(FIELD MEMORY)	
IC7, 8		MN4260S	IC(LINE MEMORY)	
IC9		KAG04	CUSTOM IC(DIGITAL COMB FILTER)	
IC10		KAG05	CUSTOM IC(DIMENSION, YC SEPA)	
IC11-13		TMS4C1070B-30N	IC(MEMORY)	
IC14		KAM01	CUSTOM IC(DIGITAL COLOR NR)	
IC15, 16		HM53051FP-45	IC(RAM)	
IC17		KAND1	CUSTOM IC(COLOR B.P.F.)	
IC18		TC74HC04AF	IC(HEX INVERTER SMD)	
IC19		TC74HC4538AF	IC(DUAL MULTIVIBRATOR)	
IC20		TC7500P	IC(2CH NAND GATE)	
Q1		2SC2412K	TRANSISTOR	
Q2		2SA1037K	TRANSISTOR	
Q3		2SC2412K	TRANSISTOR	
Q4, 5		2SA1037K	TRANSISTOR	
Q6		2SC2412K	TRANSISTOR	
Q7		2SA1037K	TRANSISTOR	
Q8		2SC2412K	TRANSISTOR	
Q9, 10		2SA1037K	TRANSISTOR	
Q11		DT0124EK	DIGITAL TRANSISTOR	
MECHANISM ASSY (X92-1620-41)				
1	3A	A10-2846-01	CHASSIS	
2	2B	A11-0707-23	SUB CHASSIS CALKING ASSY	
4	2B	A11-0709-13	SUB CHASSIS ASSY	
6	1A	A11-0772-03	SUB CHASSIS CALKING ASSY	
7	1B	A11-0776-03	SUB CHASSIS	
8	2B	A11-0774-03	SUB CHASSIS CALKING ASSY	
9	2A	A21-1819-03	DRESSING PANEL	
11	3A	D10-3128-04	ARM	
13	2A	D10-3130-04	ARM	
14	2B	D10-3131-04	ROD	
15	3A	D10-3133-14	SLIDER ASSY	
16	3B	D12-0129-03	CAM	
18	2A	D13-0919-04	GEAR	
19	2A	D13-0920-04	GEAR	
20	2A	D13-0921-04	GEAR	
25	2A	D13-0922-04	GEAR	
26	2A	D13-0923-04	GEAR	
27	2A	D13-0942-04	GEAR	

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28	2A	D13-0926-04	GEAR	
29	2A	D13-0943-14	GEAR (GEAR)	
30	2B	D13-0931-03	LACK (GEAR)	
31	2A	D15-0334-14	PULLEY	
32	2A	D16-0301-05	BELT	
33	2A	D23-0248-04	RETAINER	
42	2B	E35-0060-05	FLAT CABLE	
46	1B	G01-3502-04	COMPRESSION SPRING	
49	3B	G02-0984-04	FLAT SPRING	
50	2B	G02-0996-04	FLAT SPRING	
51	1A, 1B	G16-0770-04	SHEET	
55	1B	J11-0186-04	CLAMPER ASSY	
56	1B	J11-0183-04	CLAMPER	
57	2B	J19-3388-11	HOLDER	
58	1B	J19-3522-03	HOLDER	
60	2A	J21-5726-04	MOUNTING HARDWARE ASSY	
62	2B	J90-0670-04	RAIL	
63	1B	J99-0519-13	TRAY ASSY	
65	2B	J21-5898-04	MOUNTING HARDWARE	
-	-	J61-0081-05	WIRE BAND	
A	-	N09-2812-05	ADJUSTABLE SCREW	
B	-	N09-1515-05	TAPPING SCREW (3X8)	
C	-	N09-2749-05	MACHINE SCREW	
D	-	N09-2809-05	SET SCREW	
E	-	N09-2811-05	SEWS (TAPITE SCREW)	
F	-	N89-3004-46	BINDING HEAD TAPITE SCREW	
G	-	N19-0366-04	FLAT WASHER	
H	-	N19-0880-04	FLAT WASHER	
I	-	N84-2008-46	PAN HEAD TAPITE SCREW	
J	-	N35-2005-45	BINDING HEAD MACHINE SCREW	
K	-	N35-2603-46	BINDING HEAD MACHINE SCREW	
M	-	N09-2961-05	SEMS (MACHINE SCREW)(M3X10)	
N	-	N84-2005-46	PAN HEAD TAPITE SCREW	
P	-	N86-2610-46	BINDING HEAD TAPITE SCREW	
R	-	N89-3008-45	BINDING HEAD TAPITE SCREW	
S	-	N89-3008-46	BINDING HEAD TAPITE SCREW	
T	-	N82-2608-46	BINDING HEAD TAPITE SCREW	
U	-	N84-3008-46	PAN HEAD TAPITE SCREW	
66	2B	S64-0012-05	LEVER SWITCH(LD OPEN)	
DM	3A	T42-0618-03	MOTOR ASSY(DISC MOTOR)	
FM	3A	T42-0584-04	MOTOR ASSY(FEED MOTOR)	
LM	3A	T42-0524-05	DC MOTOR(LOADING MOTOR)	
PU	2B	X93-1000-02	OPTICAL PICKUP ASSY(VSF-1B)	

L:Scandinavia K:USA P:Canada
Y:PX(Far East, Hawaii) T:England E:Europe
Y:AAFE(S)(Europe) X:Australia M:Other Areas

△ indicates safety critical components.

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SPECIFICATIONS

Type

Video disc format Laser vision format
 Signal read mechanism Semiconductor laser
 Video output format NTSC
 Video output lines 4 lines (two S-video terminals, two RCA pin terminals)
 Audio output lines 3 lines (one optical, two RCA pin terminals)

Power Requirements

Voltage and frequency AC 120V, 60Hz (For the U.S.A.) AC 220V (For other countries)
 Power consumption 60W
 Maximum external dimensions (Width x Height x Length) 476 (18-3/4") x 163 (6-7/16") x 436 (17-3/16") mm
 Weight (standard) 20.0kg (44.1lb)

Video system

Video output level 1Vp-p (75 Ω load, sync. negative), C output : 0.286Vp-p (75 Ω load, sync. negative)
 Horizontal resolution 425 lines
 Video S/N ratio 52dB or above

Digital Audio System

Frequency 4Hz ~ 20kHz (EIAJ)
 Sound to noise ratio 105dB or above (EIAJ)
 Dynamic range 98dB or above (EIAJ)
 Overall harmonic distortion 0.0015% (1kHz) or below (EIAJ)
 Wow & Flutter Below measurable levels ($\pm 0.001\%$ W.PEAK) (EIAJ)
 Output level / Impedance 2V / 100 Ω
 Optical output (optical fiber terminal) -15dBm ~ -21dBm (Wave length 660nm)
 Operating temperature 5°C ~ 40°C
 Operating humidity 5% ~ 90% (to prevent condensation)

KENWOOD follows a policy of continuous advancements in development. For this reason specifications may be changed without notice.

Note :

Component and circuitry are subject to modification to insure best operation under differing local conditions. This manual is based on, the U.S.A. (K) standard, and provides information on regional circuit modification through use of alternate schematic diagrams, and information on regional component variations through use of parts list.

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