Ref. No. 3980
032007

ONKYO SERVICE MANUAL

COMPACT DISC PLAYER
MODEL DX-7355

RC-686C

Black, Silver and Golden models

B MPP	230 AC, 50Hz
S MPP	230 AC, 50Hz
G MGR	220-230V AC, 50/60Hz
G MWT	120V/220-240V AC, 50/60Hz

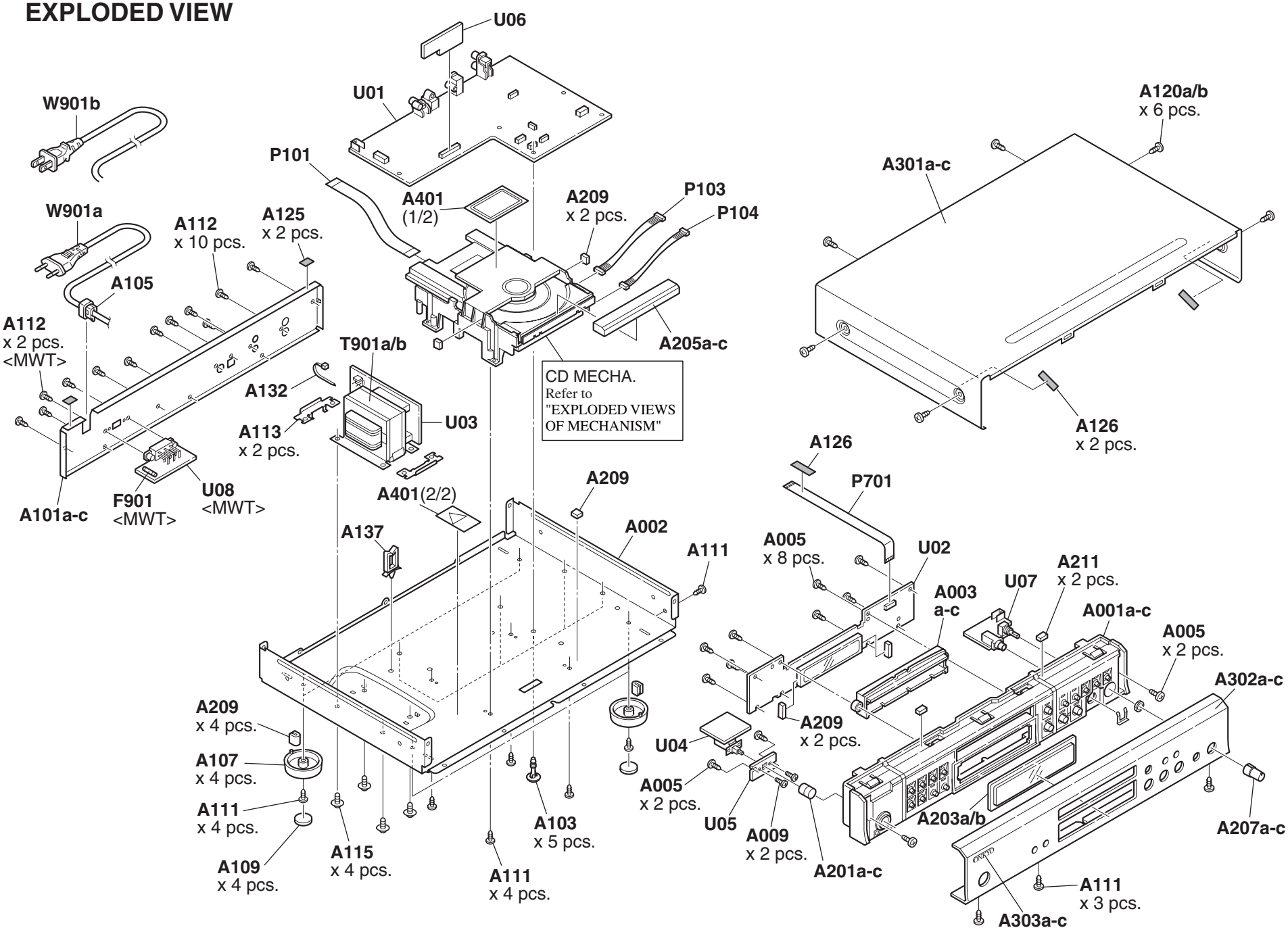
SAFETY-RELATED COMPONENT WARNING!!

COMPONENTS IDENTIFIED BY MARK ⚠ ON THE SCHEMATIC DIAGRAM AND IN THE PARTS LIST ARE CRITICAL FOR RISK OF FIRE AND ELECTRIC SHOCK. REPLACE THESE COMPONENTS WITH ONKYO PARTS WHOSE PART NUMBERS APPEAR AS SHOWN IN THIS MANUAL.

MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

ONKYO®
IMAGINATIVE SIGHT & SOUND

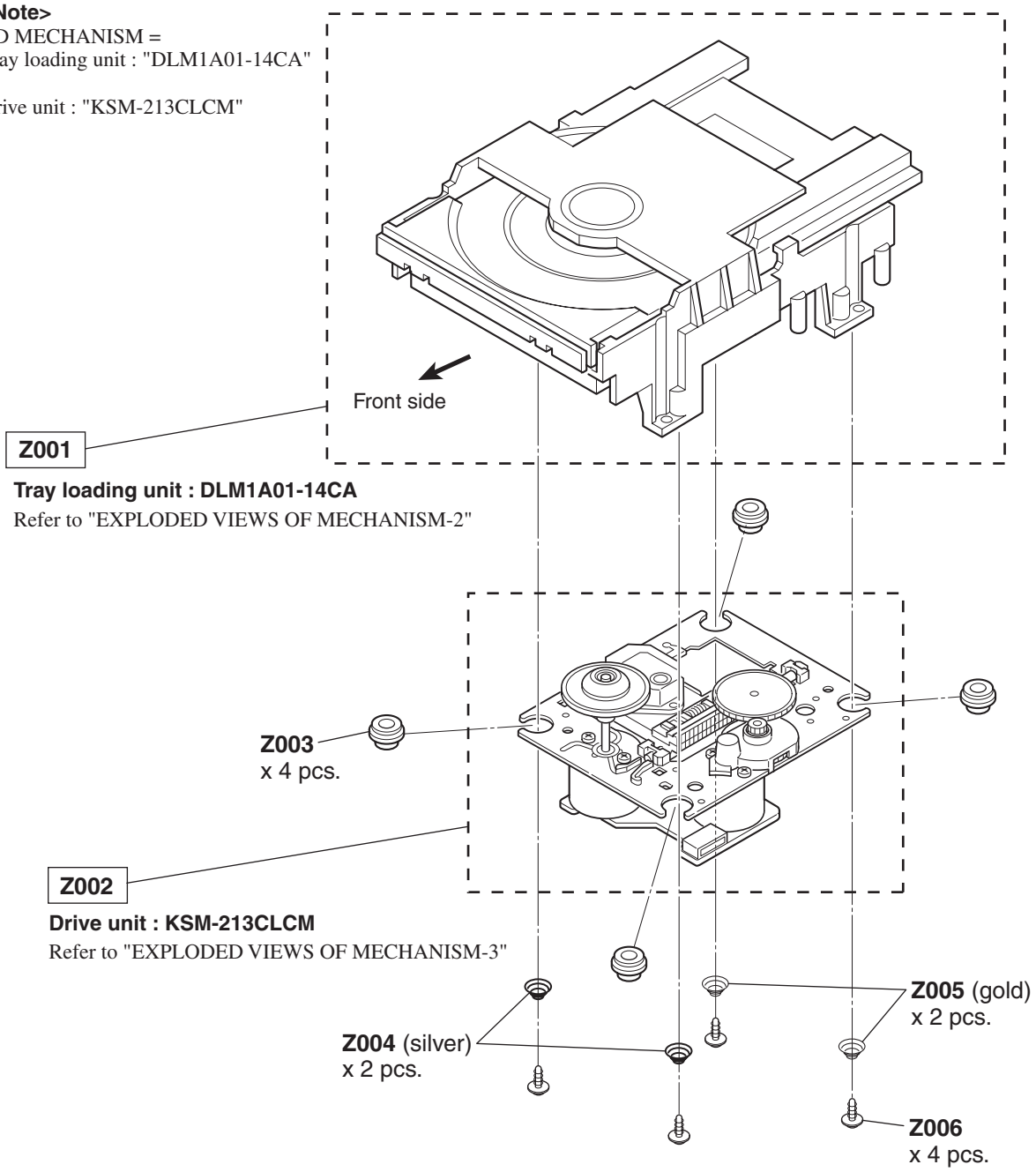
EXPLODED VIEW



EXPLODED VIEWS OF MECHANISM-1

CD MECHANISM : DLM1A01-14CA + KSM-213CLCM

<Note>
CD MECHANISM =
Tray loading unit : "DLM1A01-14CA"
+
Drive unit : "KSM-213CLCM"

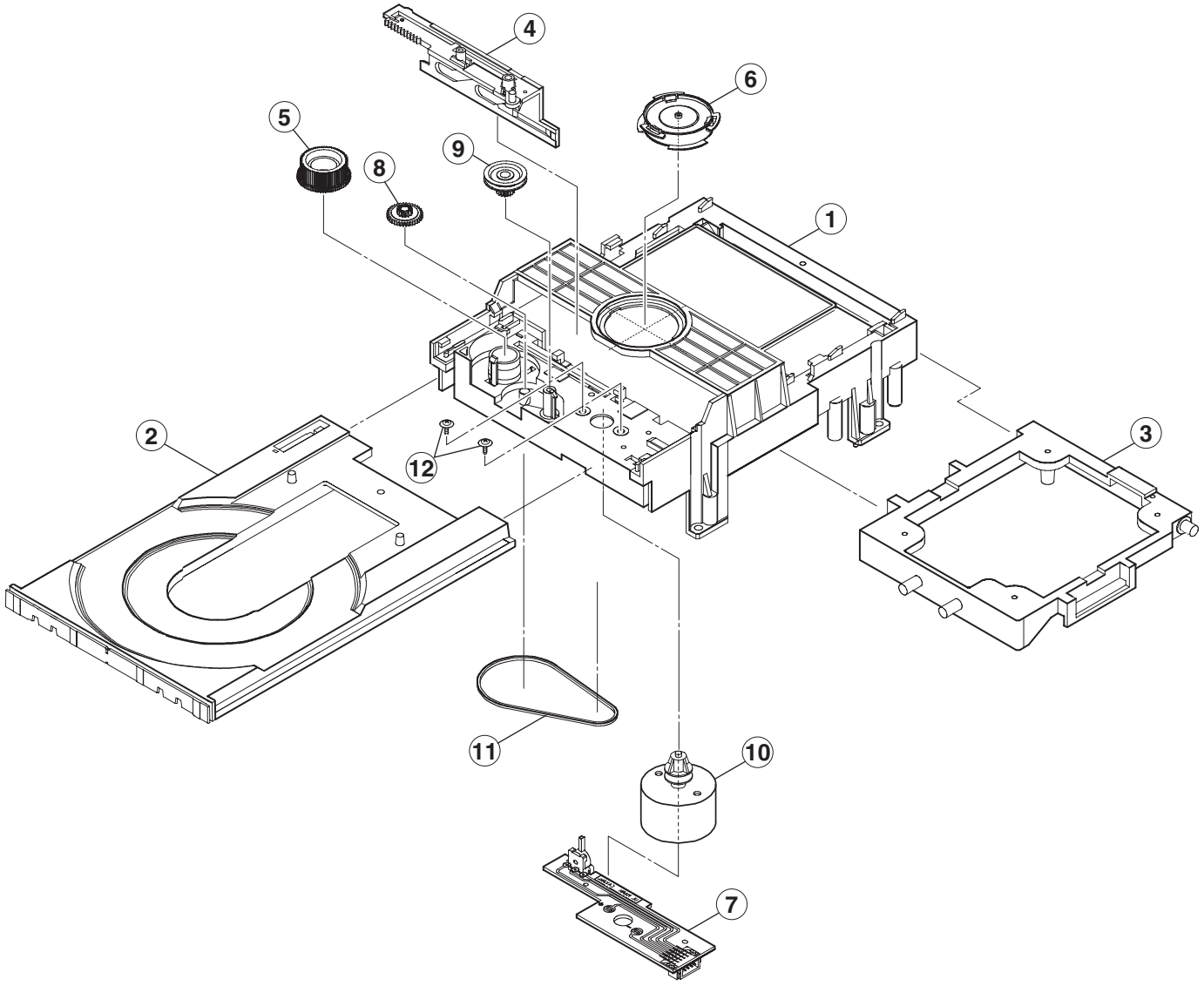


PARTS LIST

REF. NO.	PART NO. (SN)	PART NAME	DESCRIPTION	Q'TY
Z001	24800056	CD Tray Loading unit	DLM1A01-14CA	1
Z002	24800017	CD Drive unit	KSM-213CLCM	1
Z003	24818058	INSULATOR	(CDC-A)	4
Z004	24820071	SPRING	TP-D (silver)	2
Z005	24820072	SPRING	TP-E (gold)	2
Z006	801632	SCREW	2.6 x 8 x W10	4

EXPLODED VIEWS OF MECHANISM-2

CD TRAY LOADING UNIT : DLM1A01-14CA

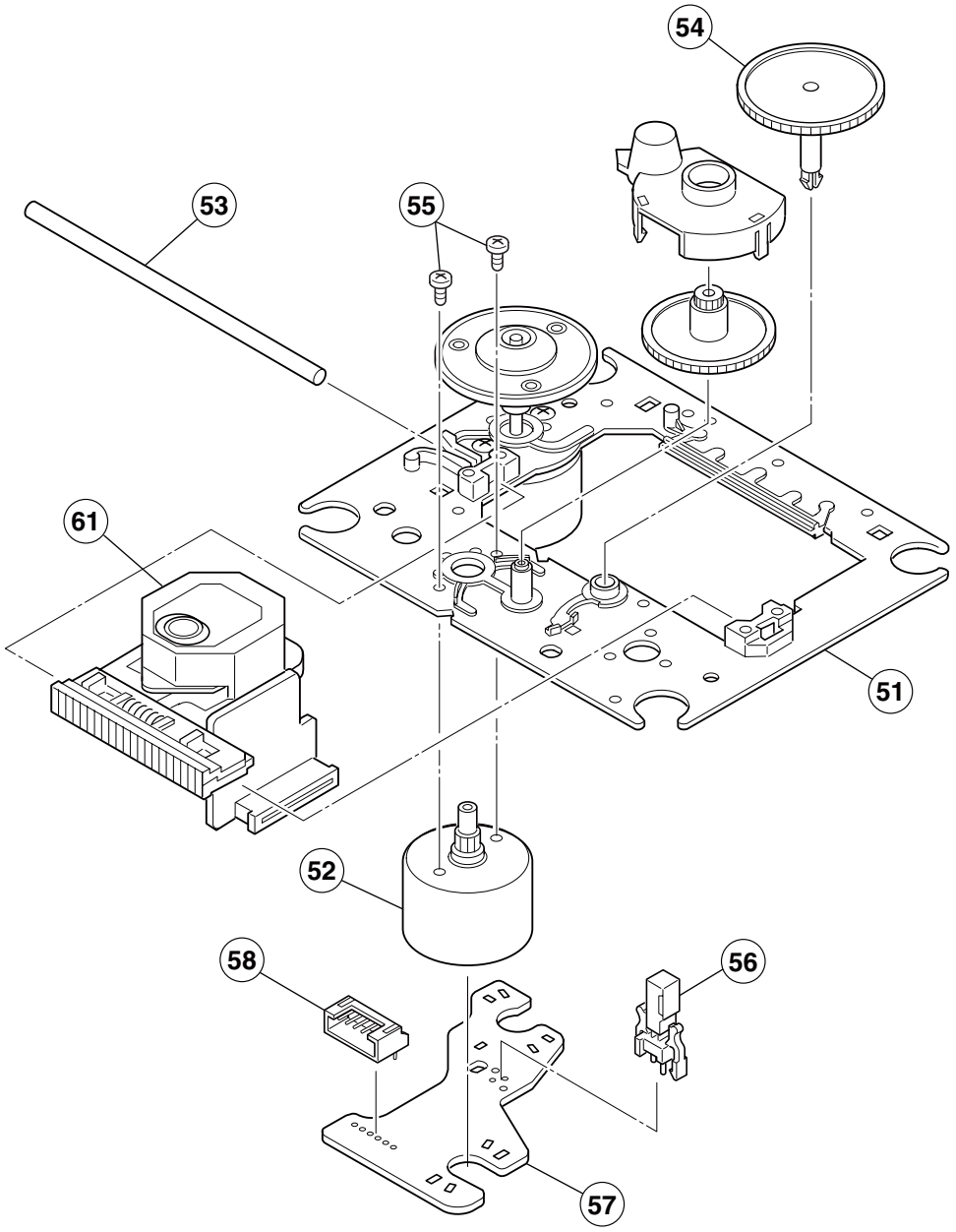


PARTS LIST

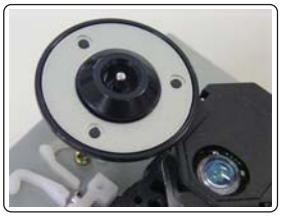
REF. NO.	PART NO. (SN)	DESCRIPTION	Q'TY
1	65-210-1054	CHASSIS	1
2	65-218-1055	TRAY	1
3	65-211-2040	SUB CHASSIS	1
4	65-239-2004	CAM SLIDER	1
5	65-222-3005	GEAR TRAY	1
6	65-093-4057H	CLAMPER ASS'Y	1
7	65-093-4058H	PWB ASS'Y	1
8	65-222-4037	GEAR A	1
9	65-222-4004	PULLEY GEAR	1
10	65-093-4068H	MOTOR ASS'Y	1
11	02-083-4274	LOADING BELT	1
12	GSP14A25027	SCREW	2

EXPLODED VIEWS OF MECHANISM-3

CD DRIVE UNIT : KSM-213CLCM



OK

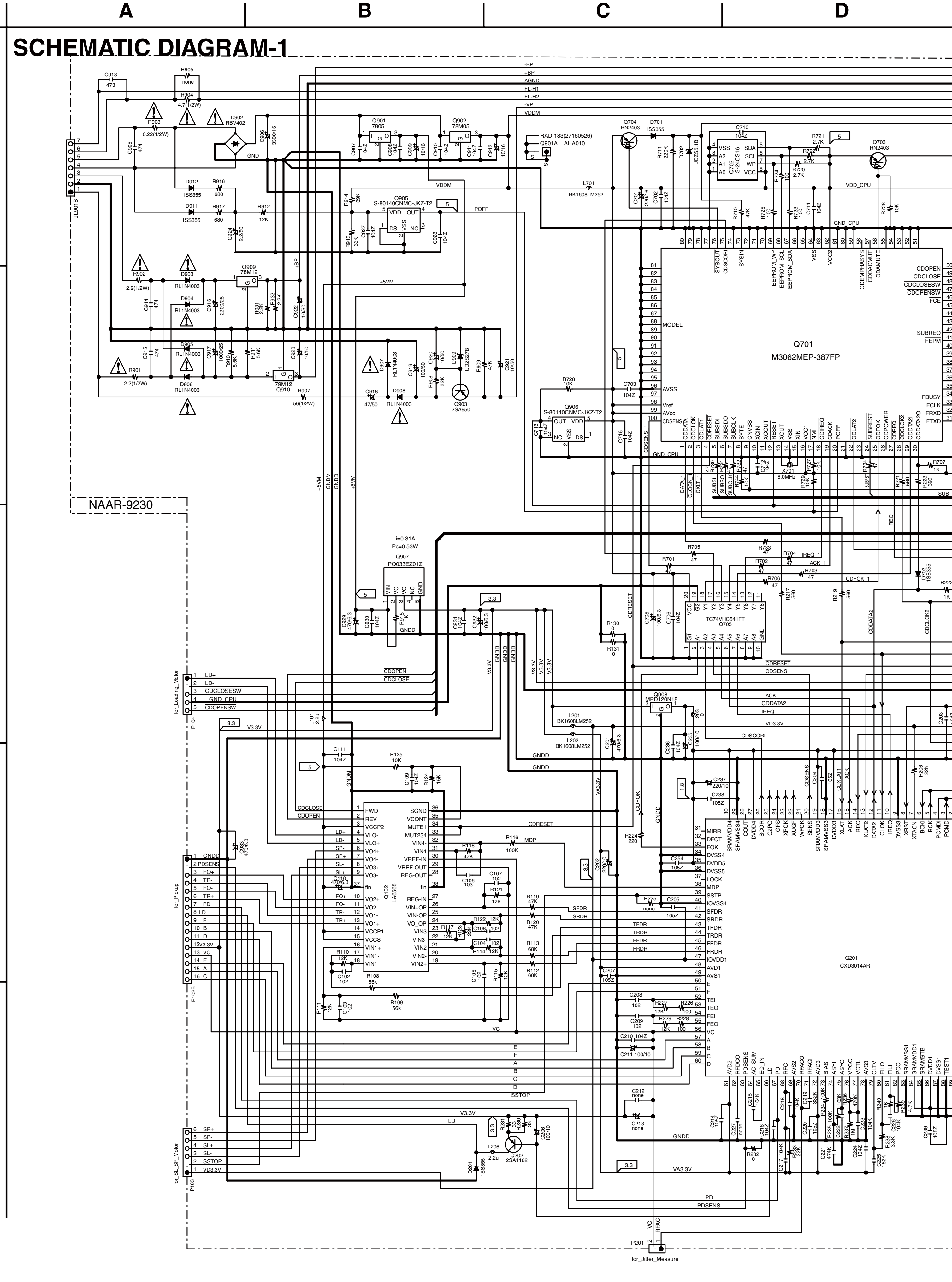


NG

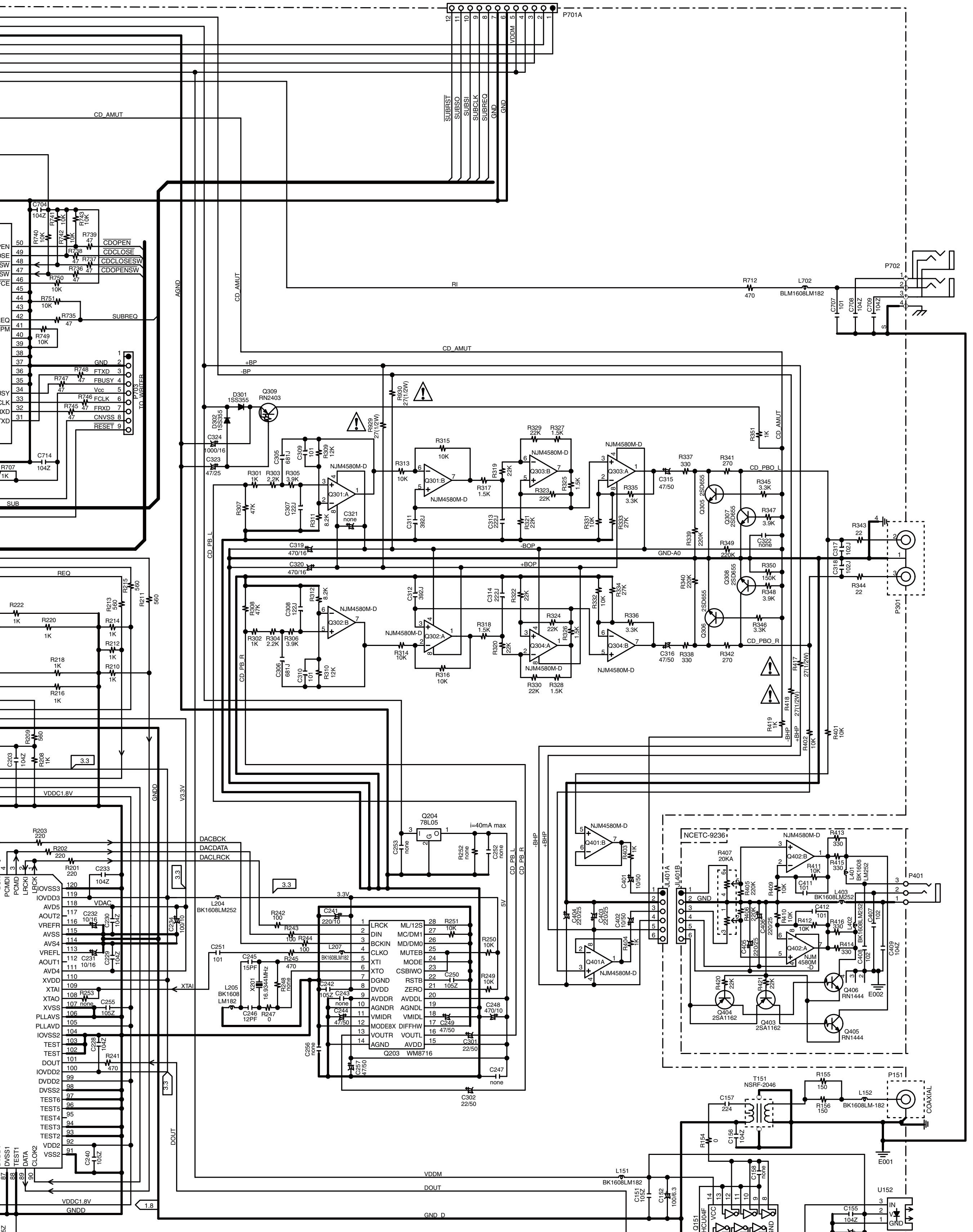
PARTS LIST

REF. NO.	PART NO. (SN)	DESCRIPTION	Q'TY
51	X-2625-877-1	Motor chassis ass'y	1
52	X2625-769-1	Motor gear ass'y	1
53	2626-908-01	Sled shaft	1
54	24810023	Gear (A) (S)	1
55	7621-255-15	P2 x 3, Screw	2
56	24840008	Leaf switch	1
57	1639-678-12	Motor PC board	1
58	1-564-722-11	Connector 6pin	1
61	8848-483-05	KSS-213C, Pickup	1

SCHEMATIC DIAGRAM-1



E	F	G	H



CAUTION

FOR CONTINUED PROTECTION AGAINST FIRE HAZARD, REPLACE ONLY WITH FUSE OF SAME TYPE AND RATING INDICATED.

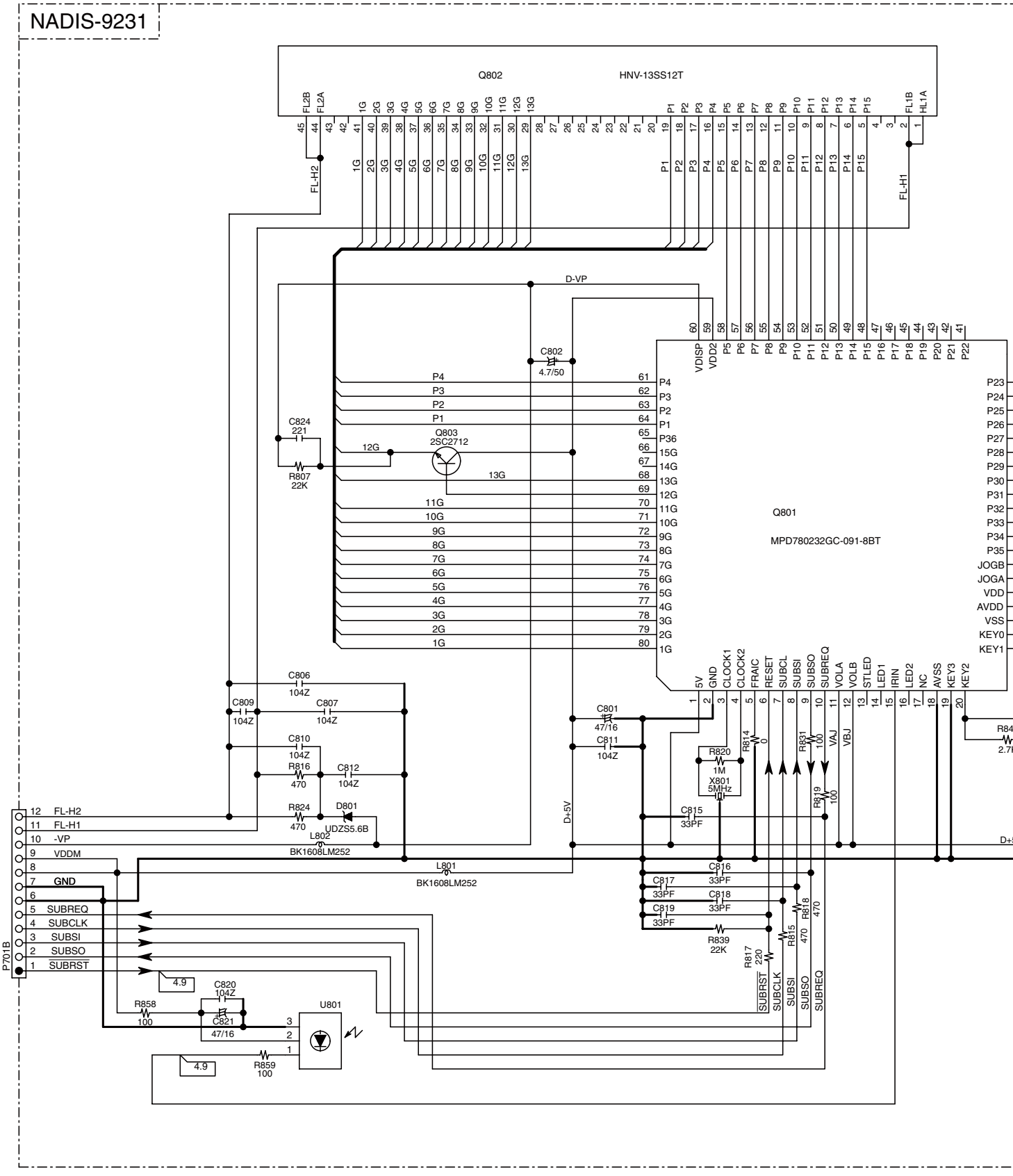
ATTENTION

AFIN D'ASSURER UNE PROTECTION PERMANENTE CONTRE LES RISQUES D'INCENDIE, REMPLACER UNIQUEMENT PAR UN FUSIBLE DE MEME TYPE ET CALIBRATION COMME INDIQUE.

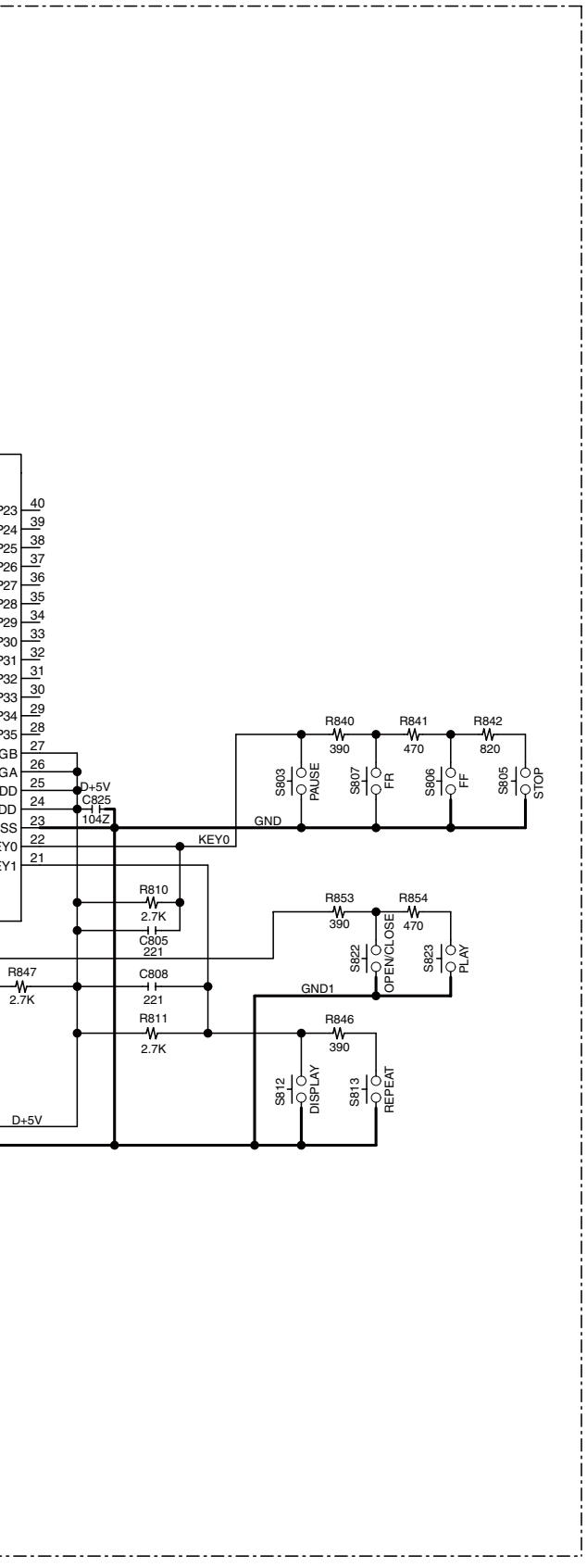
THIS SYMBOL LOCATED NEAR THE FUSE INDICATES THAT THE FUSE USED IS SLOW OPERATING TYPE FOR CONTINUED PROTECTION AGAINST FIRE FUSE HAZARD,REPLACE WITH SAME TYPE FUSE. FOR FUSE RATING REFER TO THE MAKING ADJACENT TO THE SYMBOL.

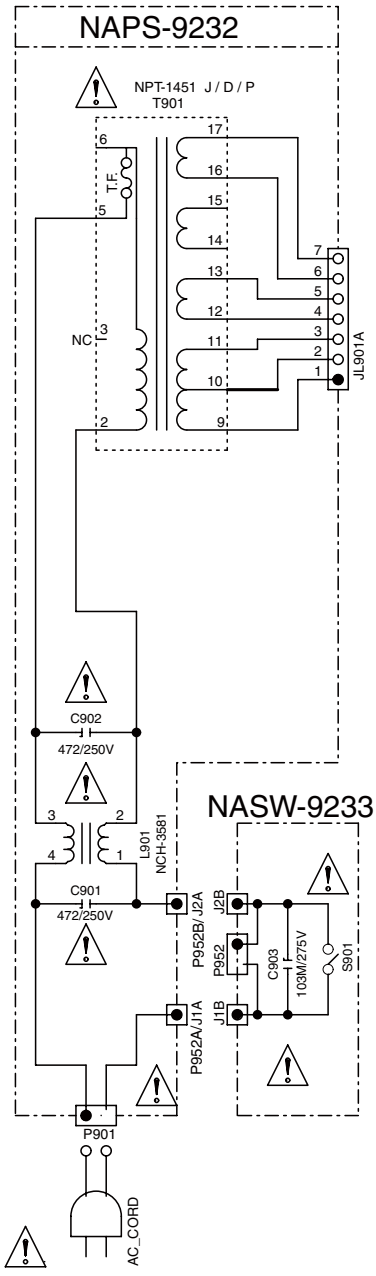
CE SYMBOLE INDIQUE QUE LE FUSIBLE UTLISE EST A LENT, E POUR UNE PROTECTION PERMANENTE,N'UTILISER QUE DES FUSIBLES DE MEME TYPE. CE DARNIER EST INDIQUE LA QU LE PRESENT SYMBOL EST APPOSE.

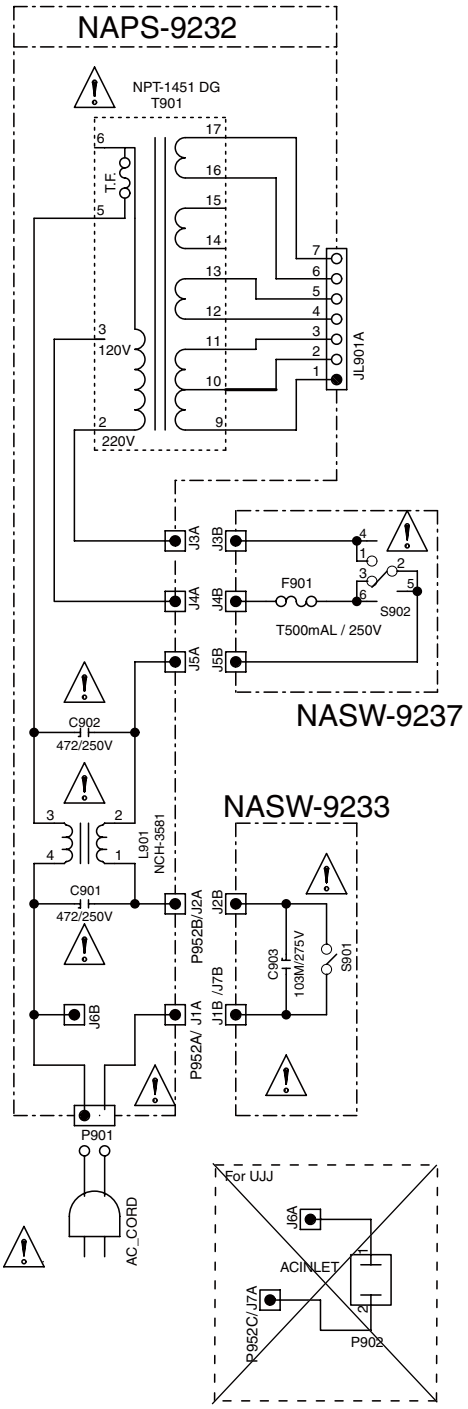
SCHEMATIC DIAGRAM-2



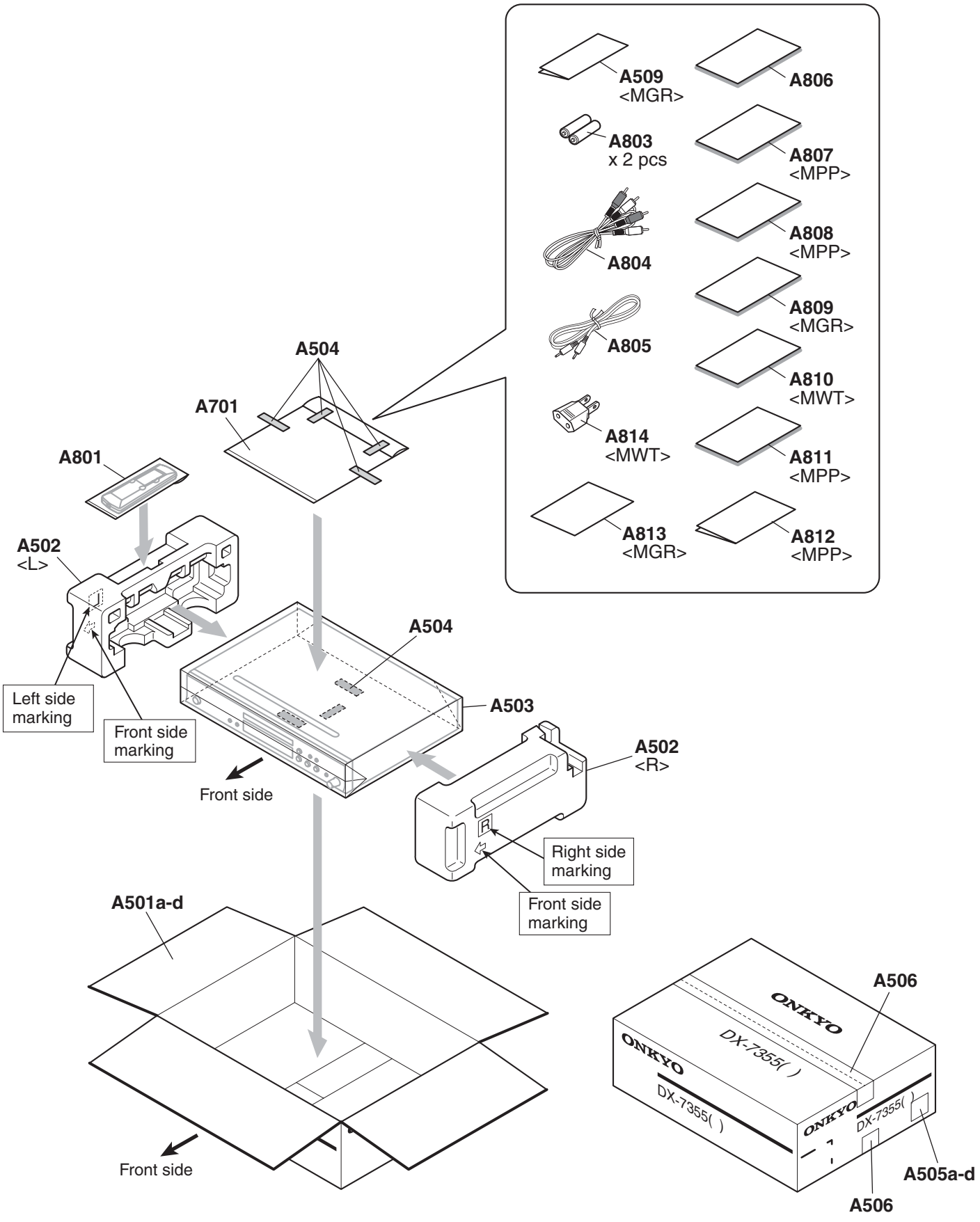
E F G H


P23 40
P24 39
P25 38
P26 37
P27 36
P28 35
P29 34
P30 33
P31 32
P32 31
P33 30
P34 29
P35 28
GB 27
GA 26
DD 25
DD 24
SS 23
EY0 22
EY1 21
D+5V
C825
104Z
GND
KEY0
R840
390
R841
470
R842
820
S803
PAUSE
S807
FR
S806
FF
S805
STOP
R810
2.7K
C805
221
R853
390
R854
470
S822
OPEN/CLOSE
S823
PLAY
R847
2.7K
C808
221
GND1
R811
2.7K
R846
390
S812
DISPLAY
S813
REPEAT
D+5V


NAPS-9232
NPT-1451 J / D / P
T901
T.F.
NC
JL901A
C902
472/250V
C901
472/250V
L901
NCH-3581
NASW-9233
P952B/ J2A
J2B
P952
C903
103M/275V
S901
P952A/J1A
J1B
P901
AC_CORD


NAPS-9232
NPT-1451 DG
T901
T.F.
120V
220V
JL901A
J3A
J3B
J4A
J4B
J5A
J5B
F901
T500mAL / 250V
S902
NASW-9237
C902
472/250V
C901
472/250V
L901
NCH-3581
NASW-9233
P952B/J2A
J2B
C903
103M/275V
S901
J6B
P952A/ J1A
J1B /J7B
P901
AC_CORD
For UJJ
J6A
ACINLET
P952C/ J7A
P902

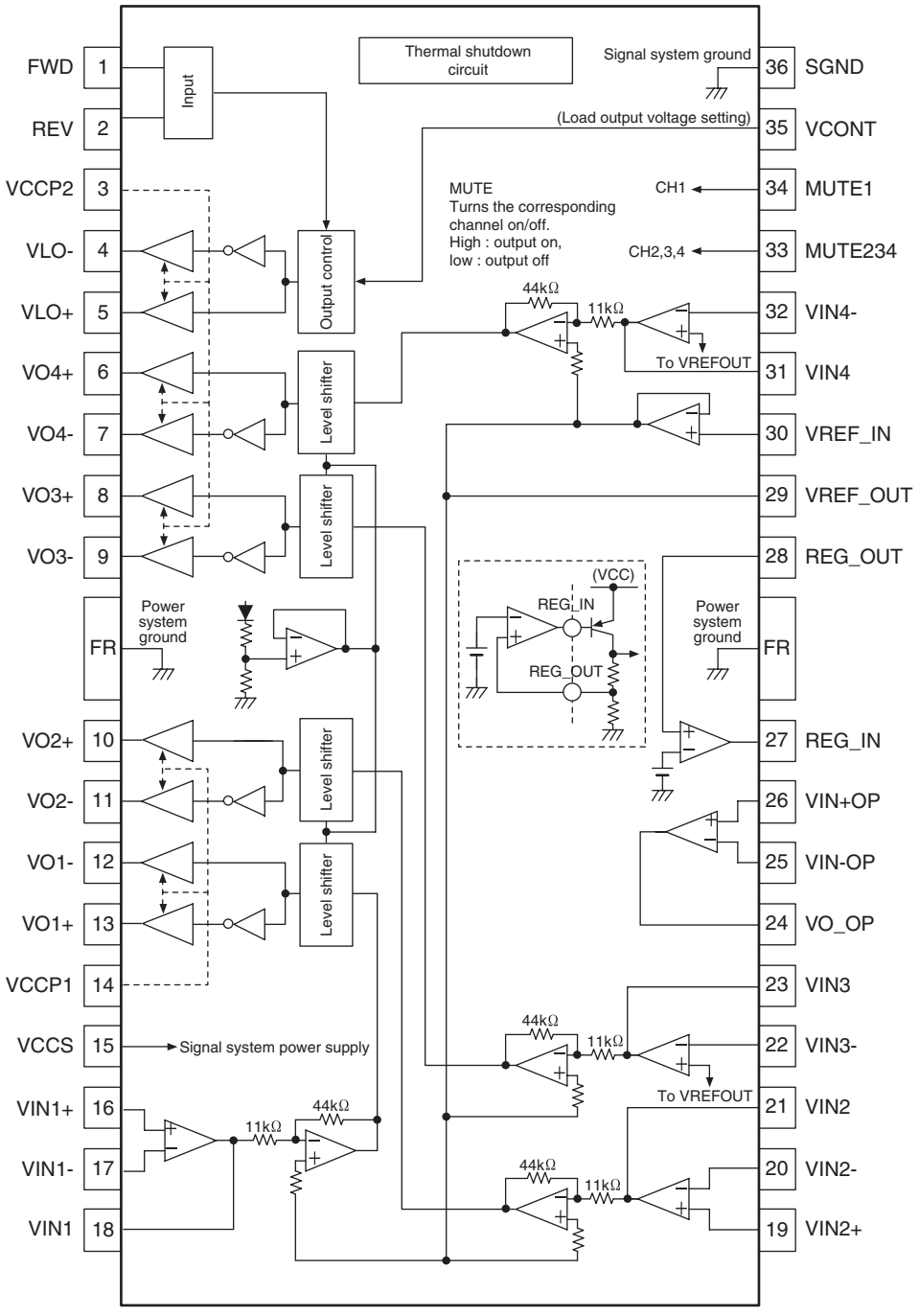
PACKING PROCEDURE



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-1

Q102 : LA6565 (Five-Channel CD Actuator Driver)-1/2

BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-2

Q102 : LA6565 (Five-Channel CD Actuator Driver)-2/2

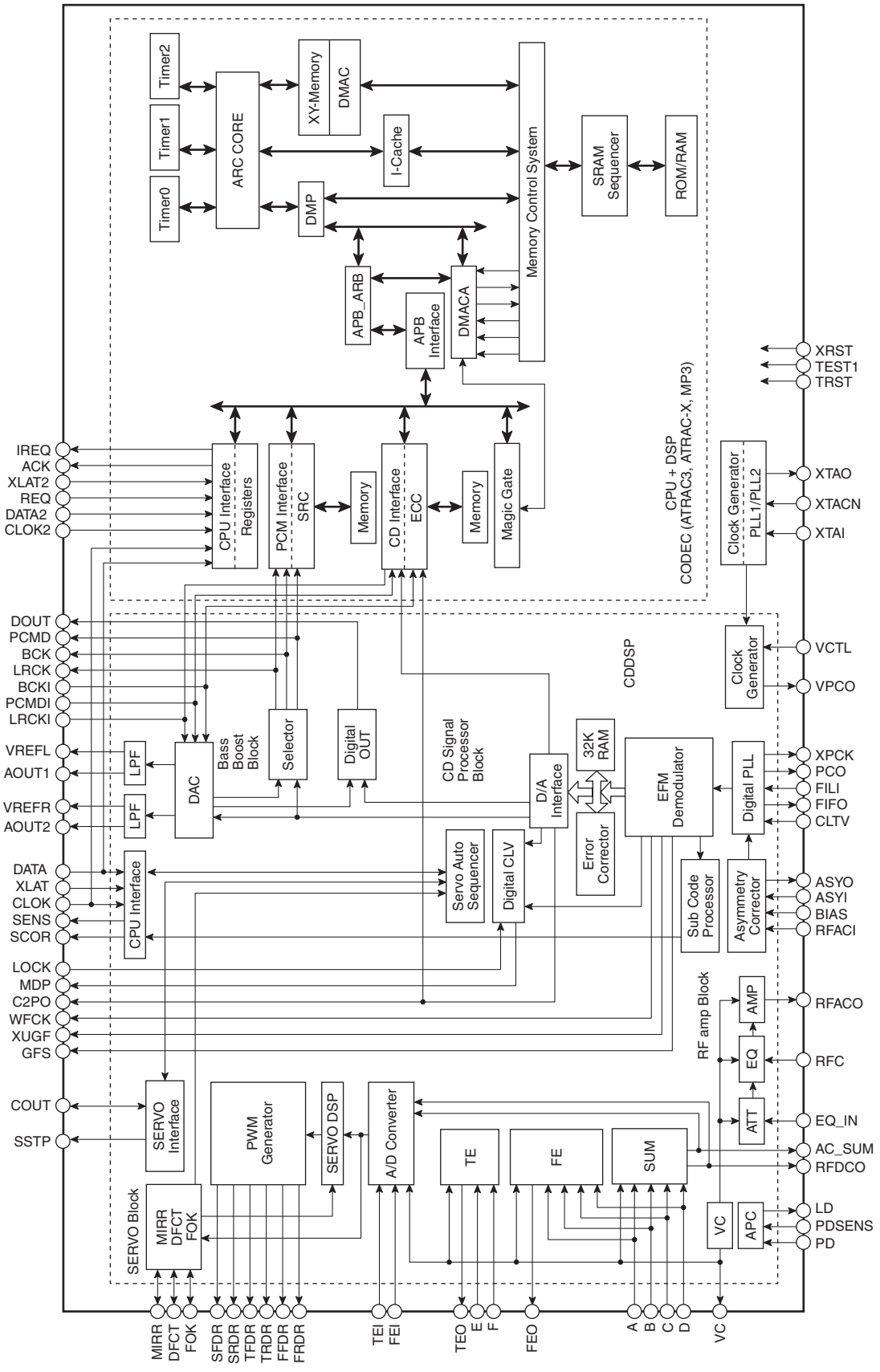
TERMINAL DESCRIPTION

Pin No.	Pin Name	Description
1	FWD	Loading output direction switching (FWD). Loading system logic input.
2	REV	Loading output direction switching (REV). Loading system logic input.
3	VCCP2	Channels 3, 4, and loading power stage power supply.
4	VLO-	Loading output (-)
5	VLO+	Loading output (+)
6	VO4+	Channel 4 output (+)
7	VO4-	Channel 4 output (-)
8	VO3+	Channel 3 output (+)
9	VO3-	Channel 3 output (-)
10	VO2+	Channel 2 output (+)
11	VO2-	Channel 2 output (-)
12	VO1-	Channel 1 output (-)
13	VO1+	Channel 1 output (+)
14	VCCP1	Channels 1 and 2 power stage power supply
15	VCCS	Signal system power supply
16	VIN1+	Channel 1 input. Input operational amplifier + input.
17	VIN1-	Channel 1 input. Input operational amplifier - input.
18	VIN1	Channel 1 input. Input operational amplifier output.
19	VIN2+	Channel 2 input. Input operational amplifier + input.
20	VIN2-	Channel 2 input. Input operational amplifier - input.
21	VIN2	Channel 2 input. Input operational amplifier output.
22	VIN3-	Channel 3 input. Input operational amplifier - input.
23	VIN3	Channel 3 input. Input operational amplifier output.
24	VO_OP	Operational amplifier output
25	VIN-OP	Operational amplifier - input
26	VIN+OP	Operational amplifier + input
27	REG_IN	Regulator error amplifier output. Connect this pin to the base of the external pnp transistor.
28	RFG_OUT	Regulator error amplifier input (+).
29	VREF_OUT	VREF amplifier (voltage follower) output.
30	VREF_IN	VREF input. Apply the external reference voltage to this pin.
31	VIN4	Channel 4 input. Input operational amplifier output.
32	VIN4-	Channel 4 input. Input operational amplifier - input.
33	MUTE234	Controls the on/off state of channels 2, 3, and 4.
34	MUTE1	Channel 1 output on/off control
35	VCONT	Loading block output high-level voltage setting
36	S_GND	Signal system ground

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-3

Q201 : CXD3014R (CD Digital Signal Processor with Built-in RF Amplifier and Digital Servo + Digital High & Bass Boost + CODEC) -1/4

BLOCK DIAGRAM



IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-4

Q201 : CXD3014R (CD Digital Signal Processor with Built-in RF Amplifier and Digital Servo + Digital High & Bass Boost + CODEC) -2/4

TERMINAL DESCRIPTION

Pin No.	Pin name	I/O	Description
1	LRCK	O	LR clock output.
2	LRCKI	I	LR clock input.
3	PCMD	O	PCMD data output.
4	PCMDI	I	PCMD data input.
5	BCK	O	BCK data output.
6	BCKI	I	BCK data input.
7	XTACN	I	Oscillation circuit control. Self-oscillation when high, oscillation stop when low.
8	XRST	I	System reset. Reset when low.
9	DVSS3	---	Internal digital GND.
10	IREQ	O	ARC ⟶ Interrupt to microprocessor.
11	CLOK	I	CPU I/F ARC(CLK)
12	DATA2	I/O	CPU I/F ARC(DATA)
13	XLAT2	I	Codec latch signal.
14	REQ	I	CPU I/F ARC (REQ).
15	ACK	O	CPU I/F ARC (ACK).
16	XLAT	I	CDDSP control latch signal.
17	DVDD3	---	Internal digital power supply.
18	DVSS8	---	Internal digital GND.
19	DVDD8	---	Internal digital power supply.
20	SENS	O	SENS output to CPU.
21	WFCK	O	WFCK output.
22	XUGF	O	XUGF output. Output MNT0, RFCK, SOUT by command switch.
23	XPCK	O	XPCK output. Output MNT1, SOCK by command switch.
24	GFS	O	GFS output. Output MNT2, XROF, XOLT by command switch.
25	C2PO	O	C2PO output. Output MNT3, GTOP by command switch.
26	SCOR	O	High output when the subcode sync, S0 or S1, is detected.
27	DVDD4	---	Digital power supply.
28	COUT	I/O	Track number count signal input/output.
29	DVSS9	---	Internal digital GND.
30	DVDD9	---	Internal digital power supply.
31	MIRR	I/O	Mirror signal input/output.
32	DFCT	I/O	Defect signal input/output.
33	FOK	I/O	Focus OK signal input/output.
34	DVSS4	---	Internal digital GND.
35	DVDD5	---	Internal digital power supply.
36	DVSS5	---	Internal digital GND.
37	LOCK	I/O	GFS is sampled at 460Hz; when GFS is high, this pin outputs a high signal. If GFS is low eight consecutive samples, this pin outputs low. Or input when LKIN = "1".
38	MDP	O	Spindle motor servo control output.
39	SSTP	I	Disc innermost detection signal input.
40	IOVSS1	---	I/O digital GND.
41	SFDR	O	Sled drive output.
42	SRDR	O	Sled drive output.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-5

Q201 : CXD3014R (CD Digital Signal Processor with Built-in RF Amplifier and Digital Servo + Digital High & Bass Boost + CODEC) -3/4

TERMINAL DESCRIPTION (Continued)

Pin No.	Pin name	I/O	Description
43	TFDR	O	Tracking drive output.
44	TRDR	O	Tracking drive output.
45	FFDR	O	Focus drive output.
46	FRDR	O	Focus drive output.
47	IOVDD1	---	I/O digital power supply.
48	AVD1	---	Analog power supply.
49	AVS1	---	Analog GND.
50	E	I	E signal input.
51	F	I	F signal input.
52	TEI	I	Tracking error signal input to DSSP block or F input.
53	TEO	O	Tracking error signal output from RF amplifier block.
54	FEI	I	Focus error signal input to DSSP block or A input.
55	FEO	O	Focus error signal output form RF amplifier block.
56	VC	I/O	Center voltage output from RF amplifier block. Center voltage input to DSSP block by command switch.
57	A	I	A signal input.
58	B	I	B signal input.
59	C	I	C signal input.
60	D	I	D signal input.
61	AVD2	---	Analog power supply.
62	RFDCO	I/O	RFDC signal output. RFDC signal input to DSSP block by command switch.
63	PDSENS	I	Reference voltage pin for PD.
64	AC_SUM	O	RFAC summing amplifier output.
65	EQ_IN	I	Equalizer circuit input.
66	LD	O	APC amplifier output.
67	PD	I	APC amplifier input.
68	RFC	I	Equalizer cut-off frequency adjustment pin.
69	AVS2	---	Analog GND.
70	RFACO	O	RFAC signal output.
71	RFACI	I	RFAC signal input or EFM signal input.
72	AVD3	---	Analog power supply.
73	BIAS	I	Asymmetry circuit constant current input.
74	ASYI	I	Asymmetry comparator voltage input.
75	ASYO	O	EFM full-swing output. (Low = VSS, High = VDD)
76	VPCO	O	Wide-band EFM PLL charge pump output.
77	VCTL	I	Wide-band EFM PLL VCO2 control voltage input.
78	AVS3	---	Analog GND.
79	CLTV	I	Multiplier VCO1 control voltage input.
80	FILO	O	Master PLL (slave = digital PLL) filter output.
81	FILI	I	Master PLL filter input.
82	PCO	O	Master PLL charge pump output.
83	DVSS6	---	Internal digital GND.
84	DVDD6	---	Internal digital power supply.
85	SRAMSTB	I	Normally low.
86	DVDD1	---	Internal digital power supply.
87	DVSS1	---	Internal digital GND.

IC BLOCK DIAGRAMS AND TERMINAL DESCRIPTIONS-6

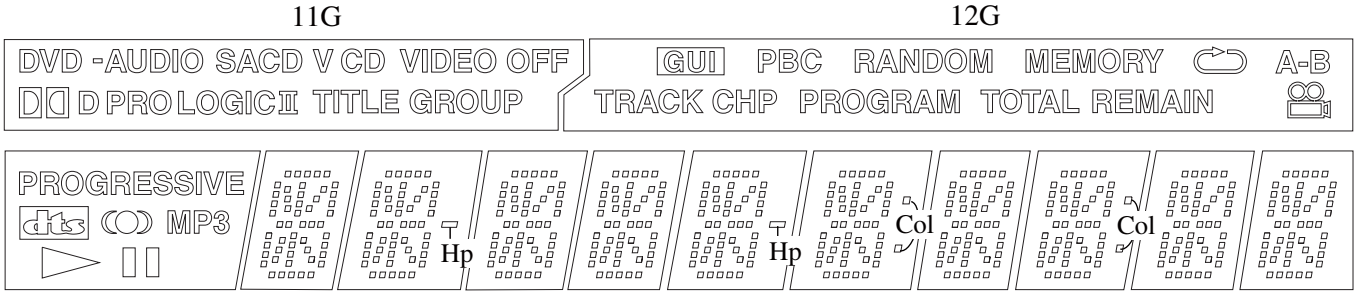
Q201 : CXD3014R (CD Digital Signal Processor with Built-in RF Amplifier and Digital Servo + Digital High & Bass Boost + CODEC) -4/4

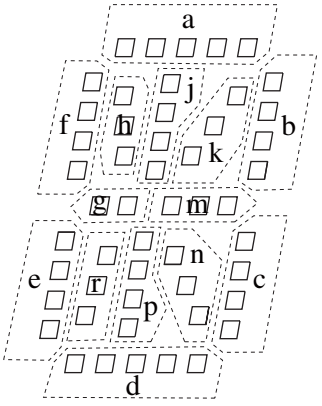
TERMINAL DESCRIPTION (Continued)

Pin No.	Pin name	I/O	Description
88	TEST1	I	Test mode set.
89	DATA	I/O	CPU I/F ARC (DATA).
90	CLOK2	I	CPU I/F ARC (CLK).
91	DVSS7	---	Internal digital GND.
92	DVDD7	---	Internal digital power supply.
93	TEST2	I	Test pin. Normally GND.
94	TEST3	I	Test pin. Normally GND.
95	TEST4	O	Open.
96	TEST5	I	Test pin. Normally GND.
97	TEST6	I	Test pin. Normally GND.
98	DVSS2	---	Internal digital GND.
99	DVDD2	---	Internal digital power supply.
100	IOVDD2	---	I/O digital power supply.
101	DOUT	O	Digital Out output.
102	TEST	I	Test pin. Normally GND.
103	TES1	I	Test pin. Normally GND.
104	IOVSS2	---	I/O digital GND.
105	PLLAVD	---	PLL cell power supply.
106	PLLAVS	---	PLL cell GND.
107	XVSS	---	Master clock GND.
108	XTAO	O	Crystal oscillation circuit output.
109	XTAI	I	Crystal oscillation circuit input.
110	XVDD	---	Master clock power supply.
111	AVD4	---	Analog power supply.
112	AOUT1	O	Lch analog output.
113	VREFL	O	Lch reference voltage.
114	AVS4	---	Analog GND.
115	AVS5	---	Analog GND.
116	VREFR	O	Rch reference voltage.
117	AOUT2	O	Rch analog output.
118	AVD5	---	Analog power supply.
119	IOVDD3	---	I/O digital power supply.
120	IOVSS3	---	I/O digital GND.

FL TUBE VIEW

Q802 : HNV-13SS12T





(1G-10G)

	1G	2G	3G	4G	5G	6G	7G	8G	9G	10G	11G	12G	13G
P1	a	a	a	a	a	a	a	a	a	a	GROUP	REMAIN	–
P2	h	h	h	h	h	h	h	h	h	h	TITLE	TOTAL	–
P3	l	j	j	j	j	j	j	j	j	j	PRO LOGIC		–
P4	k	k	k	k	k	k	k	k	k	k	D	TRACK	–
P5	b	b	b	b	b	b	b	b	b	b		CHP	–
P6	f	f	f	f	f	f	f	f	f	f	CD	GUI	–
P7	m	m	m	m	m	m	m	m	m	m	V	-B	–
P8	g	g	g	g	g	g	g	g	g	g	SACD	A	–
P9	c	c	c	c	c	c	c	c	c	c	-AUDIO	PROGRAM	–
P10	e	e	e	e	e	e	e	e	e	e	DVD		
P11	r	r	e	r	r	r	r	r	r	r	II	MEMORY	
P12	p	p	p	p	p	p	p	p	p	p	VIDEO OFF	RANDOM	PROGRESSIVE
P13	n	n	n	n	n	n	n	n	n	n	–	PBC	MP3
P14	d	d	d	d	d	d	d	d	d	d	–	–	
P15	–	–	col	–	col	Hp	–	–	Hp	–	–	–	

SERVICE PROCEDURE-1

PROTECTION OF EYES FROM LASER BEAM DURING SERVICING

This set employs a laser. Therefore, be sure to follow carefully the instructions below when servicing.

WARNING!!

SERVICE WARNING : DO NOT APPROACH THE LASER EXIT WITH THE EYE TOO CLOSELY. IN CASE IT IS NECESSARY TO CONFIRM LASER BEAM EMISSION, BE SURE TO OBSERVE FROM A DISTANCE OF MORE THAN 30cm FROM THE SURFACE OF THE OBJECTIVE LENS ON THE OPTICAL PICKUP BLOCK.

Laser Diode Properties

Material: GaAS/GaAlAs
Wavelength: 760-800nm
Laser output: max. 0.5mW*
Emission Duration: continuous
*This output is the value measured at a distance about 1.8mm from the objective lens surface on the Optical Pickup Block.

LASER WARNING LABEL

The labels shown below are affixed.

1. Warning label

2. Class 1 label

LUOKAN 1
LASERLAITE

KLASS 1
LASER APPARAT

Printed on rear panel

PRECAUTIONS

1. Ground for the work-desk.
   Place a conductive sheet such as a sheet of copper (with impedance lower than 10 Mohm) on the work-desk and place the set on the conductive sheet so that the chassis can be grounded.
2. Grounding for the test equipments and tools.
   Test equipments and toolings should be grounded in order that their ground level is the same the ground of the power source.
3. Grounding for the human body.
   Be sure to put on a wrist-strap for grounding whose other end is grounded.
   Be particularly careful when the workers wear synthetic fiber clothes, or air is dry.
4. Select a soldering iron that permits no leakage and have the tip of the iron well-grounded.
5. Do not check the laser diode terminals with the probe of a circuit tester or oscilloscope.

SERVICE PROCEDURE-2

1. Initialize the unit.

(1) Press and hold down the UP [►►I] button, then press the REPEAT button.

FL display: *CLEAR* ---> *READING* ---> *NO DISC*

(2) Press the POWER button to turn off the unit.

(3) Disconnect the AC power cord from a wall outlet.

2. Check the version of Main microprocessor (Q701) and Sub microprocessor (Q801).

(1) Connect the AC power cord into a wall outlet.

(2) Press the POWER button to turn on the unit.

(3) Change into the state of *"NO DISC"*.

(4) Press and hold down the DISPLAY button, then press the PAUSE [❚❚] button and press the STOP [■] button.

FL display: *SYS 1.00*

(5) Press the DISPLAY button.

FL display: *DK06Z21A* <--- Main microprocessor version

(6) Press the DISPLAY button.

FL display: *SUB03506A* <--- Sub microprocessor version

(7) Press the DISPLAY button.

FL display: *CK_SUM:6241*

(8) Press the POWER button to turn off the unit.

(9) Disconnect the AC power cord from a wall outlet.

3. Setting position before shipment.

(1) POWER button : OFF

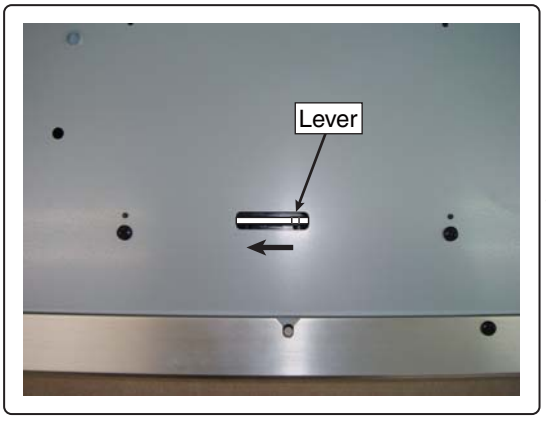
(2) PHONES LEVEL : MIN.

4. Take out the Disc.

If cannot take out the disc, please take out disc as follows.

(1) The lever in the direction of the arrow.

(2) The tray is slowly drawn out by the hand.



--- Bottom view ---

Front panel

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