ORDER NO. DPD831030–1

Technical Guide

VOL. 1

CIRCUIT DESCRIPTIONS

Compact Disc Player

SL-P10

Technics

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
DISCPLAYER DIVISION, SERVICE GROUP.

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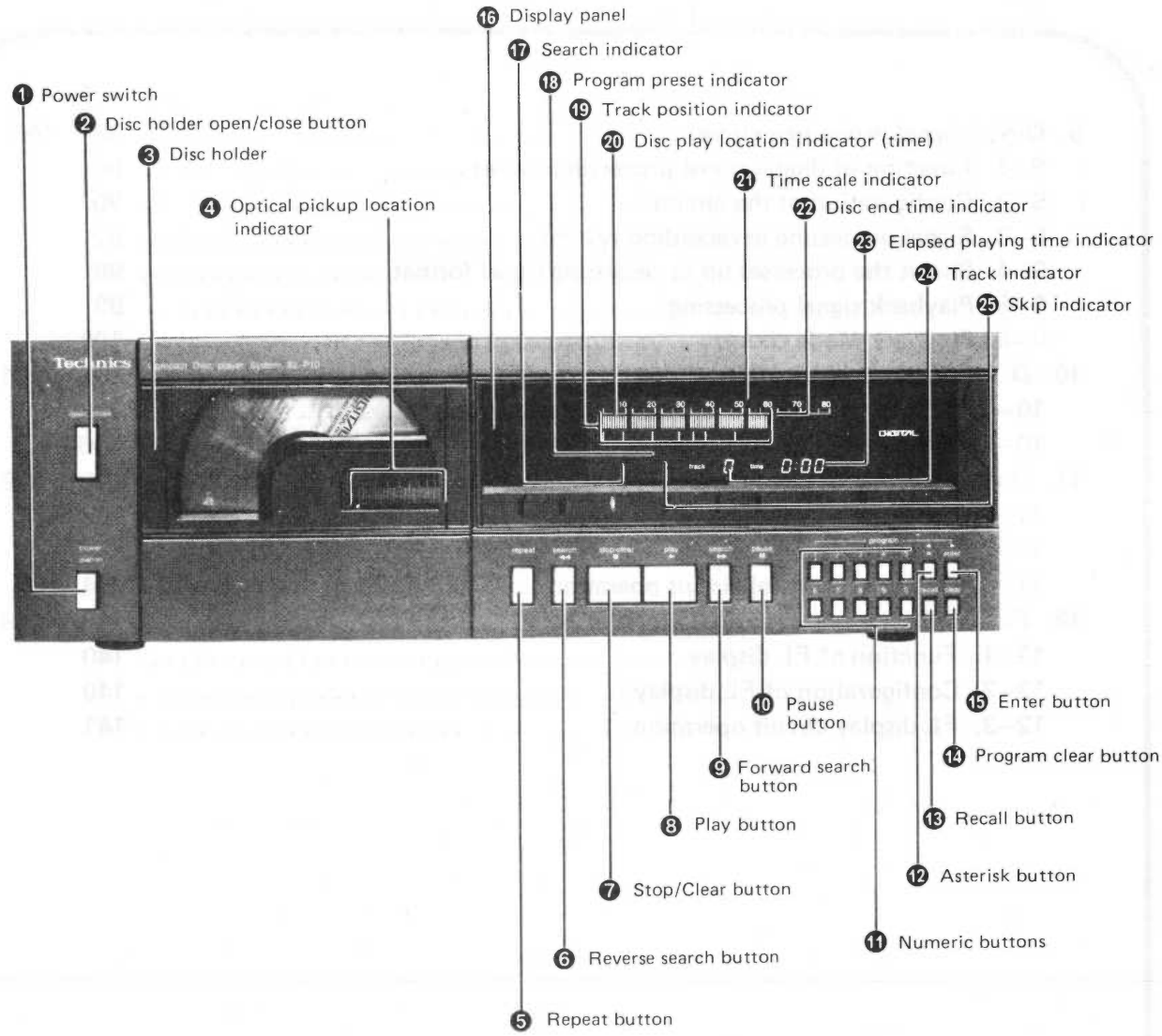
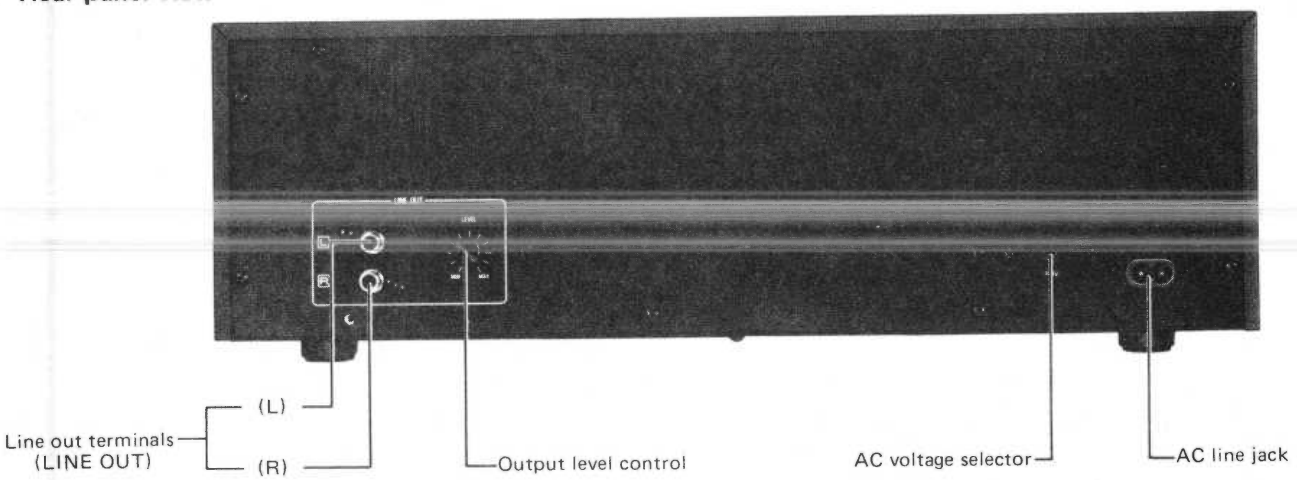
1. Location of controls

- **Front panel view**



- **Rear panel view**



Functions

- **Optical pickup operation buttons and indicators**

❶ Power switch (Power push on)

- Press once to turn power on and again to turn power off.
- When power is turned on, the following indicators light up:
  - ❹ Pickup location indicator
  - ㉑ Time scale indicator
  - ㉓ Elapsed playing time indicator
  - ㉔ Track indicator
  - Ⓐ Stop/Clear indicator

❷ Disc holder open/close button (open/close)

- Press this button to insert or remove a disc. When this button is pressed, the disc holder ❸ opens.
- Press this button again to close the holder.

❸ Disc holder

- The disc will be loaded automatically once it has been inserted about half way by hand.

❹ Optical pickup location indicator

- This indicator shows the approximate location of the optical pickup at all times.

❺ Repeat button (repeat)

- Press this button to activate the repeat play mode.
- The repeat indicator Ⓔ lights up to show when the repeat mode is activated, Press this button again to cancel the repeat mode. The program function can be used with repeat to play any section of a disc repeatedly.

❻ Reverse search button (◄◄ search)

- Press to move the pickup inward (toward the beginning of the disc).
- The reverse search indicator Ⓒ lights up to show when this button is being used.
- This button has two steps: press gently to move the pickup slowly and firmly to move the pickup rapidly.
- If this button is pressed when the stop/clear indicator Ⓐ is illuminated, the pickup will return to the stating position (the beginning of the first track). If the play button ❽ is pressed during reverse search operation, disc play will resume at that point.
- When the reverse search button ❻ is pressed during disc play, the pickup will move only as long as the button is held down, Disc play will resume at the point where the reverse search button ❻ is released.

❼ Stop/Clear button (■ Stop·Clear)

- Press this button to stop disc play. If this button is pressed during program disc play, the program will be cleared from the memory.
- The stop/clear indicator Ⓐ lights up to show when this button has been pressed.

❽ Play button (play ►)

- Press this button to begin disc play. The play indicator Ⓓ lights up to show when this button has been pressed.
- When this button is pressed during disc play, the pickup returns to the starting position and disc play starts again from the beginning. (During program disc play, the pickup returns to the beginning of the program.)

❾ Forward search button (search ►►)

- Press to move the pickup outward (toward the end of the disc).
- The forward search indicator Ⓔ lights up to show when this button is being used.
- This button has two steps: press gently to move the pickup slowly forward and firmly to move the pickup rapidly forward.
- If this button is pressed when the stop/clear indicator Ⓐ is illuminated, the pickup will advance to the outer edge of the disc (the end of the last track). If the play button ❽ is pressed during forward search operation, disc play will resume at that point.
- When the forward search button is pressed during disc play, the pickup will move only as long as the button is held down. Disc play will resume at the point where the forward search button ❾ is released.

❿ Pause button (❚❚ pause)

- Press this button to temporarily stop disc play. The pause indicator Ⓕ lights up to show when this button has been pressed. To resume disc play, press this button again.

- **Programming buttons**

⓫ Numeric buttons

- Use these buttons to enter the number of each track to be played and the order in which they are to be played.
- These buttons can also be used to enter the starting and finishing points of disc play.
  (Disc play can also be started and/or ended in the middle of any track by programming play from X minutes and Y secondes of track Z to A minutes and B secondes of track C.)

⓬ Asterisk button (✱)

- When programming disc play by minutes and seconds, press this button after entering the track number and again after entering the number of minutes.
- Each time this button is pressed during normal disc play, the pickup moves to the beginning of the previous track to permit reverse skip play. Note that the first time this button is pressed, the pickup will return to the beginning of the track being played at that time.
  Example: If this button is pressed while the third track is being played, the pickup will return to the beginning of the third track. If the button is pressed again, the pickup will return to the beginning of the second track and normal disc play will start at that point.
- When this button is pressed during program disc play, disc play is returned to the previous program step.

⓭ Recall button (recall)

- Press this button to recall the program.
- The current program is shown by the track indicator ㉔ and elapsed playing time indicator ㉓.

⓮ Program clear button (clear)

- Press this button to clear the program from the memory.
- When this button is pressed during program disc play, the program will be cleared but disc play will continue.

⓯ Enter button (►enter)

- Press this button to enter the program in the memory.
- Each time this button is pressed during normal disc play, the pickup moves to the beginning of the next track to permit forward skip play.
  Example: If this button is pressed while the third track is being played, the pickup will advance to the beginning of the fourth track. If the button is pressed again, the pickup will advance to the beginning of the fifth track and normal disc play will start at that point.
- When this button is pressed during program disc play, disc play is advanced to the next program step.

- **Display panel indicators**

⑯ Display panel
- The display panel consists of a large 14 x 5 cm fluorescent type display. Read the following explanations carefully to obtain all the benefits of this multi-function display.

⑰ Search indicator (search)
- Lights up while the information on the disc (number of tracks, total playing time, etc.) is being read.
- Also lights up while the pickup is moving to a new disc play location in either skip play mode or the program play mode.

⑱ Program preset indicator (selection)
- Shows in minutes the starting points of each program. (Lights up only when a program exists.)

⑲ Track position indicator (location)
- Shows in minutes the locations of each blank section between tracks on the disc.

⑳ Disc play location indicator (time)
- Shows in minutes the location of the pickup during disc play.
- Use this indicator to follow pickup movement when using either of the rapid search modes (by pressing the forward ⑨ or reverse search button ⑥ firmly).

㉑ Time scale indicator
- The scale goes from 0 to 80 minutes in 5 and 10 minute intervals.

㉒ Disc end time indicator
- Shows the total playing time of the disc.

㉓ Elapsed playing time indicator (time 0:00)
- Shows the position of the pickup in minutes and seconds as disc play progresses.
- When the recall button ⑬ is pressed, the programmed starting and finishing times (min., sec.) are shown in that order.

㉔ Track indicator (track 0)
- Shows the track number currently being played.
- When the recall button ⑬ is pressed, the numbers of the programmed tracks are shown in the order of play.
- If there is a mistake in the program (a program that can not be executed), an E will be displayed.
- An F is displayed to show when the limit of 63 steps has been programmmed.

㉕ Skip indicator (skip)
- Lights up when the asterisk button ⑰ or enter button ⑮ is pressed to perform skip play.

1–1. Specifications

Specifications are subject to change without notice for further improvement.
Weight and dimensions shown are approximate.

■ Audio

No. of channels:	2 (left and right stereo)
Frequency response:	4 ~ 20,000 Hz ± 0.5 dB
Dynamic range:	more than 90 dB
S/N ratio:	more than 90 dB
Total harm. dist.:	less than 0.004% (1 kHz, 0 dB)
Channel separation:	more than 90 dB
Wow and flutter:	quartz accuracy

■ Signal Format

Sampling frequency:	44.1 kHz
Correction system:	Technics Super Decording Algorithm

■ Pickup

Type:	Astigma 3-beam
Objective lens suspension:	Twin parallel suspension
Light source:	Semiconductor laser
Wavelength:	800 nm

■ Functions

Search modes:	Automatic search Manual search Program search Skip search
Program functions:	Max. of 63 steps (location of beginning of tracks, selection of starting and ending positions)
Display functions:	14 x 5 cm fluorescent display with centralized control. Time scale, track position, pickup location, playing time, program location, track, elapsed time and program contents indication.
Operation buttons:	Basic buttons: 7 Program buttons: 14
Disc loading:	Front type, automatic loading

Reference

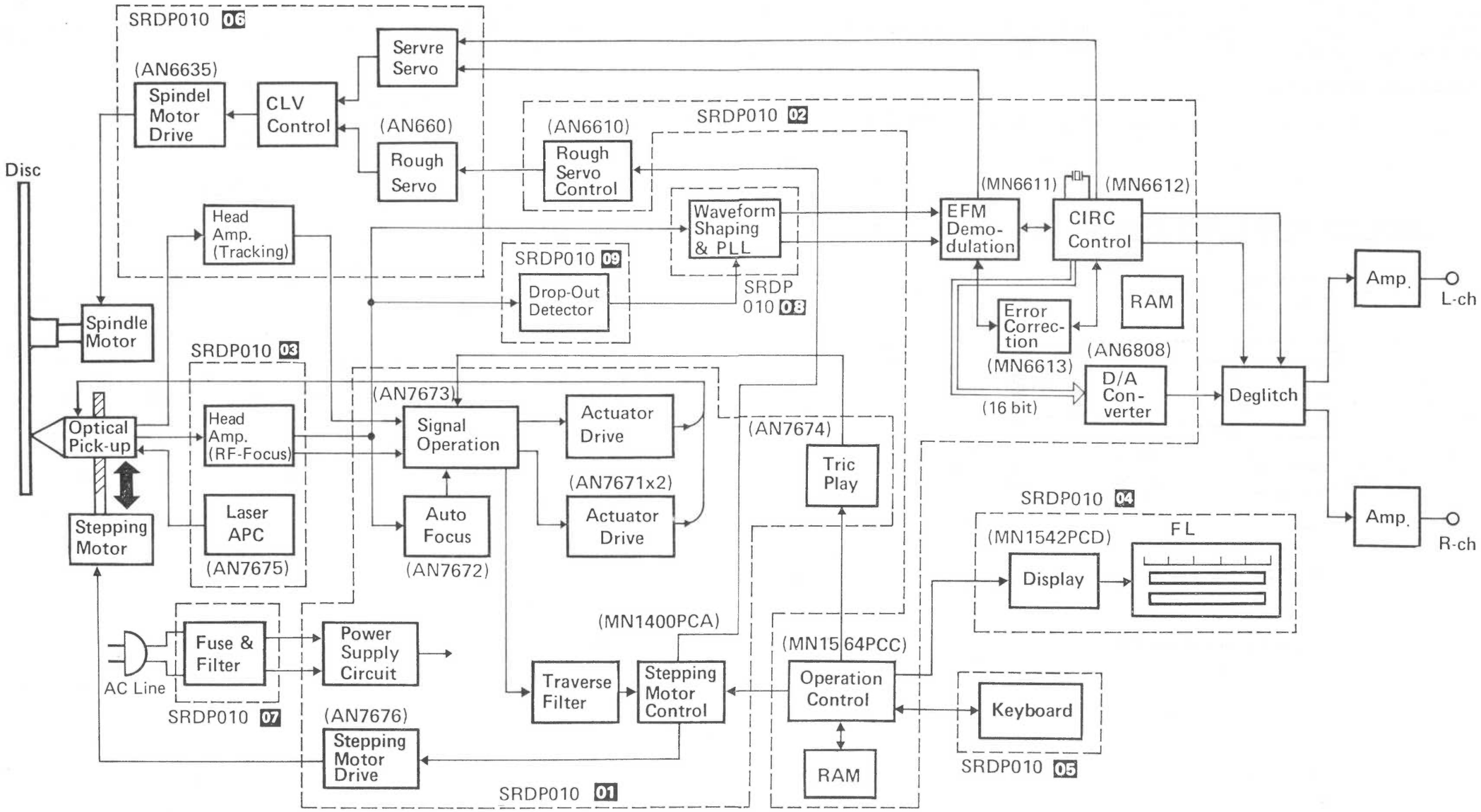
■ Compact Disc specifications

Diameter:	12 cm
Thickness:	0.12 cm
Spindle hole:	1.5 cm
Min. inside diameter of recorded section:	5 cm
Max. outside diameter of recorded section:	11.6 cm (disc is played from the inside to the outside edge)
Direction of rotation:	Counterclockwise (seen from recorded side of disc)
Tracking speed:	1.2 to 1.4 meters/second, CLV (Constant Linear Velocity)
Rotations	About 500 to 200 rpm
Playing time:	About 60 minutes (up to 75 min. can be contained)
Track pitch:	1.6 μm
Material:	Clear plastic

■ General

Power supply:	~110/120/220/240V, 50 or 60 Hz
Power consumption:	60 W
Output voltage:	Max. 1.5 volts (adjustable)
Output impedance:	220 ohms
Load impedance:	more than 5 kohms
Dimensions (WxDxH):	43 x 31.5 x 14.5 cm
Weight:	10 kg.

1–2. Block diagram of SL-P10



(1) Focaus Servo (2) Tracking Servo (3) CLV Servo (4) Traverse Servo

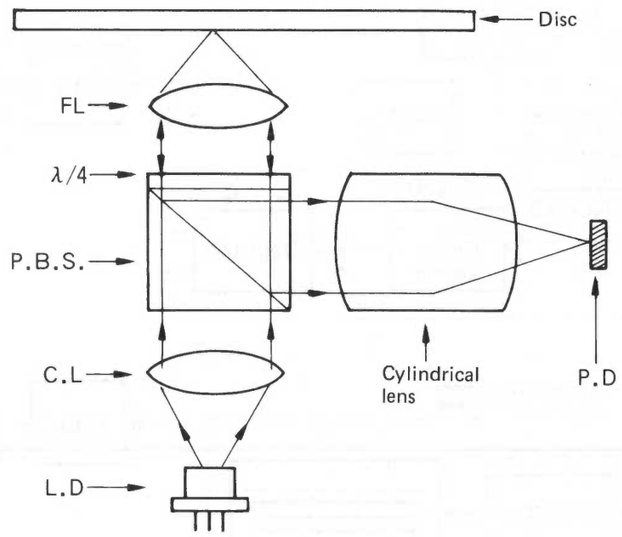
2. Optical pick-up and traverse unit

2–1. Function of optical pickup

Optical pickup (hereinafter called "optical PU") corresponds to the cartridge of conventional analog player. It employs a non-contact optical system and has two functions.
One is to pick up the signal (RF signal in CD) recorded on a disk the same as in cartridge.
Another is an important function to detect focus error and tracking error, thereby providing servo function.

2–2. Configuration of optical PU

The basic configuration of optical PU is shown in Fig. 2-1.



2–1. Confignration of optical PU.

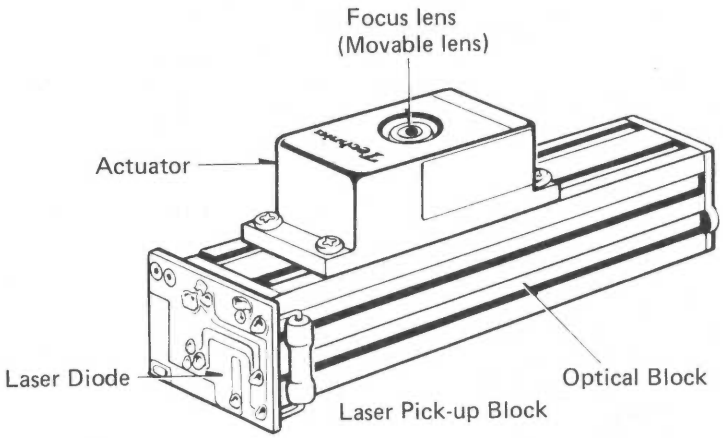
The beams of light emitted from the laser diode (hereinafter called "LD") become parallel in the collimator lens (hereinafter called "CL" and is focused on the disk by the focus lens (hereinafter called "FL") after passing through the polarized beam splitter (hereinafter called "P.B.S.") and λ/4 plate.
The light reflected from the disk follows the light in the reverse direction and is reflected from P.B.S. and is received by the photo detector (hereinafter called "PD") after passing through the detection lens unit. These can be roughly divided into 2 sections.

One is the section in which the light comes out of LD and is focused on the disk, that is called "light source section". The main optical elements at the light source are LD, CL and FL. P.B.S. and λ/4 have nothing to do with focusing.

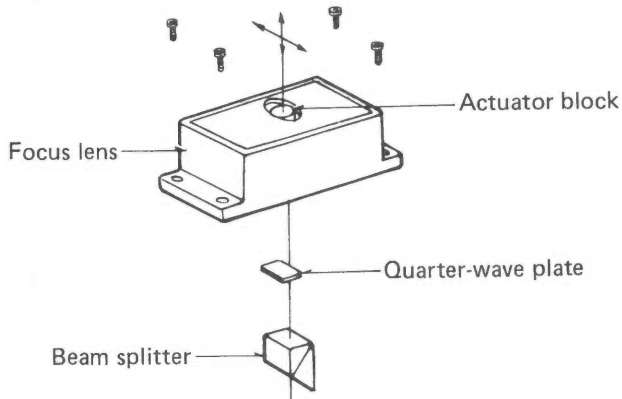
Another is the section in which the light is reflected from the disk and is received by PD, that is called "detector section".
The detector section of furnished with a lens unit and PD which serve to detect focus error and tracking error.
Another P.B.S. and λ/4 are not directly related with focusing and detection, these are inevitable for separation of "going" and "returning" light paths.

The configuration of optical PU of SL-P10 is shown in Fig. 2-2.
Grating is necessary only when a 3-beam system is used for detection of tracking error. Also, a cylindrical lens is used for the detection lens unit because an astingmatic system is employed for focus error detection, and the main parts are the same as for the basic configuration.

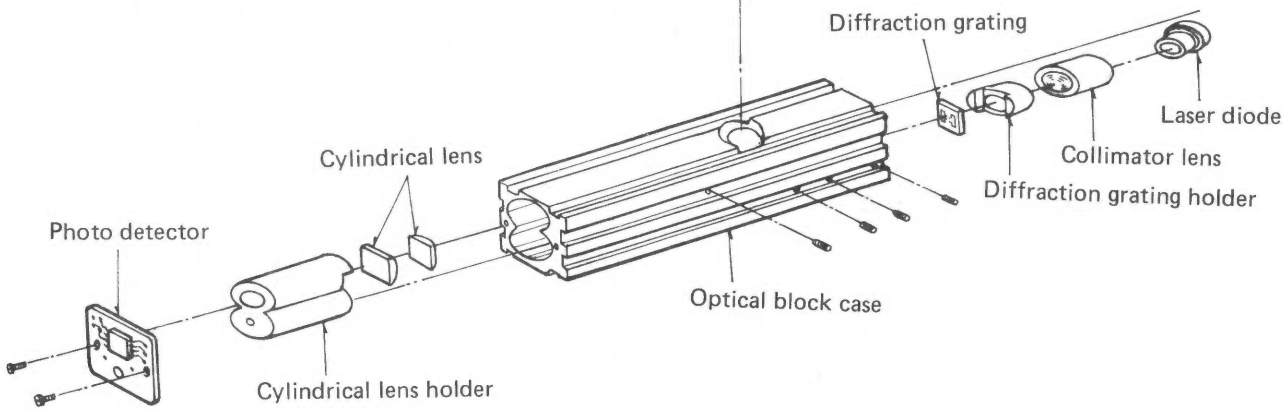
2–3. Optical pick-up and traverse unit



Travers Structure Diagram



Laser Pick-up Block



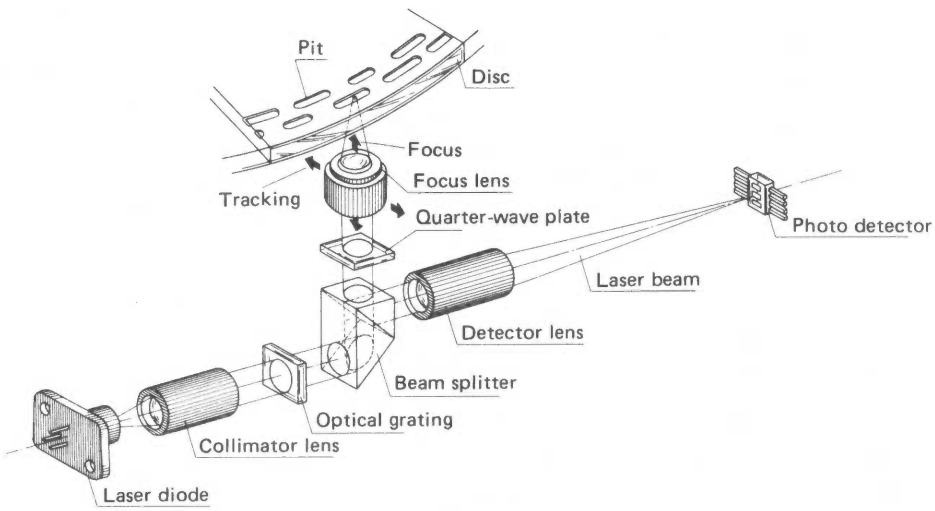


Fig. 2–2. Configuration of optical Servo

2–4. Optical PU of SL-P10

The traverse unit incorporates a spindle motor to drive the disk and a stepping motor to move the optical PU in the direction of radius and an optical PU in aluminum diecast. (See Fig. 2-3.)

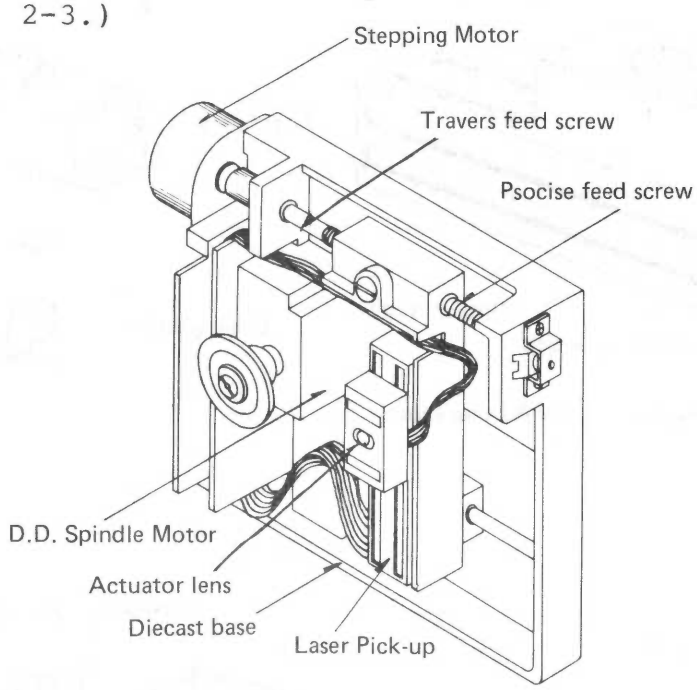


Fig. 2–3. Travers Servo Structure Diagram

2–5. Traverse unit of SL-P10

The uni-body construction improves the mutual position accuracy of component parts. Also, laser APC and RF signal head amplifier are built into the unit. An extra-mini 12-pole slotless DD motor is employed as a spindle motor.
A precision feed screw and stepping motor are used for the traverse mechanism to move the optical PU so that both high speed feed and position generating purposes required for random access can be achieved.

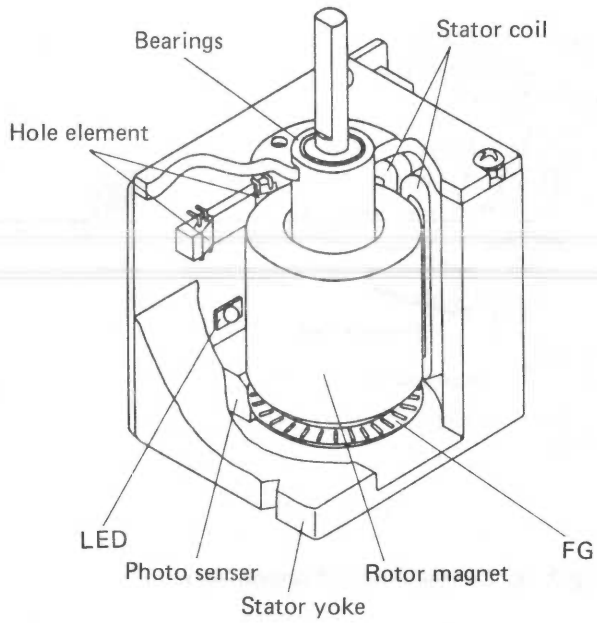
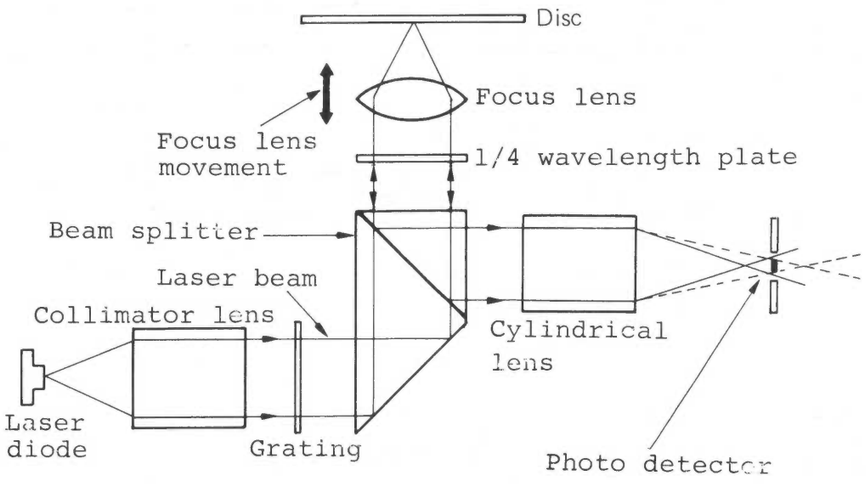


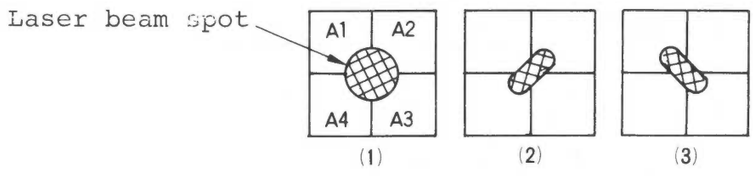
Fig. 2–4. Spindle Motor Diagram

3. Focus servo circuit

3—1. Function of focus servo

To correctly pick up the disk information, the focus lens is moved at right angles to the disk so that the laser beam is always focused on the pit of the disk. It is illustrated in Fig.3-1 and 3-2.



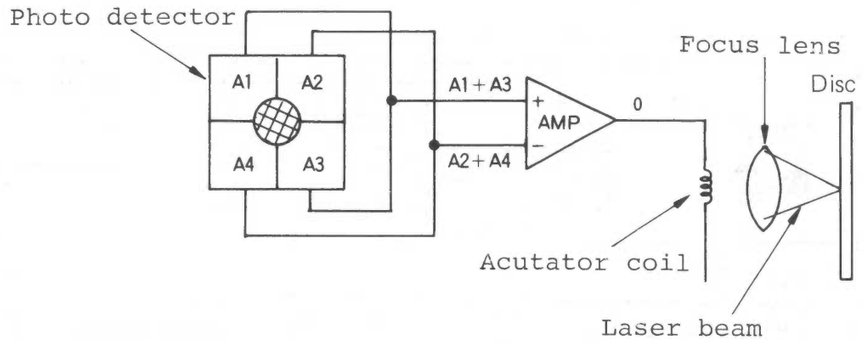


(1) Best focus
(2) Disc is too close
(3) Disc is too far

Fig. 3-1 Focus error detection by photo detector

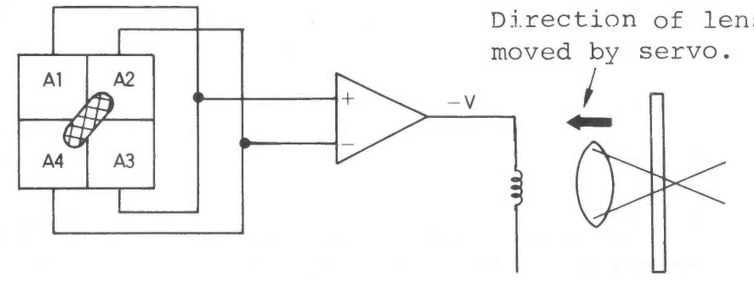
(1) Best focus

The beam received by photo detector is circular, and AMP output is (A1+A3) - (A2+A4) = 0.



(2) Disk is too close.

The beam received by photo detector is oval, and AMP output is (A1+A3) - (A2+A4) = negative voltage. The servo circuit controls the focus lens so that the negative voltage becomes zero.



(3) Disk is to far.

The beam received by photo detector is oval opposite in position to (2), and AMP output is (A1+A3) - (A2+A4) = positive voltage. The servo circuit controls the focus lens so that the positive voltage becomes zero.

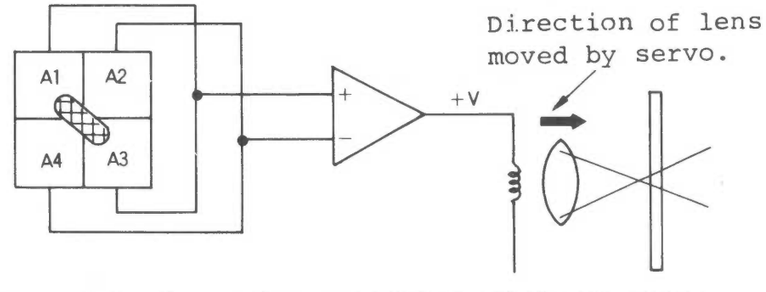
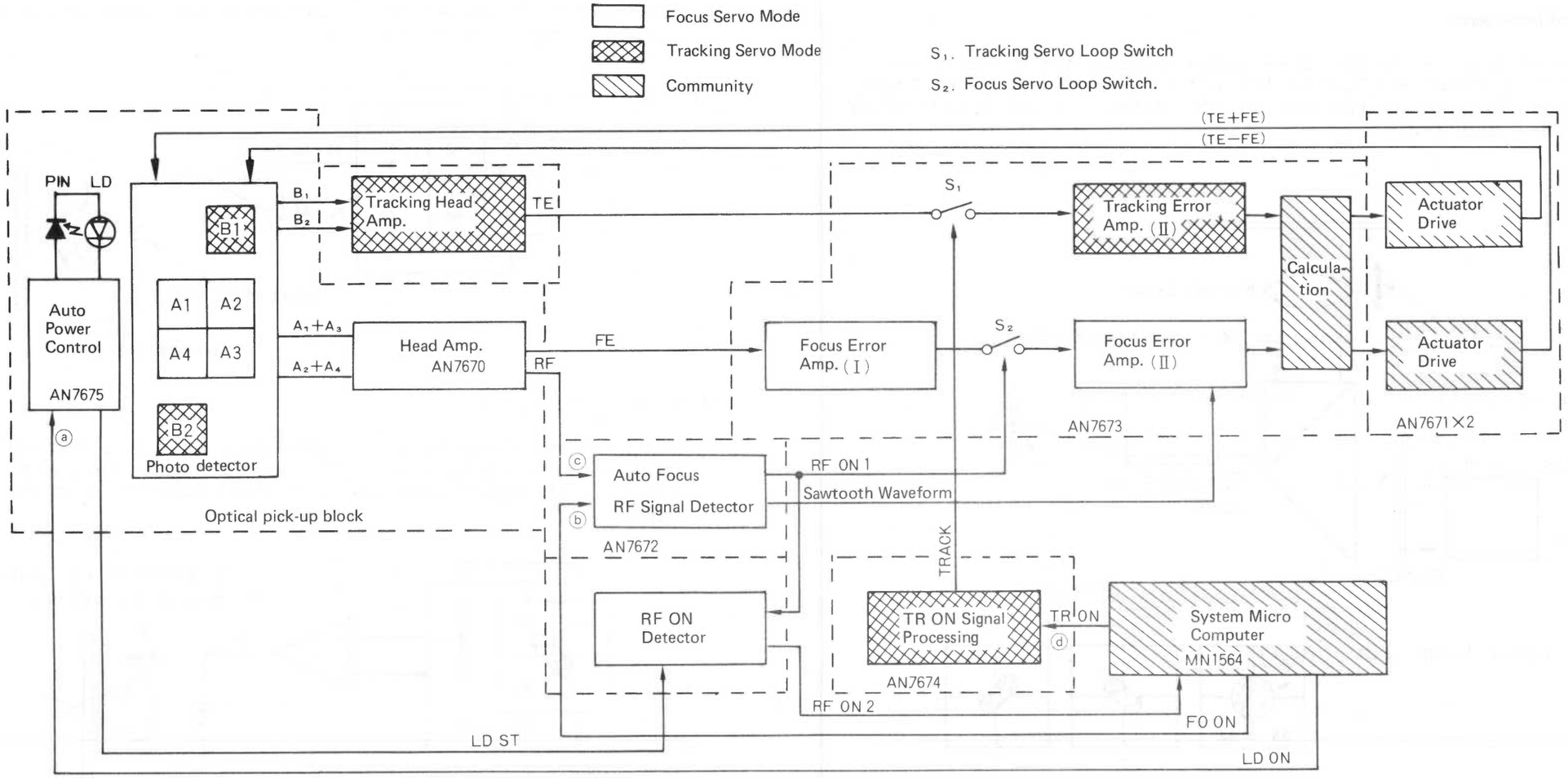


Fig. 3-2 Operation principle of focus servo

3–2. Block diagram of focus servo



TE : Tracking Error Signal (B_1-B_2)

FE : Focus Error Signal $(A_1+A_3)-(A_2+A_4)$

RF : Disc Pick-up Signal $(A_1+A_3)+(A_2+A_4)$

LD ON : Laser Diode ON Command.

FO ON : Focus Servo ON Command.

LD ST : Laser State

RF ON1 : Confirmation Signal of RF Out-Put

RF ON2 : Confirmation Signal of RF Out-Put

TR ON : Tracking Servo ON Command.

TRACK : Tracking Servo Loop Switch (S1) Control

図 · **Fig. 3–3. Block diagram of optical servo**

- Function of optical servo circuit

Unlike the playback of conventional analog disc, the player employs a system using a laser pick-up to take out the signal.

Focus servo, tracking servo and traverse servo circuits are necessary for optical servo, and each individual servo function is explained in the following.

- Focus servo

Focus servo moves the focus lens at right angles to the disc so that the laser beam is always focused to the pit of the disc.

Tracking servo moves the focus lens horizontally to the disc so that the laser beam always follows the track of the disc.

The purpose is to align the focus of laser beam to the disc pit in order to correctly pick up disc information by laser beam. Also, disc is deflected (in the direction of focus) and is permitted up to ±300 μm by the disc standard. Accordingly, if the deflection in the direction of focus is within ±300 μm, then the laser beam will be properly focused to the disc pit.

- Tracking servo

Tracking servo moves the focus lens horizontally to the disc so that the laser beam always the track of the disc.

The purpose is to let the laser beam follow the track from inner to outer periphery of disc in order to correctly read the information from disc without sound grooves like analog record. Also, disc is deviated (in the tracking direction) and is permitted up to ±70 μm by the disc standard. Accordingly, if the deflection in the tracking direction is within ±70 μm, then the laser beam will correctly follow the disc track.

- Traververse servo

The stepping motor is rotated step by step to move the optical pickup toward the inner or outer periphery of the disc. The track following distance is limited to the range in which the focus lens is movable since the tracking servo follows the disc track while moving the focus lens. The distance is 200 μm max. and this is not enough to let the laser beam follow all the track recorded on the disc with a radius of 60 μm. Accordingly, when the focus lens has followed the track by about 62.5 μm from the tracking servo, the stepping motor is rotated by 1 step to move the optical pickup in the focus lens by 62.5 μm. In this way, the range of movable focus lens is expanded so that the laser beam can follow all the track on the disc.

• Configuration of optical servo

The block diagram of optical servo is shown in Fig. 3–1.

The procedure of complete operation of optical servo: Focus servo ON (FO ON) → Auto focus → RF signal detection (RF ON) → Tracking servo ON (TR ON).

Firstly, FO ON signal from the system microcomputer enters the point (a), then the auto focus circuit delivers sawtooth wave output to directly drive the focus error amplifier (II). Thus, the lens is moved vertically and RF signal is delivered when the lens is focused. This operation is called auto focus and it is illustrated in Fig. 3–4.

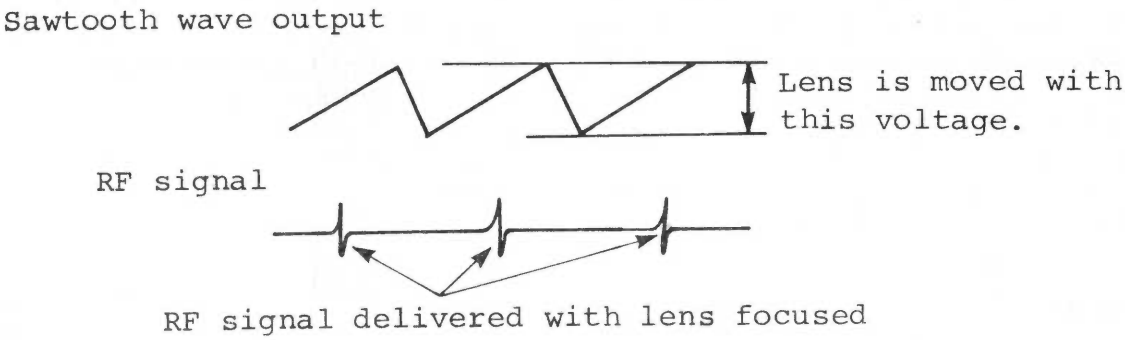


Fig: 3–4. Auto focus

When the RF signal enters the point (b), the auto focus operation is stopped and RF ON signal is generated to close S_2, activating the focus servo. The RF signal is shown in Fig. 3–5. RF ON signal also enters the system microcomputer.

The system microcomputer confirms the signal and then delivers TR ON output. S_1 is closed, activating the tracking servo. The RF signal is illustrated in Fig. 3–6.

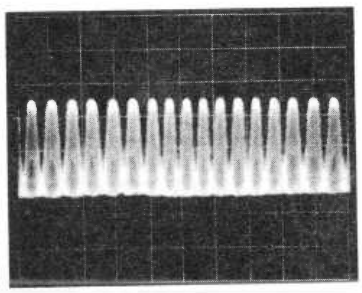


Fig. 3–5. RF signal with only focus servo ON

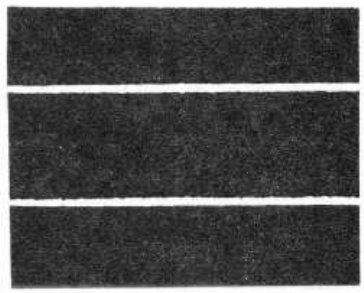


Fig. 3–6. RF signal with focus and tracking servo ON

As the tracking servo is activated and the lens starts to follow the track, the traverse servo operation is required.

The tracking servo functions with the input signal at point C that is delivered from the tracking error head amplifier.

The comparator and traverse microcomputer convert the signal change into pulses to operate the stepping motor.

3–3. Circuit operation of optical servo

1. Head amplifier and APC circuit

Before proceeding to the focus servo circuit operation of optical servo, the head amplifier and APC circuit of the optical pickup block are explained here.

The head amplifier is shown in Fig. 3–7, and the APC circuit, in Fig. 3–9.

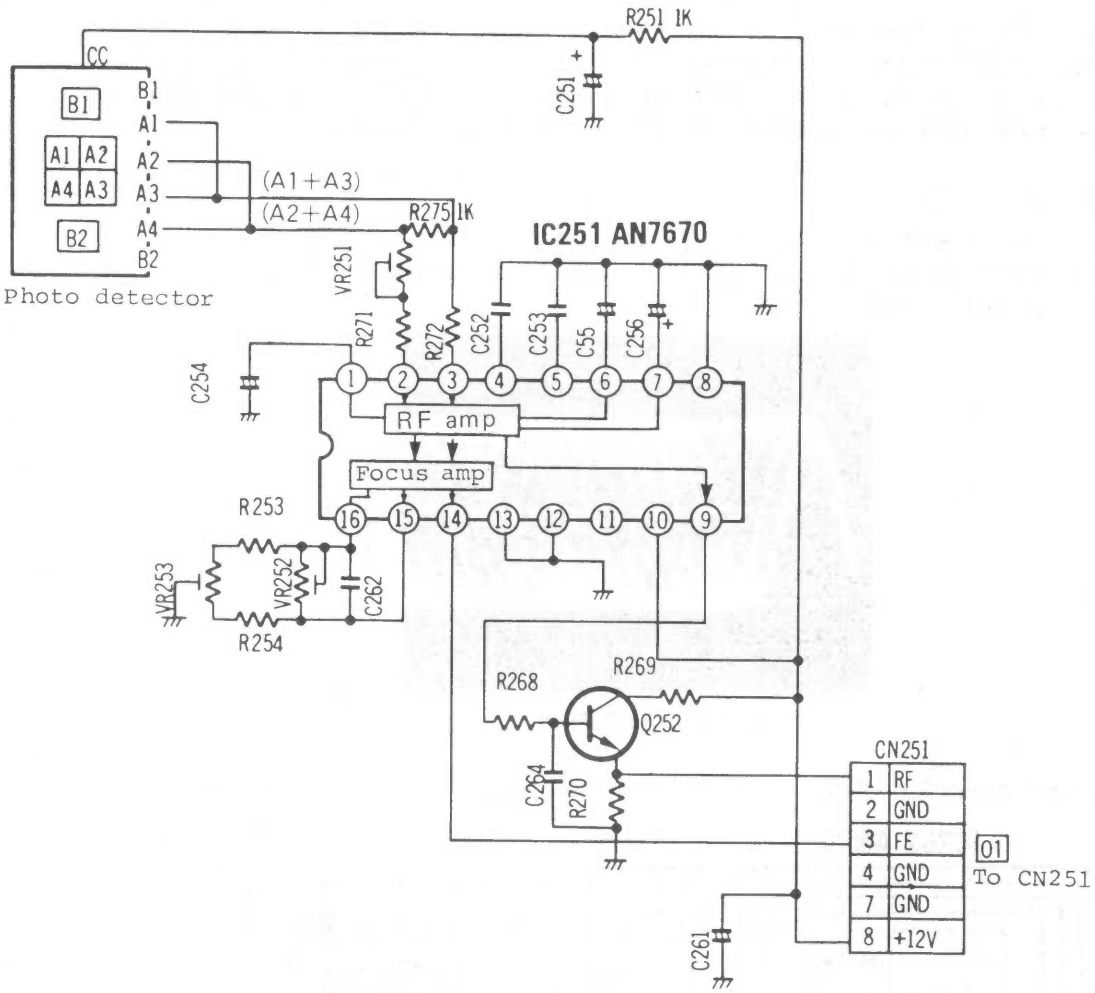


Fig. 3–7. Head amp. circuit

2. Focus error amp.

(1) Signal detected by photo detector $A_1 \sim A_4$ is connected to A_1, A_3 and A_2, A_4 to change it into $(A_1 + A_3)$ and $(A_2 + A_4)$ signals, and they are applied to IC251 pins (3) and (2).

(2) The signals applied to IC251 pins (3) and (2) are treated by the differential amplifier, and the difference between $(A_1 + A_3)$ and $(A_2 + A_4)$ is delivered as output. The error signal is focus error (FE) signal.

3. RF amp.

(1) The (A_1 + A_3) and (A_2 + A_4) signals applied to IC251 pins (3) and (2) are treated by RF amplifier in IC and are delivered as RF signal to IC251 pin (9).

(2) RF signal delivered to IC251 pin (9) is changed in impedance by transistor Q252, and is sent to 01 PCB through CN251 pin (1), and is distributed for data processing, drop-out detection and focus control.

° VR251 is a semi-fixed resistor to adjust the output level difference between (A_1 + A_3) and (A_2 + A_4) signals detected by focusing photo detector, and is adjusted so that the eye pattern* of RF signal is best.

*Eye pattern

In the observation of RF signal on the oscilloscope, the part A of Fig. 3–8 looks like eyes. So, the part is called "eye pattern".

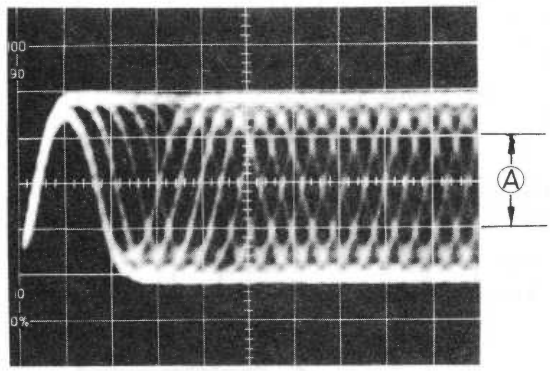


Fig. 3–8. RF signal

4. APC circuit operation (APC . . . . Auto Power Control)

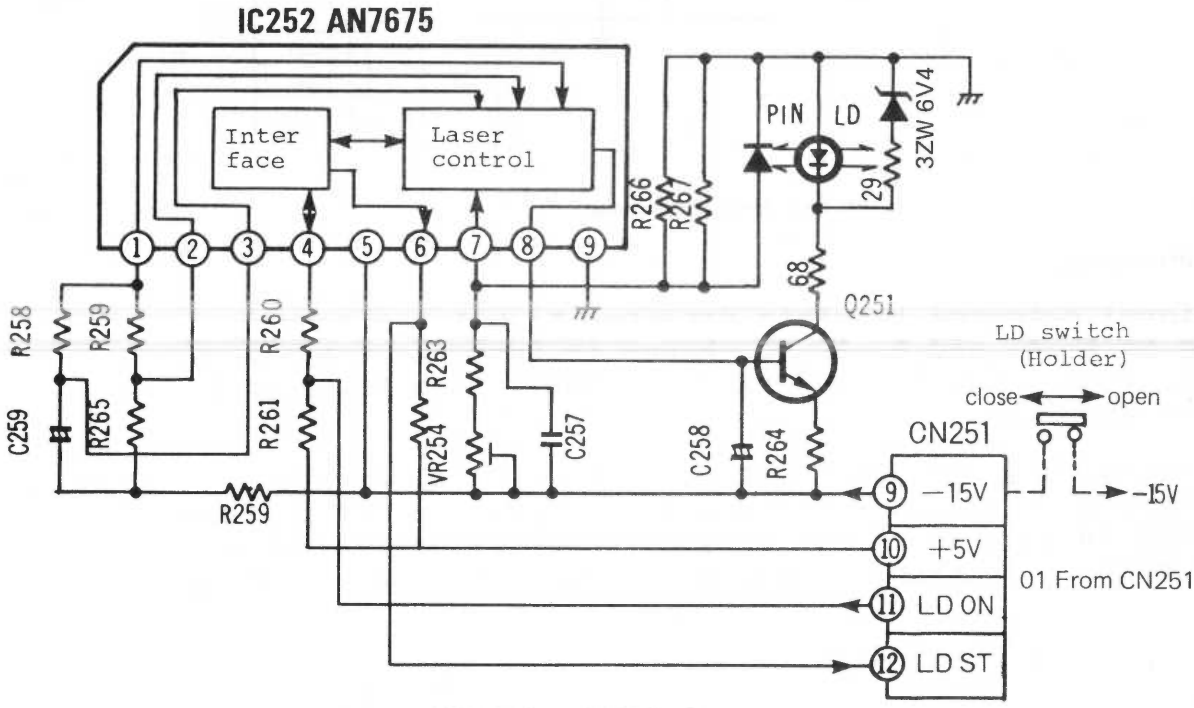


Fig. 3–9. APC circuit

IC252 (AN7675) is for APC.

When the circuit receives LD ON signal from the system microcomputer, the level at pin (4) of IC252 becomes "H".

Then, the level at pin (8) becomes "H" causing Q251 to operate and LD (laser diode) lights up. At the same time, LD STATE (laser confirming) signal at pin (6) becomes "H".

APC operation detects the light intensity of LD by the pin diode.

If the light intensity of LD is increased, the voltage at pin (7) is lowered, causing the voltage at pin (8) to lower. Conversely, if the light intensity of LD is decreased, the voltage is lowered.

° VR254 is a semi-fixed resistor to change the voltage detected at pin (7) of IC252, and it is able to change the light intensity of LD. In SL-P10, it is adjusted so that the light from the focus lens is 0.32 mW.

Incidentally, -15 V from CN251 pin (9) is supplied through LD switch (that turns ON with holder closed) of the loading mechanism.

The laser diode lighting timing ranging from insertion of disc into disc holder to play mode is illustrated in the Fig. 3–10.

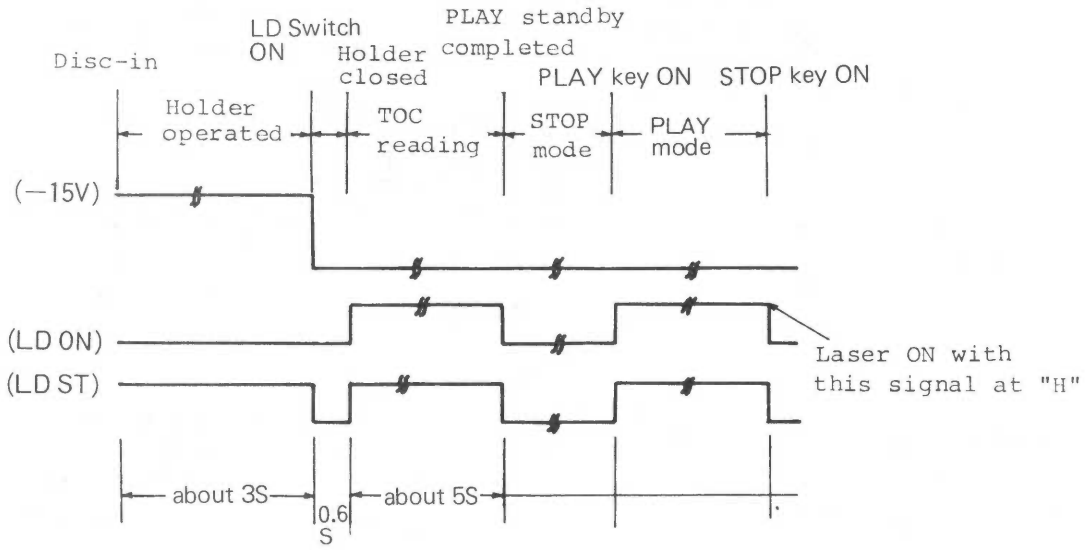


Fig. 3–10. Laser diode ON timing

5. Focus servo circuit operation

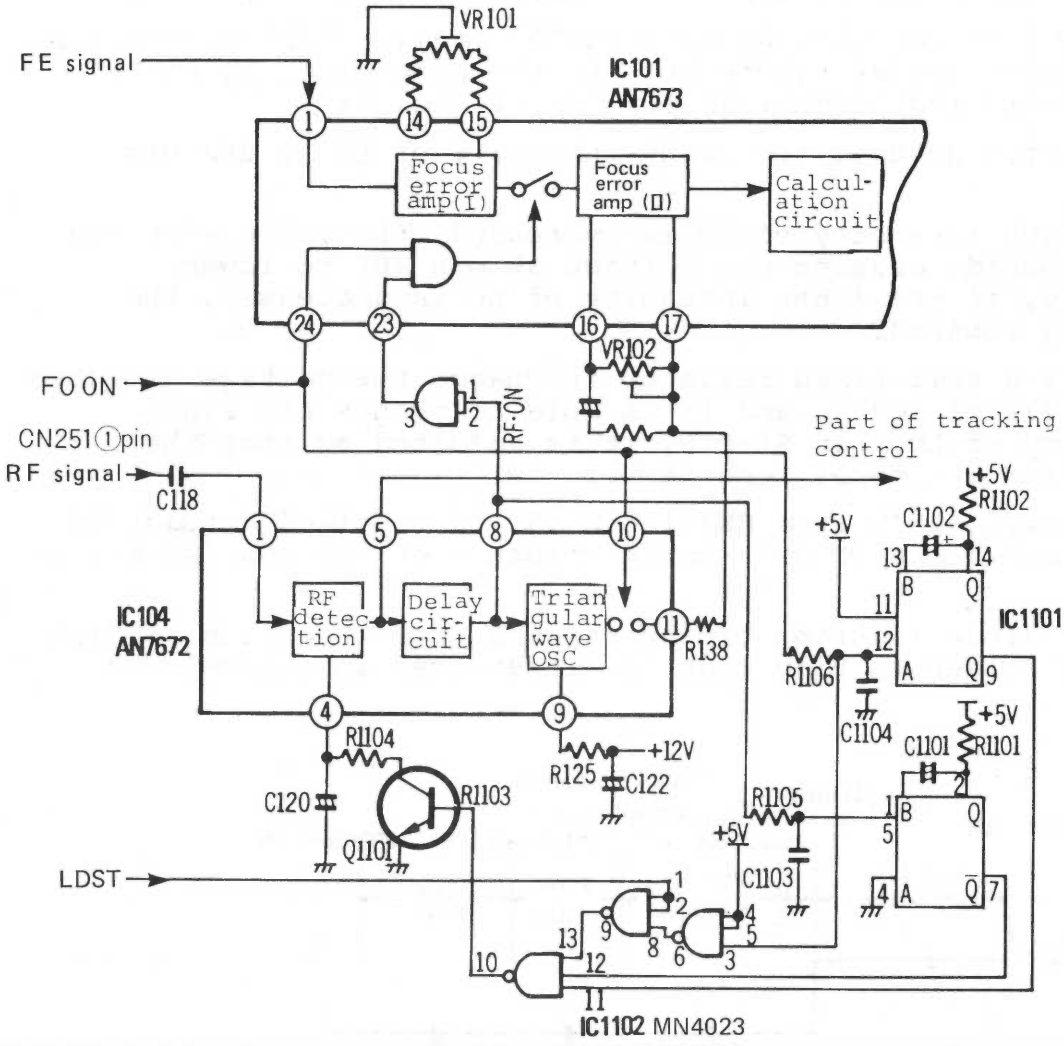


Fig. 3–11. Auto focus circuit

(1) FO ON command is delivered from system microcomputer, causing CN704 pin (2) and IC104 pin (10) to become "H". As a result, the sawtooth wave made by the triangular wave oscillator in IC104 is delivered to IC104 pin (11).

(2) The sawtooth wave is applied from R138 to the focus servo amplifier input [AN7673 pin (17)] thus forcibly move the focus lens in the focusing direction.

(3) When the focus lens moves and is focused, RF signal from photo detector comes out of CN251 pin (1). The RF signal is applied to IC104 pin (1) through C118 (high pass filter), then the sawtooth wave delivered to IC104 pin (11) stops and simultaneously IC104 pin (8) (RF ON detection) goes "H".

(When IC104 pin (8) is "H", the focus servo loop switch selected at IC101 (AN7673) pin (23) is closed to activate focus servo.)

The operation timing ranging from auto focus operation until focus servo operation is shown in Fig. 3–12.

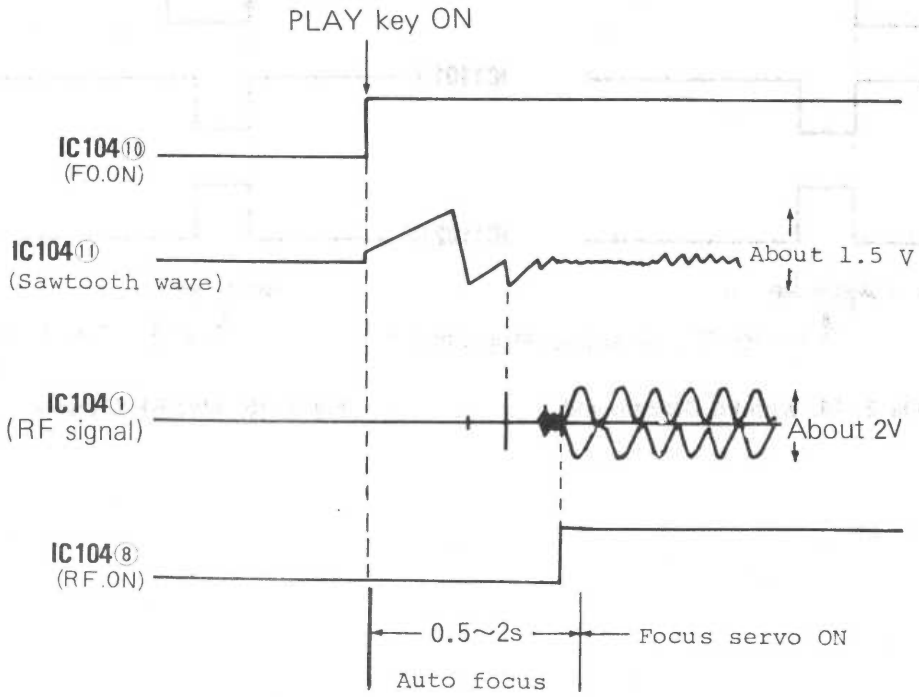


Fig. 3–12. Auto Focus → Focus servo ON timing chart

° Pulse signal of TT level according to RF signal can be obtained at IC104 pin (5). The signal is called RF real signal, and its relation with RF signal is shown in Fig. 3–13. The signal is used as part of tracking servo loop switch.

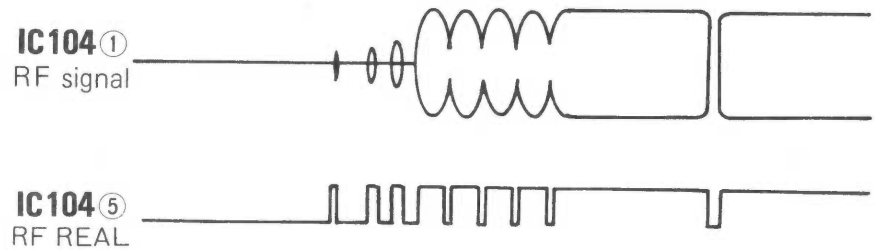


Fig. 3–13. RF signal and RF REAL signal

° The circuit consisting of IC1101 (MN4528) and IC1102 (MN4023) discontinued detection of RF ON [IC104 pin (8)] for 80 ms after delivery of FO ON and RF ON.
The purpose of this is to stabilize FE signal during retraction of focus servo.

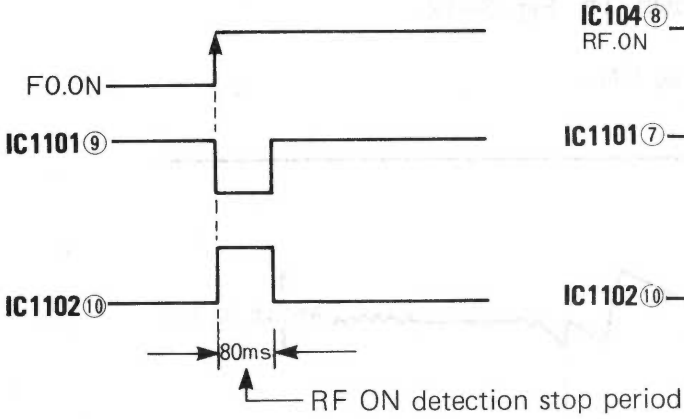


Fig. 3–14. With FO ON delivered

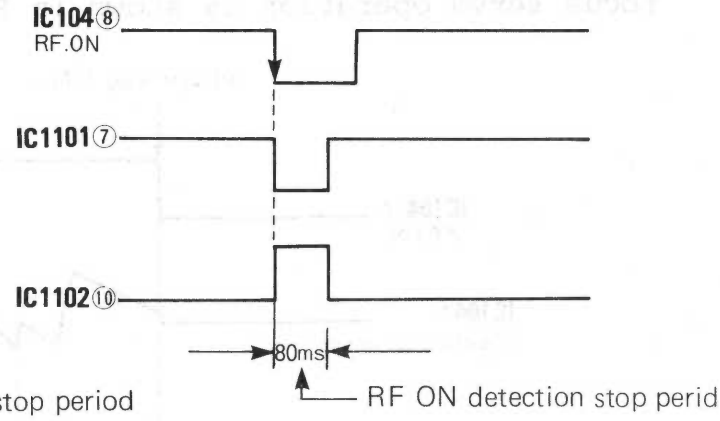
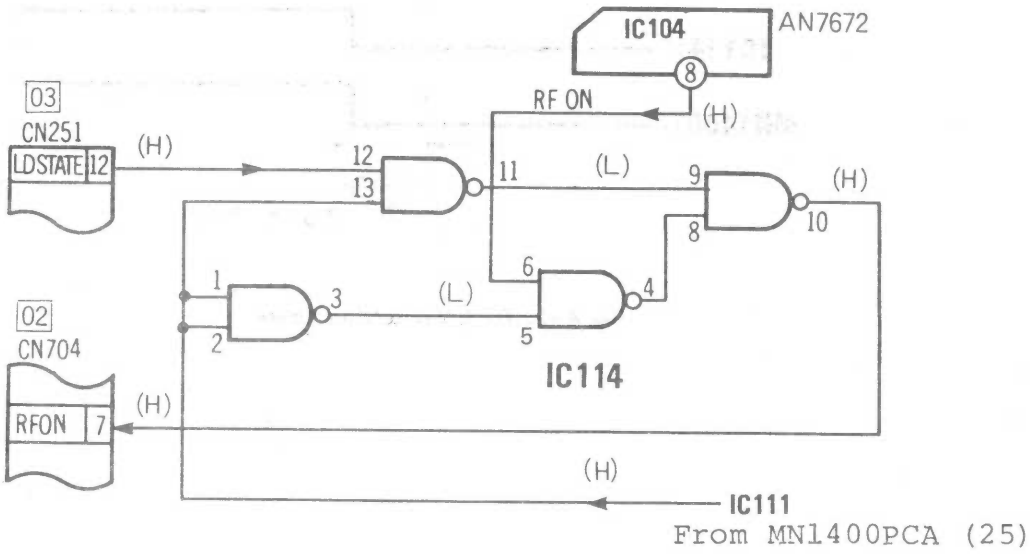


Fig. 3–15. With RF ON gone

4. Tracking servo circuit operation

4–1. RF ON detection circuit operation

The actual circuit that delivers RF ON signal to the system microcomputer is shown in Fig. 4–1.



(H) Level in PLAY mode is parenthesized.

Fig. 4–1 RF ON detection circuit

(1) When PLAY key is depressed, CN251 pin (12) goes "H" on laser lighting.

(2) When auto focus is activated due to focus search operation, IC104 pin (8) goes "H".

(3) When (1) and (2) are at "H", CN704 pin (7) delivers RF ON signal to system microcomputer.

After confirming the RF ON signal, system microcomputer delivers TR ON signal to activate tracking servo and simultaneously delivers PLAY command signal to MN1400 traverse microcomputer.

IC111 MN1400 pin (25) will become "H" from this command.

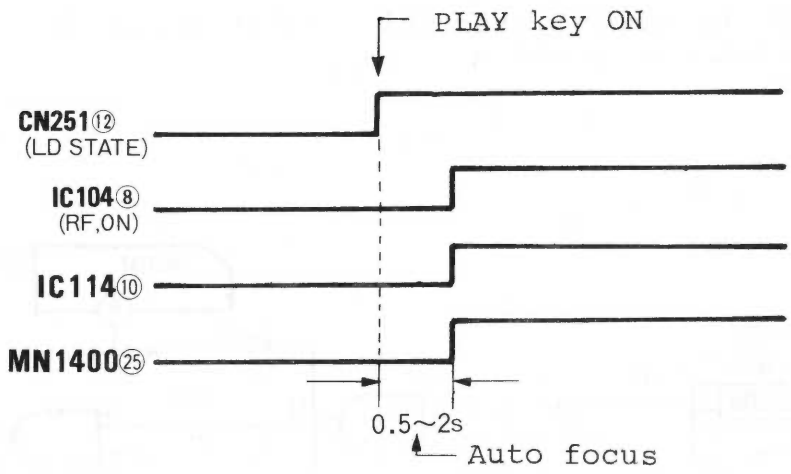


Fig. 4–2. RF ON detection timing

4–2. Tracking error head amp circuit operation

Before proceeding to the circuit that processes TR ON signal from the system microcomputer, the operation of tracking error amplifier and low frequency compensating circuit is explained here.

- Tracking error amp.

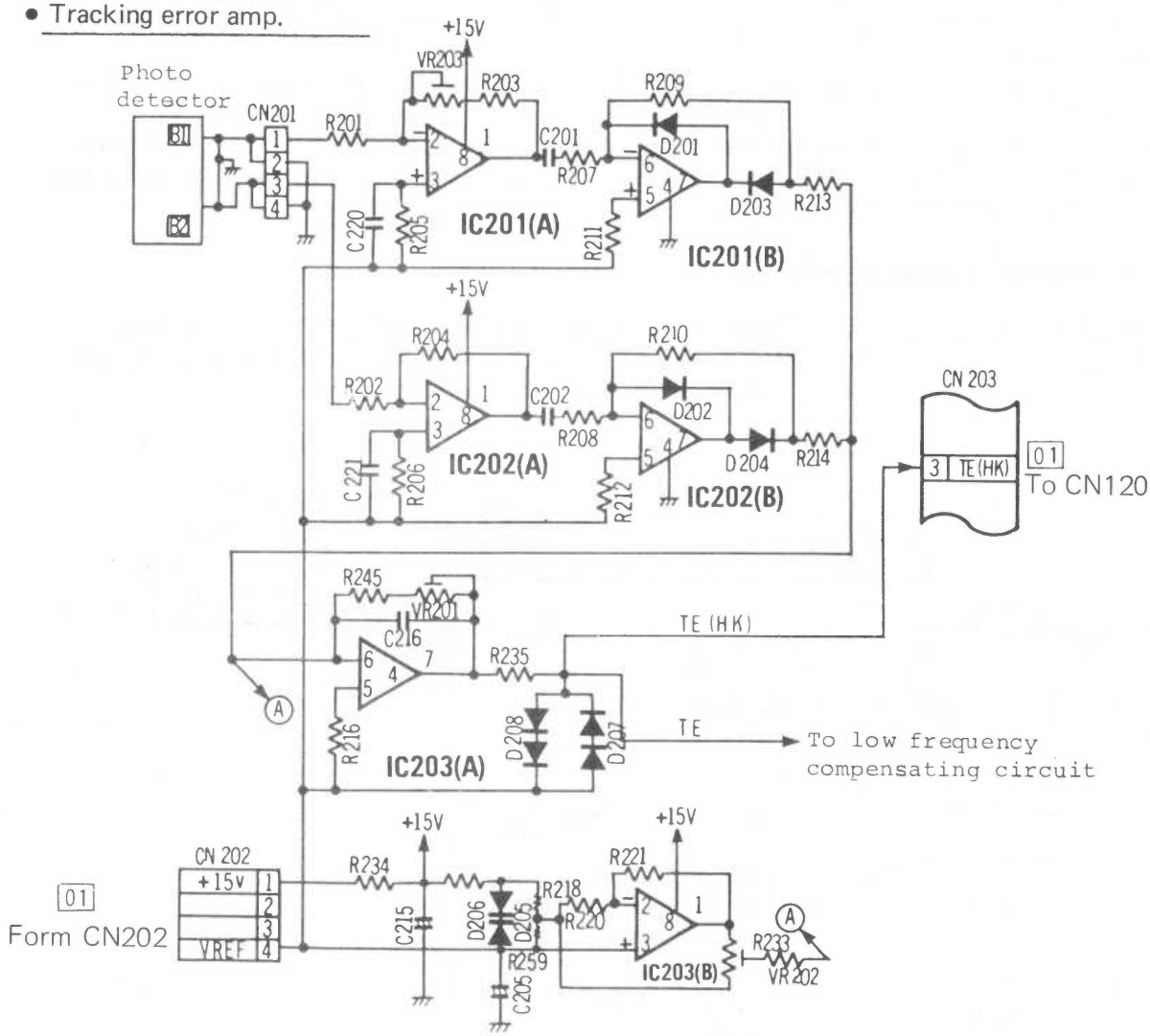


Fig. 4–3. Tracking error amplifier

(1) Tracking signals detected by tracking photo detector B_1 and B_2 are amplified by IC201 (A) and IC202 (A). The signals are then converted to positive and negative tracking signals by the detection circuit consisting of IC201 (B), 202 (B), and D201 ∿ 204.

(2) The positive and negative signals are added at R213 and R214, then the output difference between photo detectors B_1 and B_2 appears at pin (6) of IC203 (A). The level difference is tracking error (TE) signal.

(3) The tracking error signal is amplified at IC203 (A), and is delivered to the low frequency compensating circuit in the next stage. TE signal controls the traverse servo.

° Inverted amplifier consisting of IC203 (B) is a circuit to apply offset voltage to IC203 (A).
° VR201 is a semi-fixed resistor to adjust tracking servo loop gain and is adjusted so that output from photo detector is 2 Vp-p at IC203 (A) with tracking servo loop switch OFF.
° VR202 is a semi-fixed resistor to adjust offset voltage of IC203 (A) and is adjusted so that the voltage is at the same level of V REF (reference voltage) of CN202 pin (4) during stop mode.
° VR203 is a semi-fixed resistor to make the P-P levels of output delivered to D203 (anode) and D204 (cathode) equal to each other, and is adjusted so that the peaks of output waveform of IC203 pin (7) are same in positive and negative values with tracking servo switch OFF.

4–3. Low frequency compensating circuit

Tracking error signal from tracking error amplifier is shown in Fig. 4–4. It is subjected to low frequency compensation in order to stabilize the tracking servo operation.

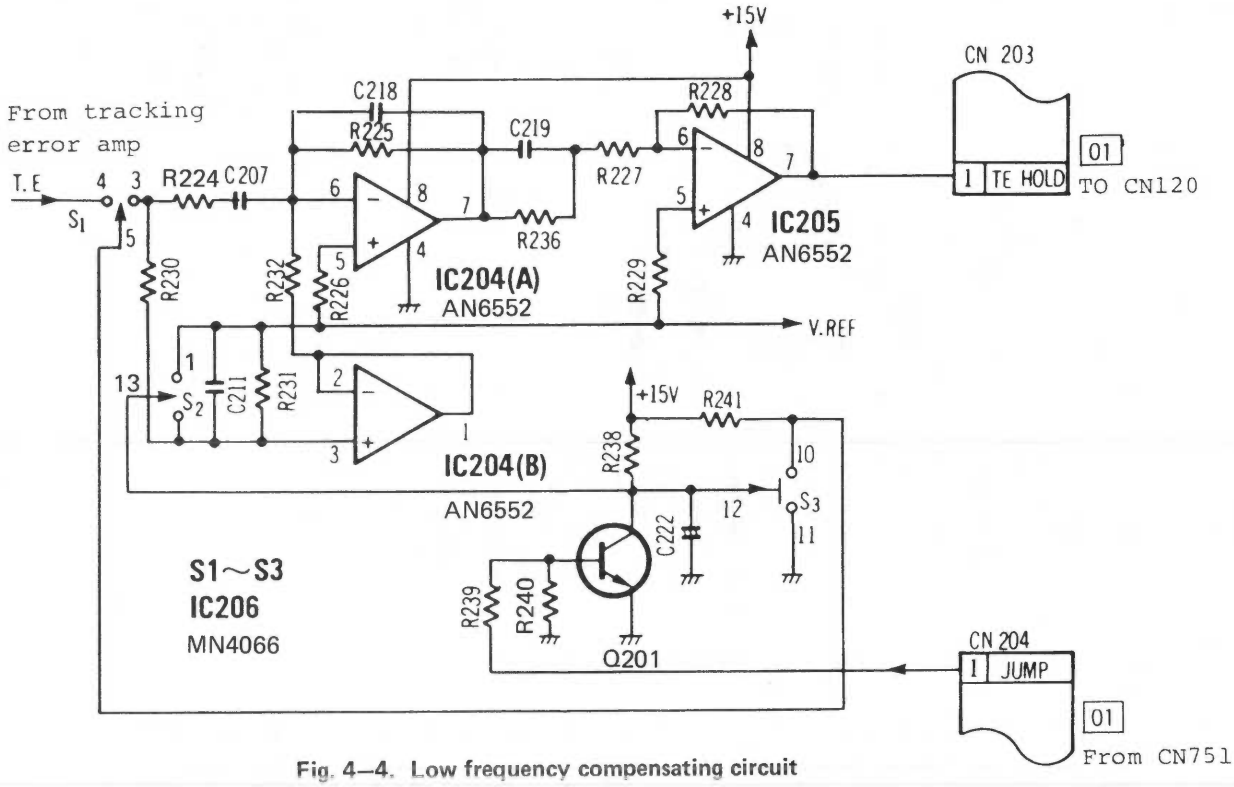


Fig. 4–4. Low frequency compensating circuit

TE signal from tracking error amplifier is applied to the input terminal [IC204 (A) pin (6)] of active filter consisting of IC204 (A), 205 and CR through S_1, thereby attenuating the high frequency part, and is delivered from CN203 pin (1) as tracking hold (TE HOLD) signal in order to control the tracking focus calcultion of 01 PCB.

° IC204 (B) serves to mix the DC part that is cut off by the input condenser C207 of IC204 pin (6) into IC204 (A) pin (6) by R232.

° The switch circuit consisting of IC206 (S_1 ∿ S_3) and Q206 turns Q201 OFF by CN204 $\overline{\text{JUMP}}$ signal (same as AN7673 pin (22) tracking servo loop switch control signal) during manual high-speed search, and makes the output level of IC205 pin (7) same as the level of V REF (reference voltage).

The operation timing of each terminal is shown in Fig. 4-6.

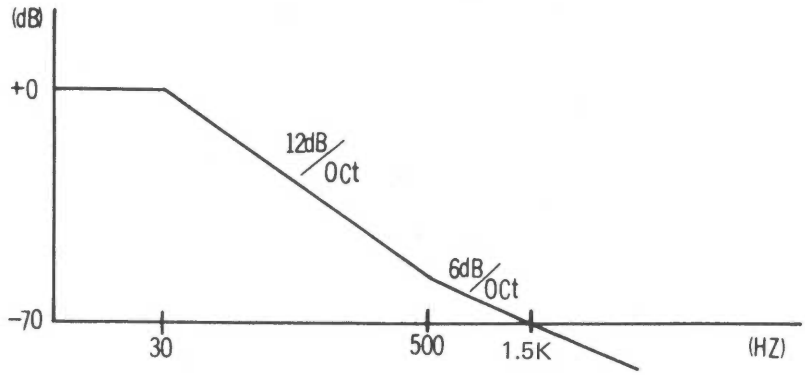
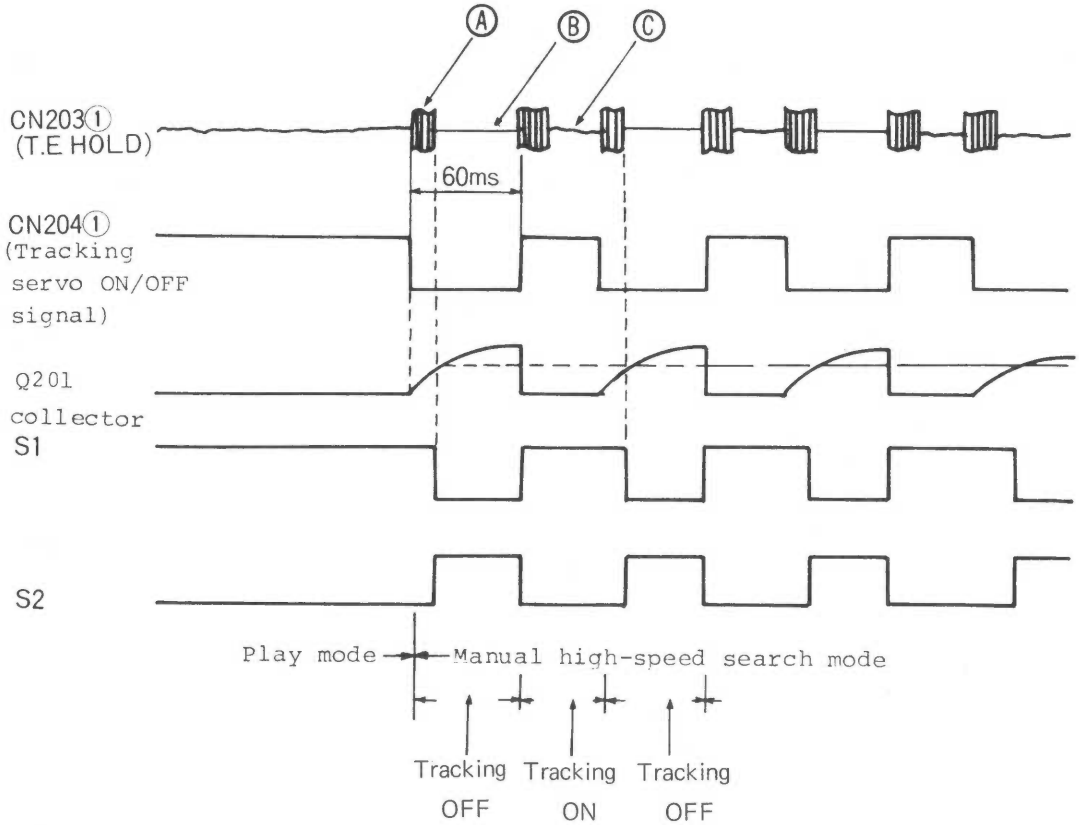


Fig. 4–5. Low frequency compensating circuit frequency characteristic



(A) TE signal when tracking servo is released.

(B) TE signal when IC205 pin (7) is made equal to V REF level by S_2.

(C) TE signal when tracking servo is activated.

Fig. 4–6. Operation timing in manual high speed mode

4–4. TR ON signal processing block circuit diagram

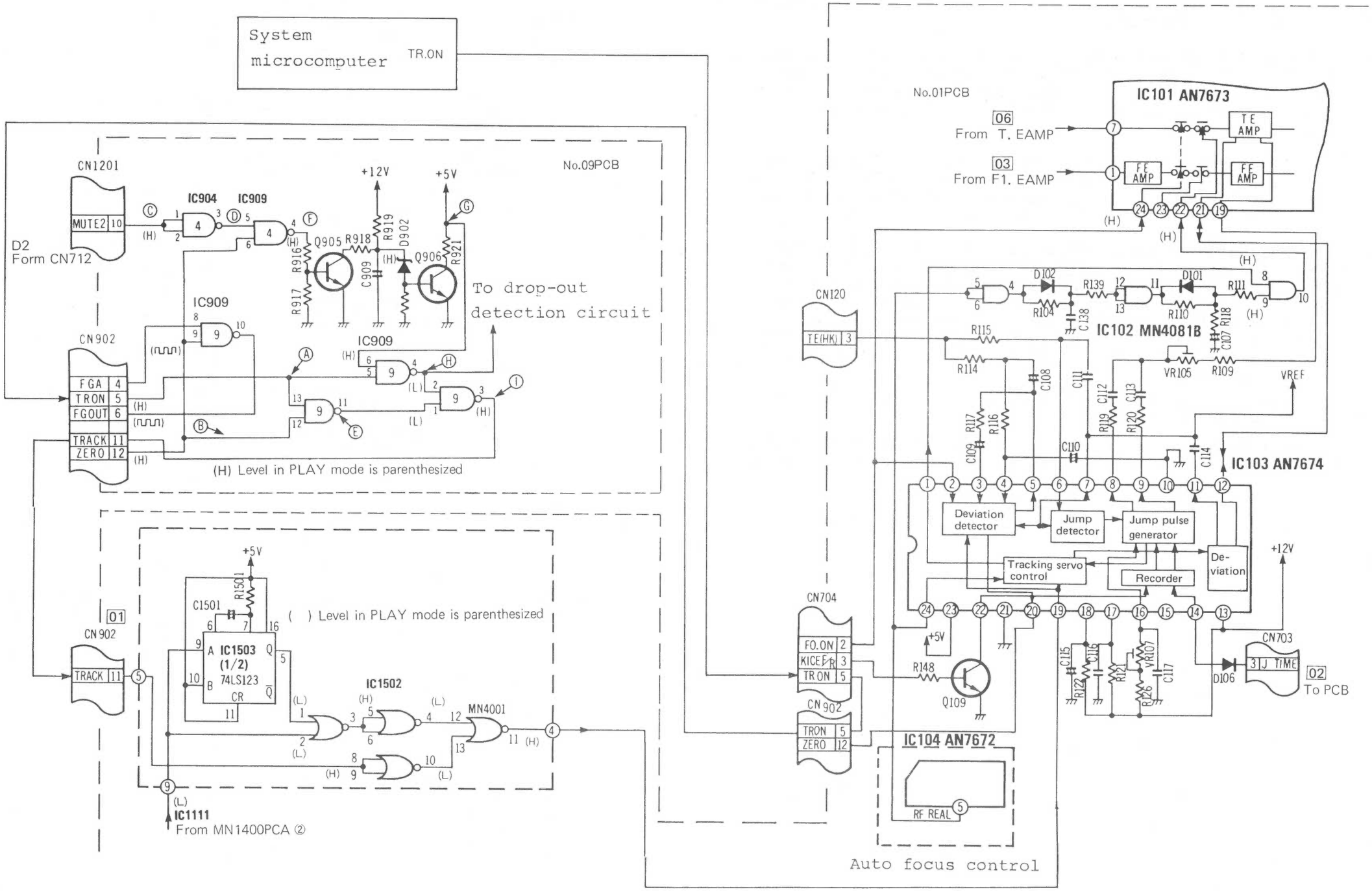


Fig. 4–7. TR ON signal processing block circuit

• Circuit operation of TR ON signal processing block

TR ON signal from system microcomputer passes through the circuit of Fig. 4–7 and turns ON the tracking servo loop switch of IC101 pin (22) (AN7673).

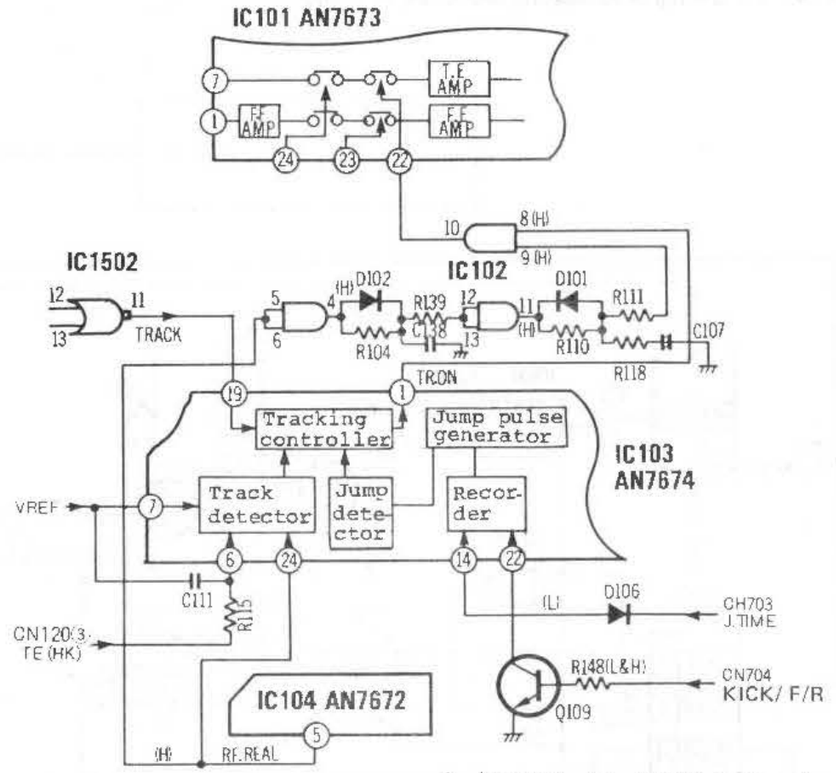
(1) System microcomputer delivers TR ON signal to CN902 pin (5) of 09 P.C.B. Then IC909 pin (5) goes "H" and CN902 pin (12) (ZERO) of 09 P.C.B. goes "L", causing IC909 pin (6) to go "H". Therefore, IC909 pin (4) goes "L".

(2) When IC909 pin (4) goes "L", the level of CN902 pin (11) of 09 P.C.B. is "H" irrespective of whether IC909 pin (1) is at "H" or "L". The operation timing when the mode is shifted from STOP to PLAY is shown in Fig. 4–9.

(3) Track signal applied to CN902 pin (11) of 01 P.C.B. from CN902 pin (11) of 09 P.C.B. causes IC1502 pins (8), (9) to change to "H". As a result, IC1502 pin (10) goes "L", and IC1502 pin (12) goes "H" for about 20 ms immediately after the stepping motor of traverse servo stops rotating at an extra-high speed, but it is at "L" during normal play mode. Therefore, the level of IC1502 pin (11) is "H".

The operation timing when the mode is shifted from STOP to PLAY is shown in Fig. 4–11.

The operation timing in mode random access play mode when the stepping motor moves at an extra-high speed is shown in Fig. 4–10.



Auto focus control circuit ( )Level in PLAY mode is paranthesized.

Fig. 4–8. Enlarged view of IC103 AN7674

(4) When IC1502 pin (11) becomes "H", IC103 pin (19) goes "H", causing tracking controller in IC103 to stand by.

In this condition, when the point at which tracking error (TE) signal, IC103 pin (6), from tracking error amp intersects with the V REF (reference voltage) level of IC103 pin (7) is synchronized with the point at which RF REAL signal, IC103 pin (24), from AN7672, then on-the-track detector delivers signal to tracking controller, making the level of IC103 pin (1) (TR ON) "H".

IC102 pin (9) goes "H" about 0.3 sec after entry of RF REAL signal from AN7672 to IC102 pins (5), (6). Then, IC102 pin (10) goes "H", actuating tracking servo.

The operation timing of IC103 and IC102 is shown in Fig. 4-12.

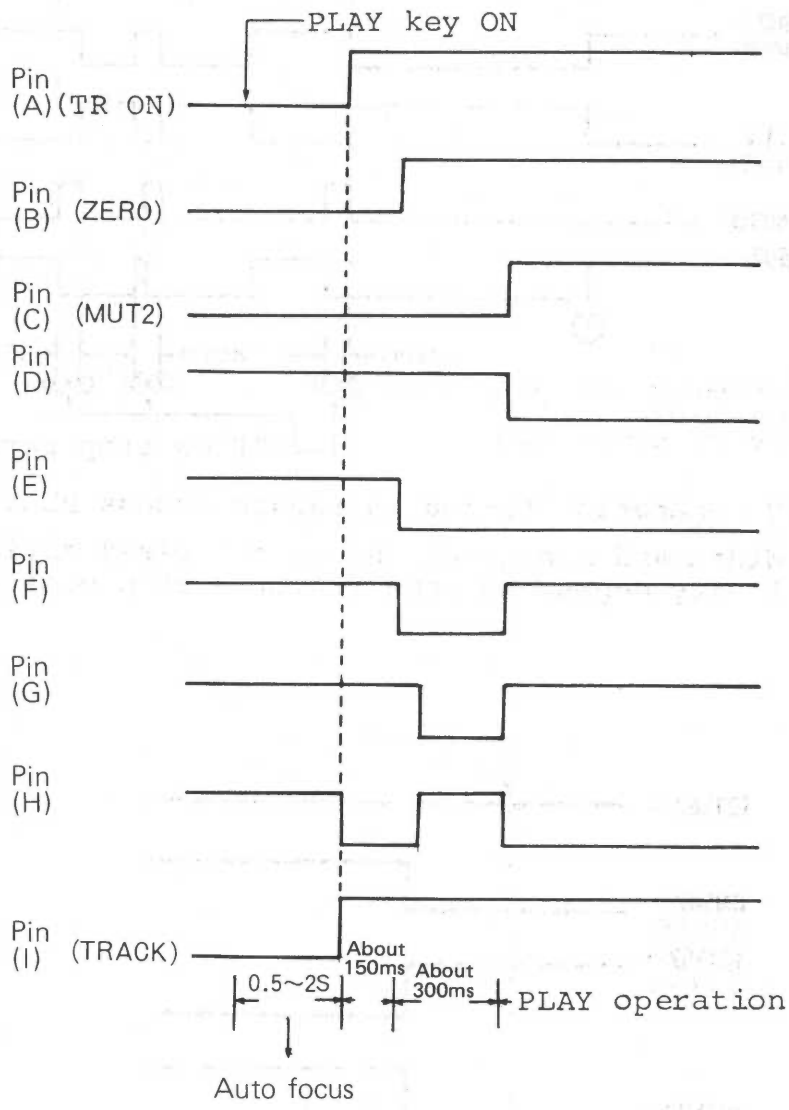
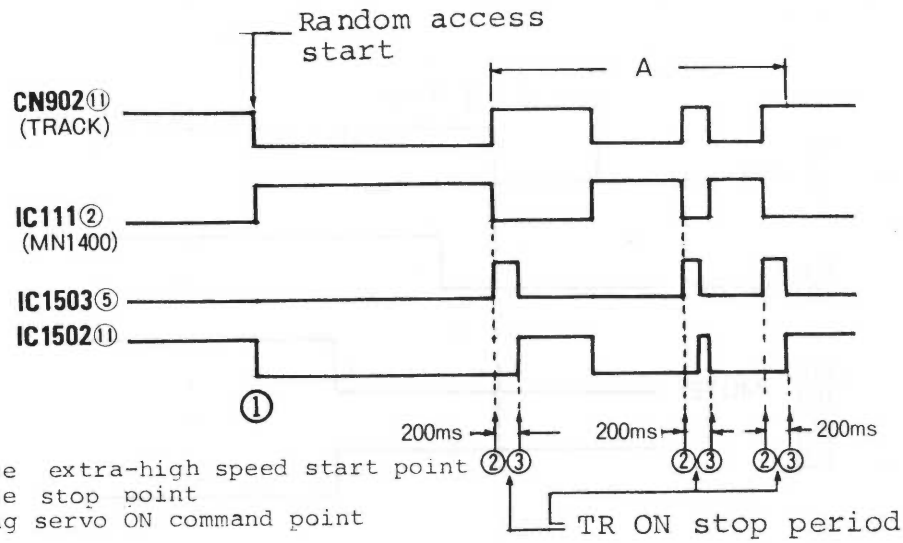


Fig. 4–9. Operation timing with P.C.B. shifted from STOP to PLAY mode



(1) Traverse extra-high speed start point
(2) Traverse stop point
(3) Tracking servo ON command point

Fig. 4-10 Operation timing in random access PLAY mode

Note) Width and number of pulses delivered during period A vary depending upon traverse stop position.

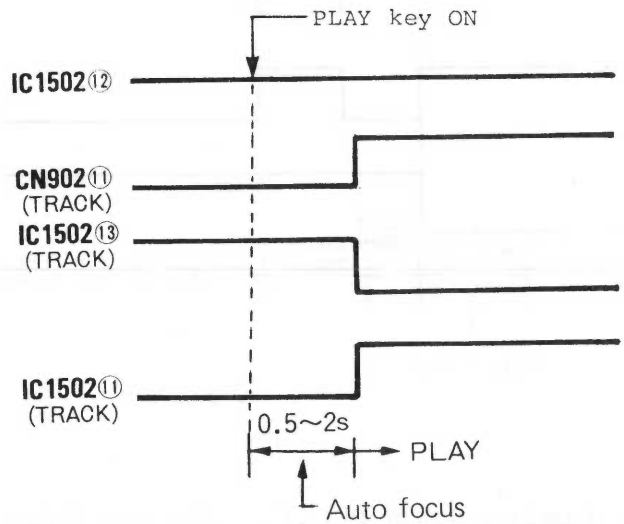


Fig. 4-11 Operation timing in STOP → PLAY mode

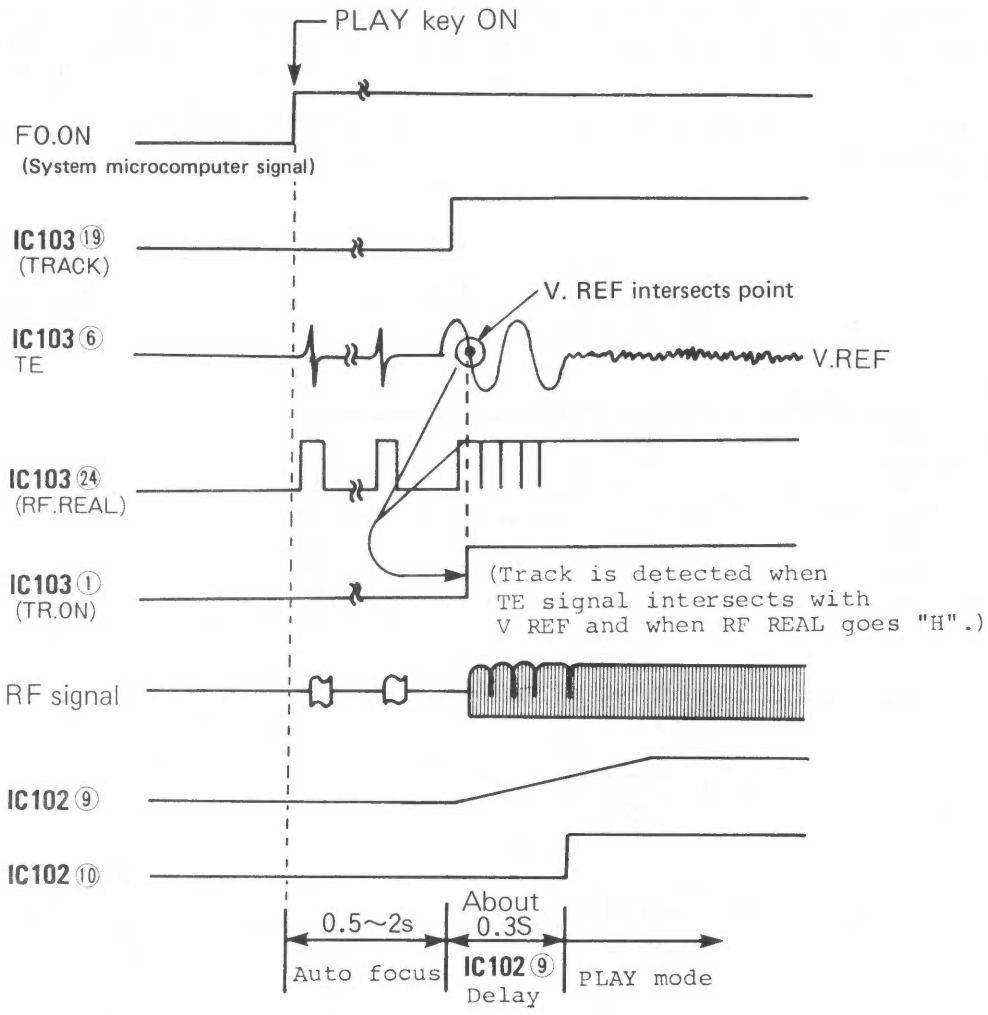


Fig. 4–12. Operation timing with IC103 and IC101 shifted from STOP to PLAY mode

4–5. Calculation and actuator drive circuit operation

Since the activated coil to drive the focus lens, is of cross winding, the focus error and tracking error signals are converted into sum signal (TE + FE) and difference signal (TE - FE) by the calculation circuit, and current is let to flow into 2 sets of actuator coil.

IC101 is the calculation circuit, and IC105 and IC106 are the drive circuit.

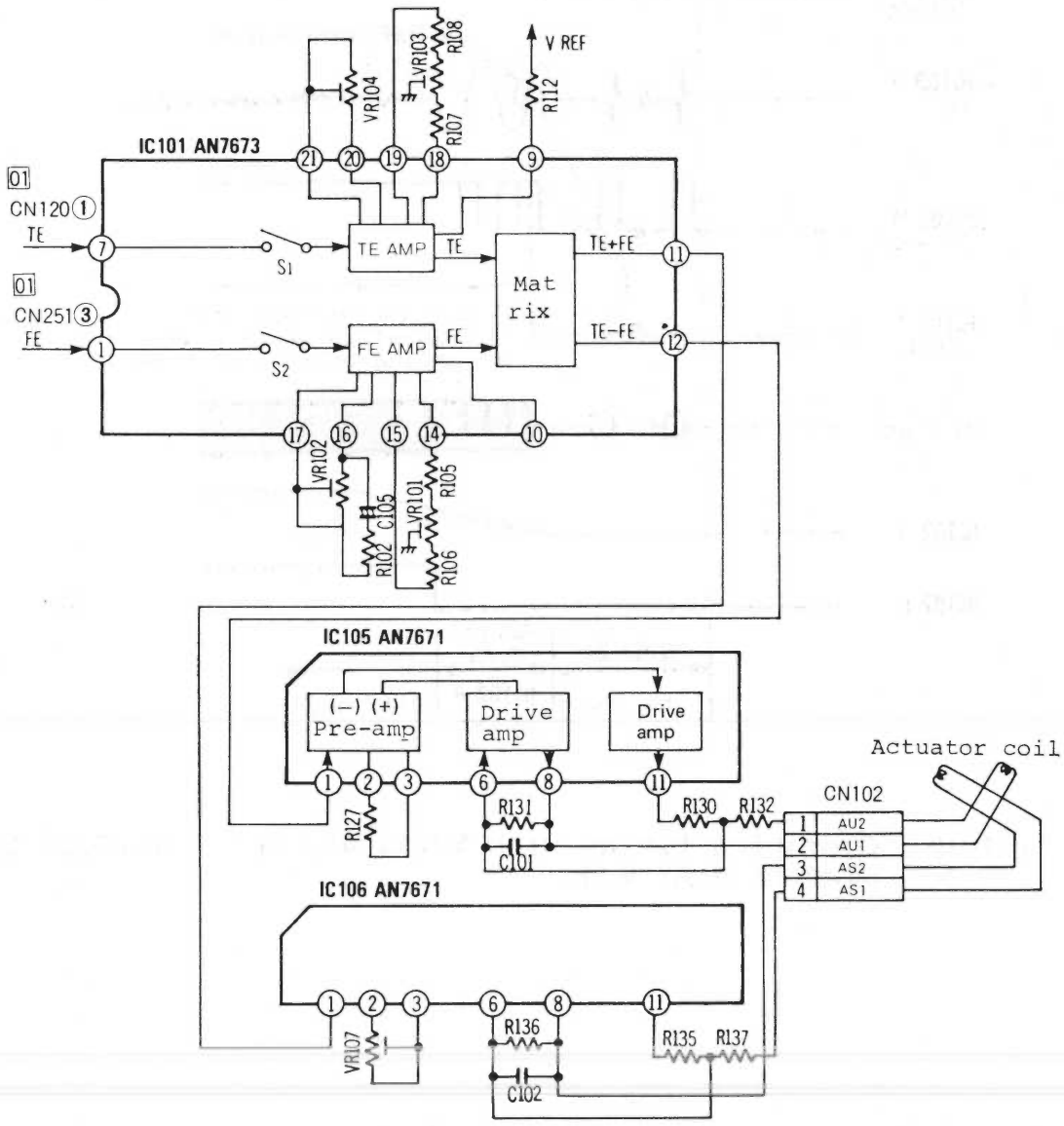


Fig. 4–13. Calculation and actuator drive circuit

(1) TE and FE signals passed through servo loop switches S_1 and S_2 are amplified by TE AMP and FE AMP, and then they are converted into (TE + FE) signal and (TE - FE) signal before being delivered to IC101 pin (11) and pin (12).

(2) Signals delivered to IC101 pins (11), (12) are applied to IC105 and IC106 pin (1) where they are amplified in power, and work to drive the actuator coil.

The actuator coil is of BTL drive as shown in Fig. 4–14.

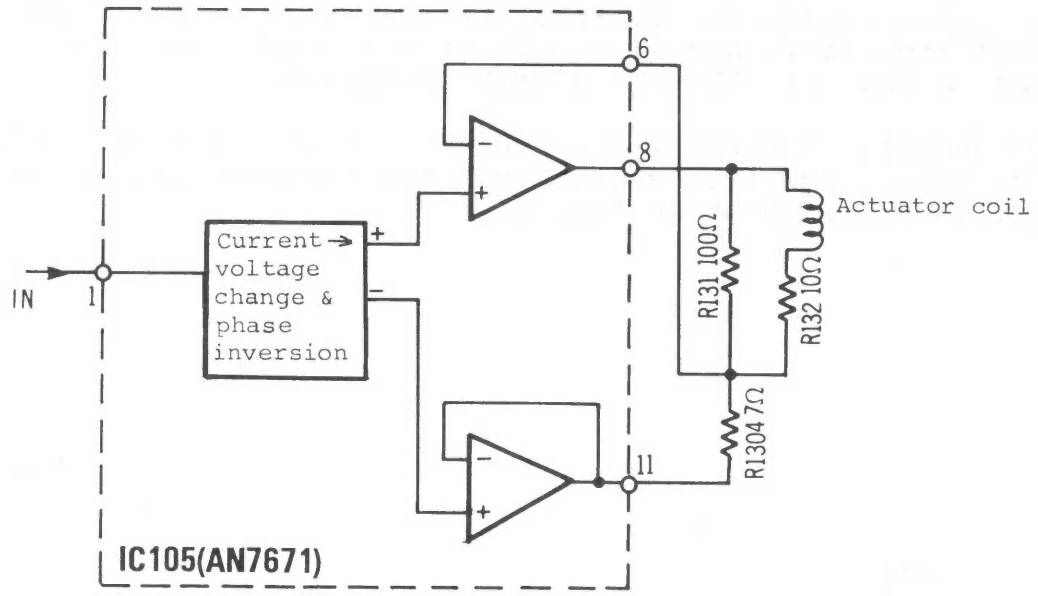


Fig. 4–14. AN7671 equivalent circuit

° VR101 is a semi-fixed resistor to adjust the offset of FE AMP in IC101 (AN7673), and it is adjusted so that no current flows into actuator coil during STOP mode.

° VR102 is a semi-fixed resistor to adjust the gain of FE AMP in IC101 (AN7673), and it is adjusted to the maximum gain position.

° VR103 is a semi-fixed resistor to adjust the offset of TE AMP in IC101 (AN7673), and it is adjusted so that no current flows into actuator coil during STOP mode.

° VR104 is a semi-fixed resistor to adjust the gain of TE AMP in IC101 (AN7673), and it is adjusted so that the tracking servo loop gain is 70 dB.

° VR107 is a semi-fixed resistor to adjust the gain of (TE - FE) signal amplifier, and it is adjusted so that the gain is equal to that of (TE + FE) signal amplifier.

° C105 and R102 determine the frequency characteristic of focus servo loop. The frequency characteristic and gain of focus servo loop are shown in Fig. 4–15.

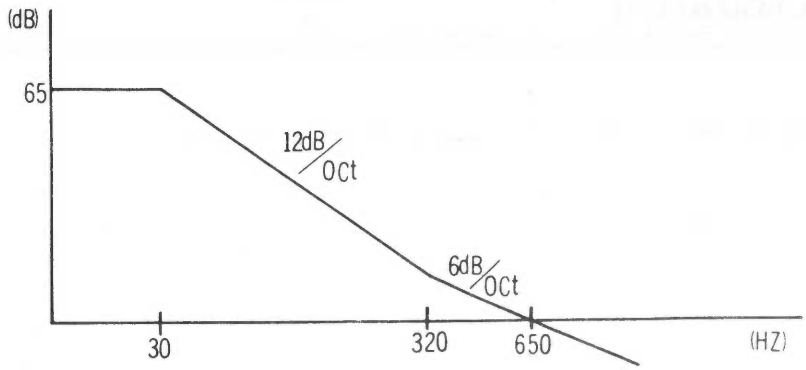


Fig. 4–15. Frequency characteristic and gain of focus servo loop

4–6. Reference voltage generation circuit (V REF) operation

The circuit generates DC operation reference (bias) point voltage of focus and tracking servo amplifier to apply DC bias (medium point voltage) to tracking error amplifier and low frequency compensating amplifier (OP AMP). Also, it is the reference voltage for zero cross and on-the-track detection of AN7674.

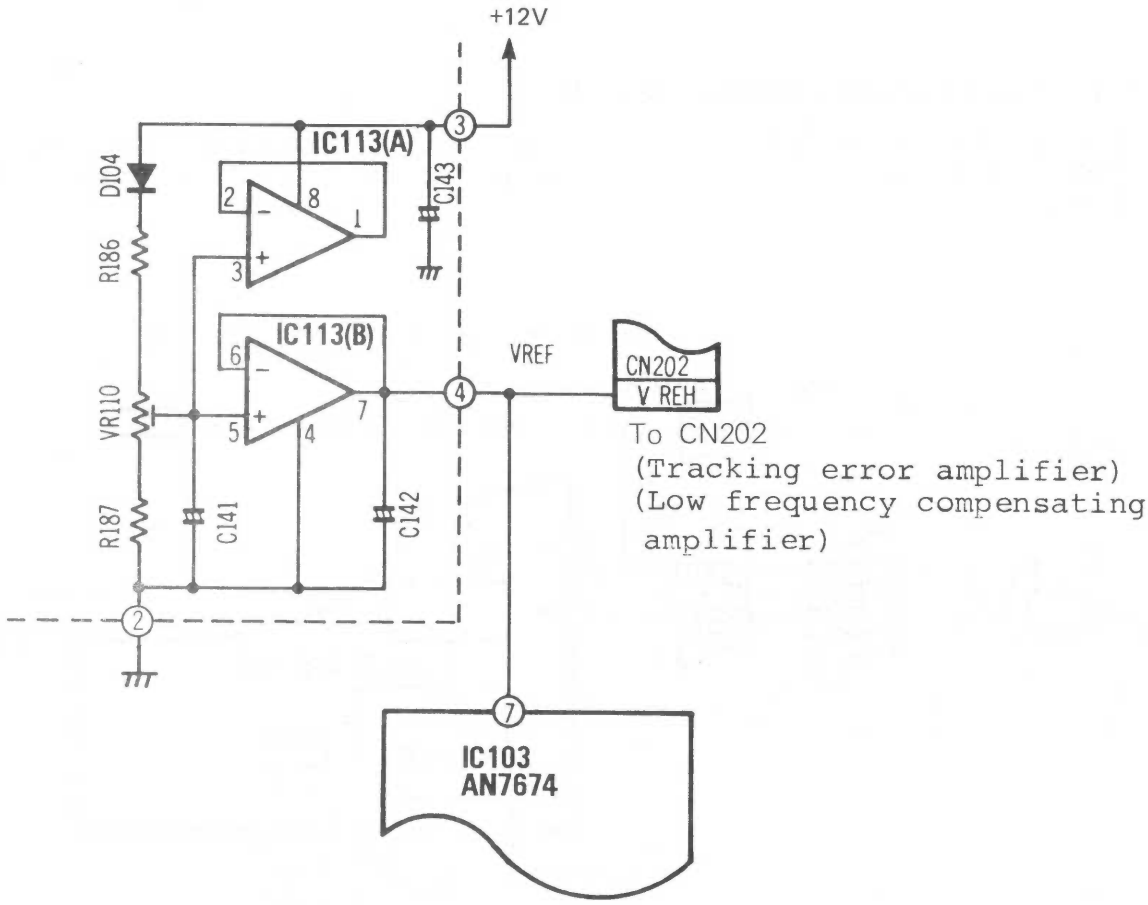


Fig. 4–16. V REF circuit

° IC113 (B) consists of non-inverse buffer amplifier of OP AMP. So, the voltage of IC113 (B) pin (5) is changed in impedance and is delivered to IC113 (B) pin (7).

° VR110 is a semi-fixed resistor to change the output voltage of IC113 (B) pin (7), and it is adjusted so that the voltage is equal to the offset voltage at focus error amplifier of focus tracking calculation amplifier (AN7673). (The voltage is about 5.7 V.)

4–7. Track jump control circuit operation

During the above-mentioned pause and manual low-speed search forward mode, laser beam jumps from inner to outer periphery of the disc, and the back jump control circuit operates. During manual low-speed search reverse mode, laser beam jumps from outer to inner periphery of the disc, and the forward jump control circuit operates. These two control operations are explained in the following.

4–8. ZERO CROSS detection circuit opertion

It detects the minimum deviation point of the disc and works to send the signal of minimum deviation point to the system micro-computer.

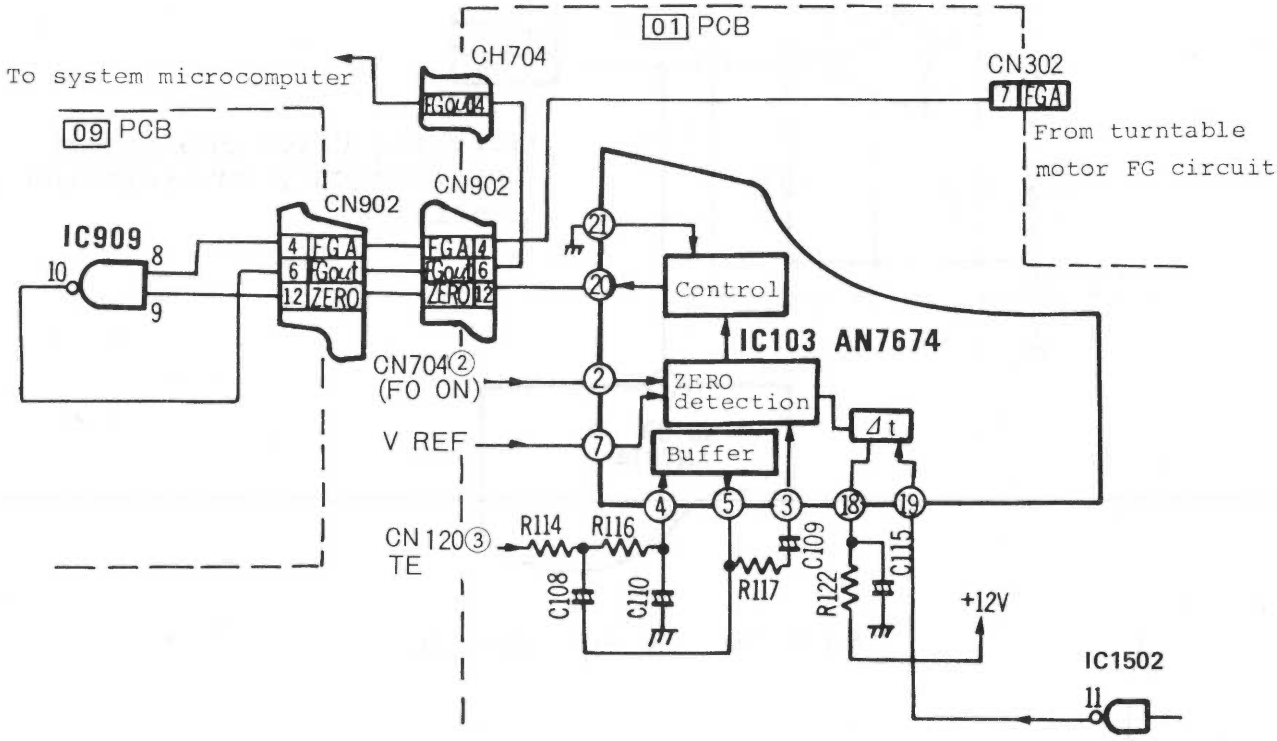


Fig. 4–17. ZERO CROSS detection circuit

(1) FO ON signal is applied to CN704 pin (2) from system microcomputer, then IC103 pin (2) goes "H" and the ZERO detection block in IC103 stands by.

(2) When focus servo is activated and TR ON signal is delivered from system microcomputer, then IC103 pin (19) goes "H". As a result, C115 to set the ZERO CROSS detection start time is charged by R122.

(3) As C115 is charged causing IC103 pin (18) to go "H", then ZERO detection block in IC starts to detect ZERO CROSS. In this condition, the tracking error signal from CN120 pin (3) crosses with V REF (reference voltage) of IC103 pin (7), then IC103 pin (20) goes "H".

(4) When IC103 pin (20) goes "H", IC909 pin (9) changes to "H". Consequently, FG signal applied to IC909 pin (8) is delivered to IC909 pin (10). FG signal thus delivered causes the system microcomputer to be informed of the ZERO CROSS point. The ZERO CROSS timing is shown in Fig. 4-18.

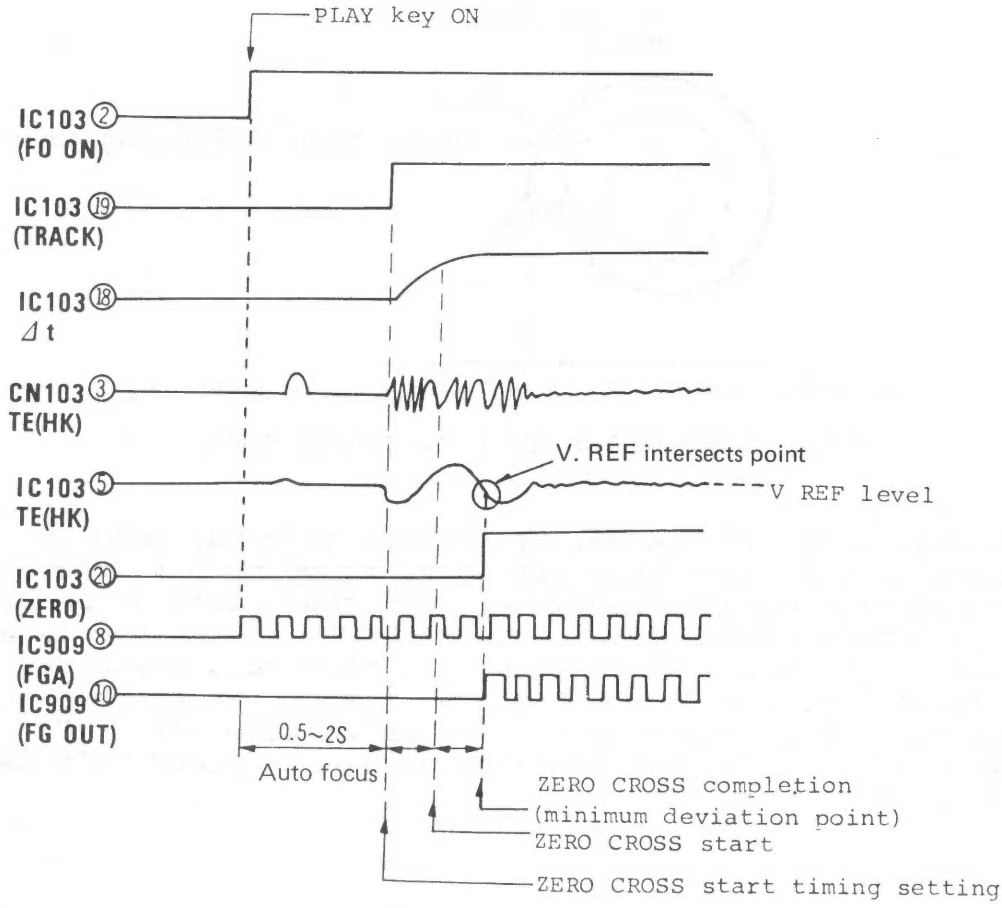


Fig. 4-18. ZERO CROSS timing

4–9. Track jump control

According to the jump timing (J. TIME in circuit diagram stands for jump timing) command from the system microcomputer during trick play, the focus lens is forcibly jumped to the inner or outer periphery of the disc.
It is pause and play lowspeed research in a mode that requires track jump.

° Pause mode

When the set is in pause mode, releasing the pause will cause a different tune to be played unless the laser beam follows up the same track. Therefore, a command signal is given from the system microcomputer every time the disc rotates in order to let the focus lens jump to return the laser beam to the original track (pause point). (The idea is the same as for still image playback in VTR.)

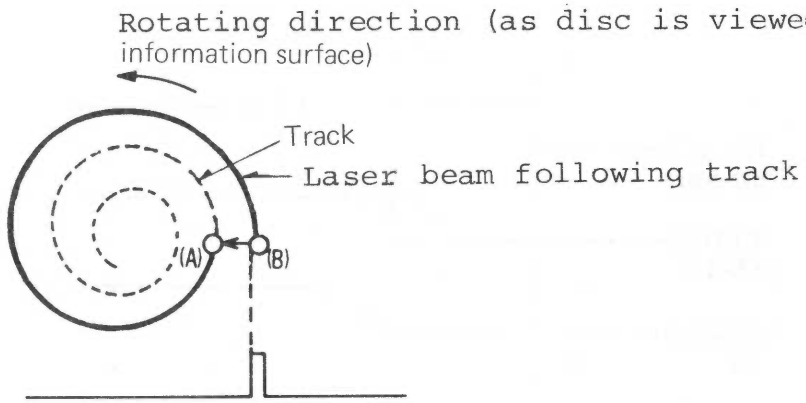


Fig. 4–19. Track jump in pause mode

In Fig. 4–19, if the set is shifted to pause mode at point A, the laser beam will move to point B as the disc is rotating counterclockwise. The focus lens at point B is jumped toward point A in order to return the laser beam to the original point A. In this way, the laser beam will follow up the track at point A where the set was shifted to pause mode. The operations (A) → (B) ... (A) → (B) ... (A) are repeated until the pause mode is released.

• Manual low-speed search forward

When the set is in manual low-speed search forward, the laser beam lets the display time advance 3 times faster than in play mode according to the jump timing command from system microcomputer. As shown in Fig. 4–20, the disc rotation is jumped by 2 tracks each to shift the laser beam to the outer periphery.

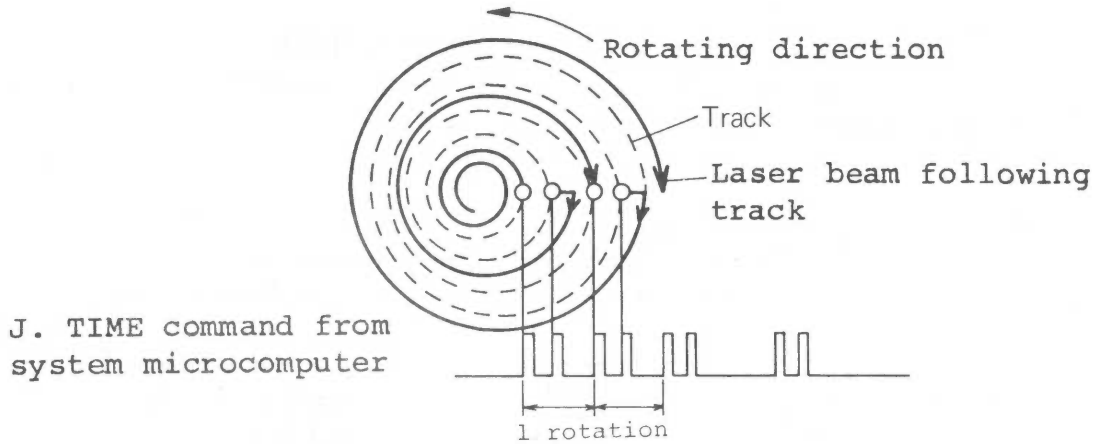


Fig. 4–20. Track jump in manual low-speed search forward mode

• Manual low-speed search reverse

When the set is in manual low-speed search reverse mode, the laser beam lets the display time delay 3 times faster than in play mode according to the jump timing command from system microcomputer. As shown in Fig. 4–21, the disc rotation is jumped by 3 tracks each to shift the laser beam to the inner periphery.

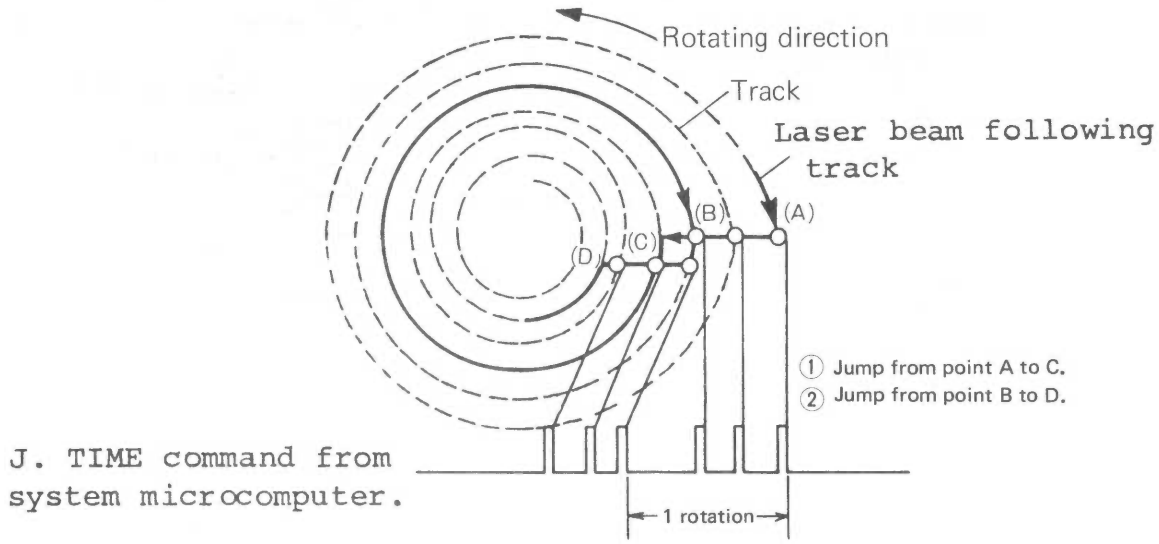


Fig. 4–21. Track jump in manual low-speed search reverse

4–10. Track jump control circuit operation

During the above-mentioned pause and manual low-speed search forward mode, laser beam jumps from inner to outer periphery of the disc, and the back jump control circuit operates. During manual low-speed search reverse mode, laser beam jumps from outer to inner periphery of the disc, and the forward jump control circuit operates. These two control operations are explained in the following.

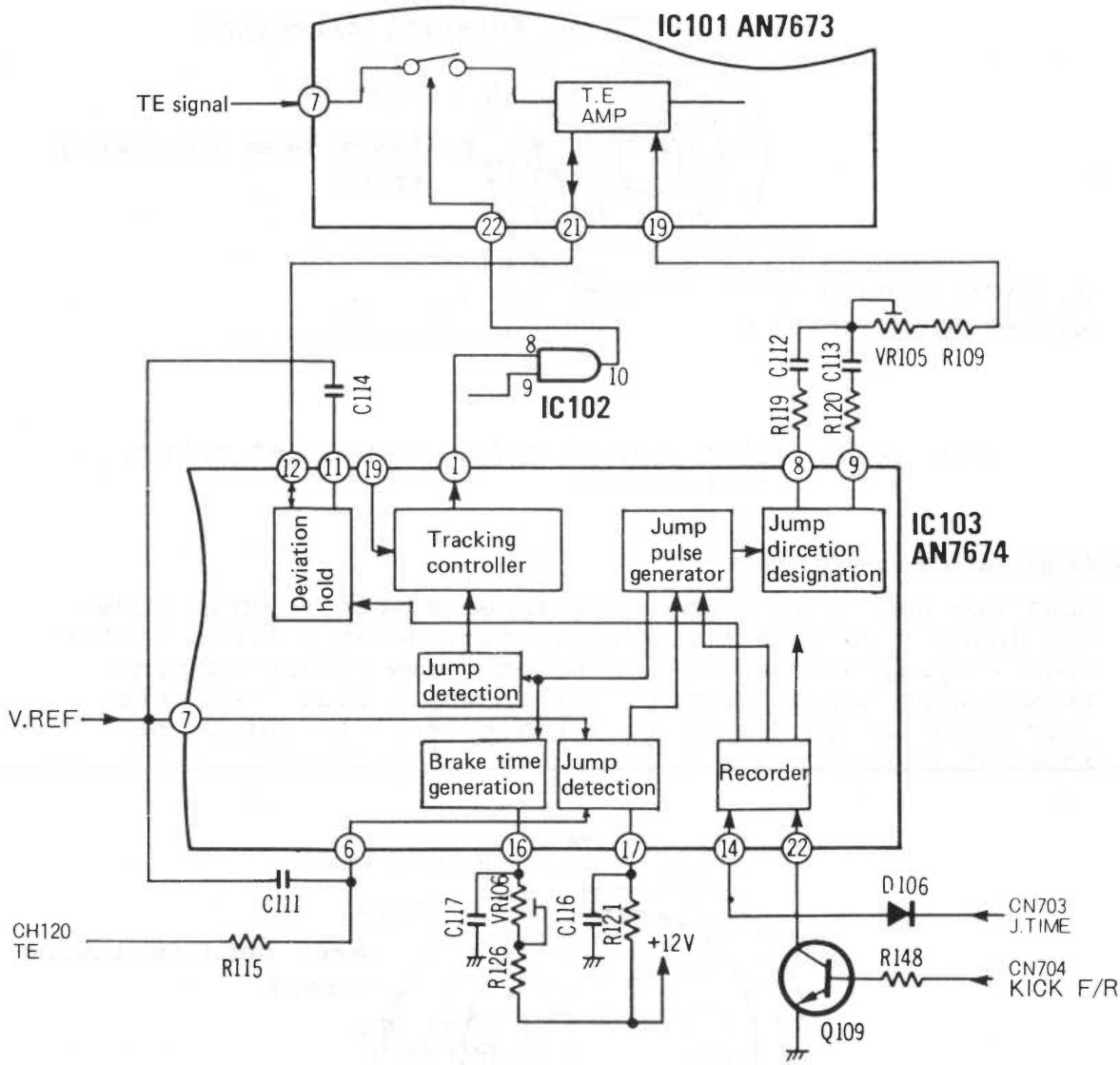


Fig. 4–22. Track jump control circuit

4—11. Back jump control circuit operation

(1) With CN704 (KICK F/R) at "L", J. TIME command is given to IC103 pin (14) from system microcomputer at the minimum deviation point of disc, then the jump pulse of IC103 pin (8) changes from "L" to "H" and simultaneously TR ON signal at IC103 pin (1) changes to "L" causing tracking servo to be released. (Jump start point)

*Jump pulse delivered to IC103 pin (8) is differentiated by C112 and is applied to the tracking error amplifier of AN7673 pin (19) . Then, the focus lens start to jump toward the inner periphery of the disc.

(2) On start of jump in step (1), C116 of IC103 pin (17) starts to be charged by R121, causing IC103 pin (17) to go "H". (Track skip detection start point)

(3) As the focus lens moves to the middle point between tracks due to the jump pulse while IC103 pin (17) is at "H", TE(HK) signal from IC103 intersects with V REF (reference voltage). As a result, the jump pulse of IC103 pin (8) changes from "H" to "L", and simultaneously C117 of IC103 pin (16) starts to be charged by R126 and VR106. (Track middle point, brake start point)

*When jump pulse of IC103 pin (8) changes from "H" to "L" ("L" → "H" in forward jump mode), the pulse applied to AN7673 pin (19) is opposite to that of step (1) . This pulse becomes the brake signal for jump function.

(4) When C117 of step (3) is charged causing IC103 pin (16) to go "H", TR ON signal of IC103 pin (1) changes to "H" on releasing of brake, and then tracking servo is activated. (Jump completion point)

4—12. Ford jump control circuit operation

(1) With CN704 (KICK F/R) at "H", J. TIME command is applied to IC103 pin (14) from system microcomputer at the minimum deviation point of disc, then jump pulse of IC103 pin (9) changes from "H" to "L" and simultaneously TR ON signal of IC103 pin (1) changes to "L" causing tracking servo to be released. (Jump start point)

* Jump pulse delivers to IC103 pin (9) is applied to the tracking error amplifier of AN7673 pin (19). Then, the focus lens starts to jump toward the inner periphery of the disc.

(2)
(3) — Same as for back jump control operation.
(4)

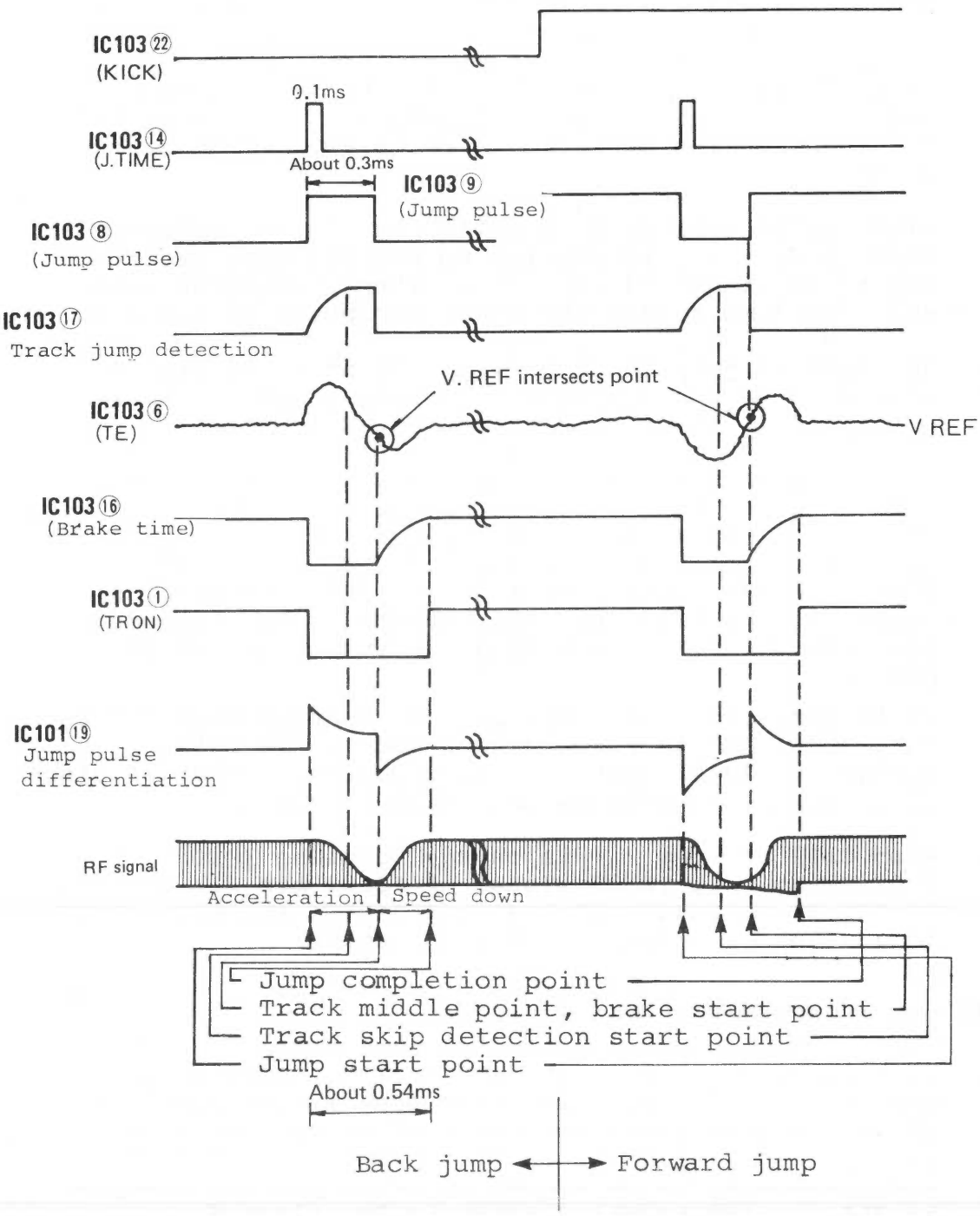


Fig. 4–23. Jump control timing

5. Traverse servo circuit

5–1. Function of traverse servo

Traverse servo functions to move the whole of optical PU from inner to outer and outer to inner periphery.

The tracking servo moves the object lens in the direction of tracking to follow the track, while the travese servo covers the radius of disc.

That is, tracking servo operates on the extended line of tracking servo, and moves the traverse base (whole of optical PU) when the lens is inclined by a specific angle. Thus, the lens always follows the track of disc within the range of tracking servo.

5–2. Configuration of traverse servo

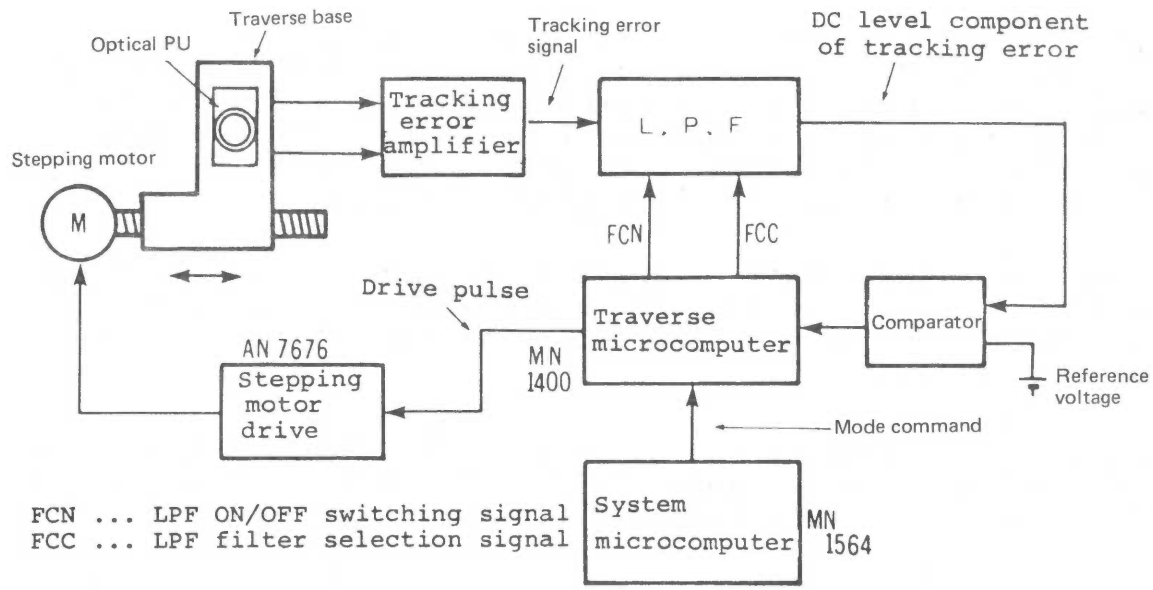


Fig. 5-1 Block diagram of traverse servo

The block diagram of traverse servo is shown in Fig. 5-1.

Traverse microcomputer (MN1400) generates drive pulses to rotate the stepping motor at the desired speed and in the desired direction, receiving the traverse mode commands signal from system microcomputer (MN1564).

There are 14 traverse modes to be set (refer to OP controller on page 132), and they can be roughly divided into the following two types of operation.

One of them is forcible control of stepping motor rotation, and the other is step by step rotation according to the quantity of tracking error. The former includes high-speed FWD and REV as typical modes, and the latter, PLAY and manual search low-speed mode.

Of those mentioned above, the latter is the function of traverse servo.

L.P.F. works to take out PC component from tracking error signal. In CD, the disc rotation at the inner periphery is different from that at the outer periphery (refer to CLV servo on page 60), and so is error period (AC component) per rotation. The filter constant is changed so that the AC component can be effectively eliminated.

When the traverse base is forcibly driven, the operation of L.P.F. is stopped because the servo loop is unnecessary in this mode. The outputs are delivered from MN1400 as FCC and FCN signals.

Also, MN1400 delivers the control signal obtained by decoding the mode command signal from system microcomputer to the relative adjacent circuits. The detail is shown in Fig. 5-2.

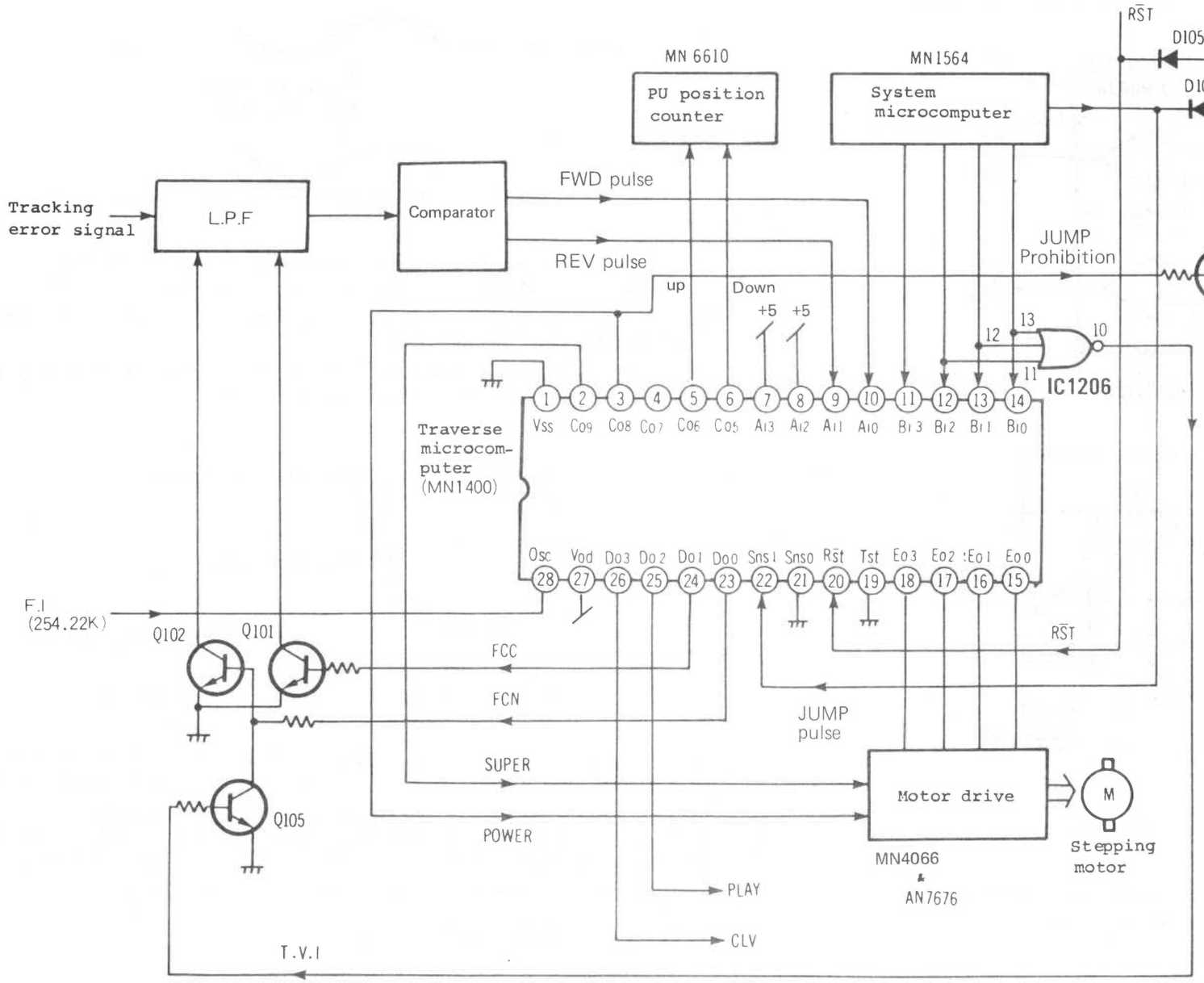


Fig. 5-2 Traverse microcomputer and adjacent circuit

[Functions of MN1400]

B10 - B13
° Traverse mode command signal input

E00 - E03
° Stepping motor drive pulse output

D00 & D01
° FCN & FCC control output of L.P.F.

A10 & A11
° 1-step FWD command pulse input

C05 & C06
° PU position counter clock input

C08
° Stepping motor electromotive force selection output
° Jump inhibit control output during traverse movement (related with SNSI)

C09
° Stepping motor drive pulse waveform change control output

D02
° PLAY mode (incl. manual search low speed) command output

D03
° Fine servo command output of CLV servo

5–3. Traverse servo circuit operation

- Tracking error signal circuit

The tracking error signal circuit is shown in Fig. 5-3.

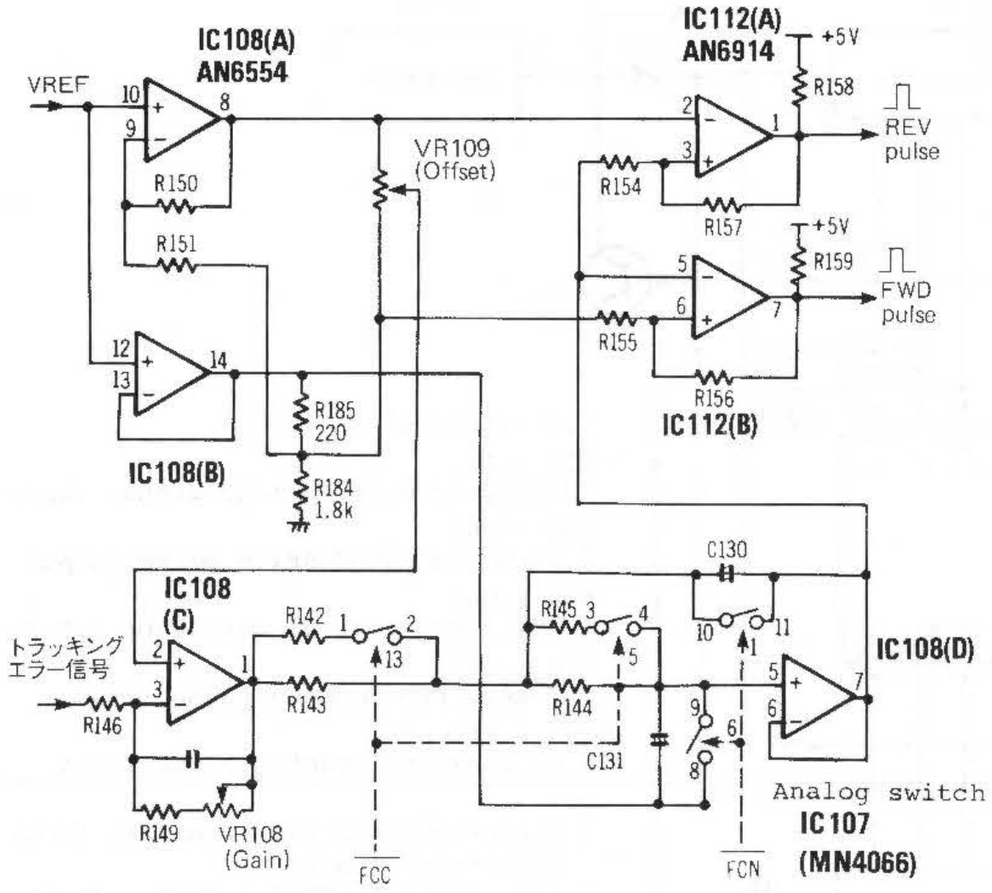


Fig. 5-3 Tracking error signal circuit

The circuit shows the tracking error signal L.P.F., comparator, and analog switch controlled by FCN and FCC signal.

Tracking error signal goes into IC108 through R146.

IC108(C) amplifies the tracking error signal and eliminates the high frequency by C132.

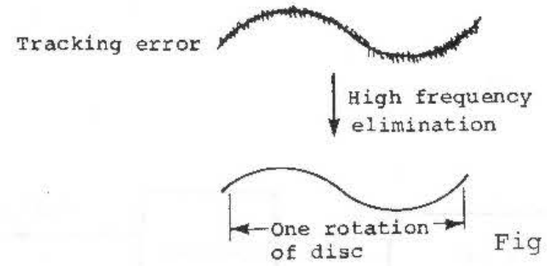


Fig. 5-4 Effects of C132

IC108(D) sets up an active type L.P.F. of 12 dB/ocf in combination with R142 - R145 and C130, C131.

The L.P.F. includes a filter constant changer using analog switch and ON/OFF switch.

The relationship between disc rotation and tracking error signal is explained in the following.

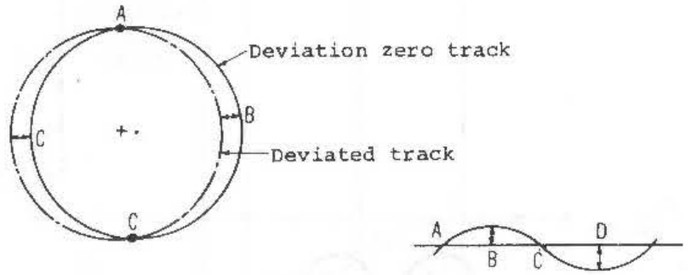


Fig. 5-5 Tracking error per rotation

In CD, the disc speed is about 200 r.p.m. at the inner periphery and about 500 r.p.m. at the outer periphery.

On the other hand, tracking error is the deviation of disc, and error signal of one period per rotation can be obtained when the tracking servo is activated. (See Fig. 5-5.)

Accordingly, when the disc speed is 200 r.p.m.

$$fTE = \frac{200 \text{ r.p.m.}}{60S} \fallingdotseq 3.3 \text{ Hz}$$

When the speed is 500 r.p.m., error signal of 8.3 Hz can be obtained.

The comparator mentioned later requires DC voltage with these components eliminated, and therefore the cut-off frequency of filter is set at 0.5 Hz and 1 Hz respectively at the inner and outer peripheries: The level of FCC signal at analog switch pins (13) and (5) is "H" at inner periphery and "L" at outer periphery.

IC108 (A) (B) make the positive and negative reference voltage of comparator with V REF voltage (≒ 6 V).

The devided voltage of R185 and R184 is about 0.6 V. Therefore, the reference voltage of comparator is (V REF + 0.6 V) on IC112 (A) side and (V REF - 0.6 V) on IC112 (B) side.

The comparison voltage is DC voltage in accordance with the quantity of tracking error taken out of L.P.F.

The relationship between servo gain and tracking error signal is explained in the following.

The principle of servo is shown in Fig. 5-6.

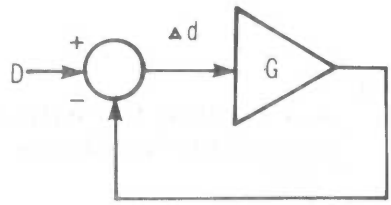


Fig. 5-6 Principle of servo function

D stands for the amount of deviation and Δd for servo accuracy, that is, the follow-up error. G stands for servo gain. When G is a limited value, servo is unable to make D completely "0", allowing some error to be included.

In Fig. 5-6, error voltage Δd can be obtained as follows:

$$\Delta d = \frac{D}{1 + G} \fallingdotseq \frac{D}{G}$$

In the case of actual CD, as the lens is gradually inclined, starting to follow the track from the neutral point, then error voltage that depends upon servo gain is accumulated on tracking error signal. It is indicated in Fig. 5-7.

L.P.F. eliminates undulation generated per disc rotation in the illustration, and therefore the output signal of L.P.F. is complete DC voltage.

The operation illustrated in Fig. 5-7 is in the FWD direction. In the case of REV deviation, error voltage is generated as shown by broken lines.

One-step feed of traverse base is 15° in rotation angle of stepping motor and 62.5 μW in distance on disc. This

corresponds to about 40 tracks. Therefore, the gain of amplifier for tracking error signal, that is, the traverse gain set by VR108 is adjusted so that voltage of 0.6 - 0.8 V can be obtained when deviation equivalent to 40 tracks is generaged in the output of L.P.F. IC112 (AN6914) is an open collector type comparator that compares the DC voltage of L.P.F. output with the reference voltage from IC108 (A), (B), and delivers 1-step feed command pulse to MN1400 in FWD and REV directions.

Since tracking error signal is inverted by IC108 (C), the comparison voltage in the case of L.P.F. output gradually drops in FWD direction.

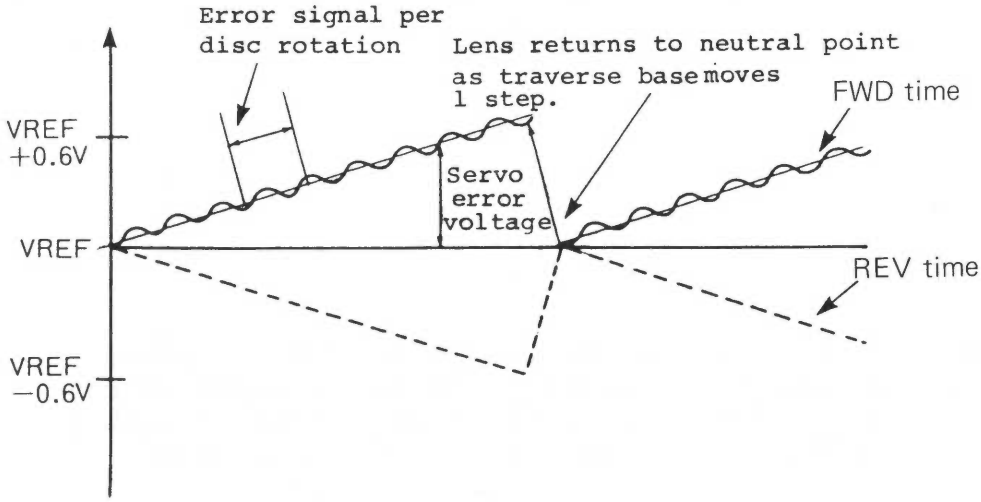


Fig. 5-7 Error voltage of tracking error signal

- Stepping motor circuit

The 4-phase pulse from MN1400 causes current to flow into the stator coil of stepping motor, thereby generating magnetic field of rotation. An actual stepping motor uses 12-pole 24 slots, but the operation is here explained with 4-pole 8 slots.

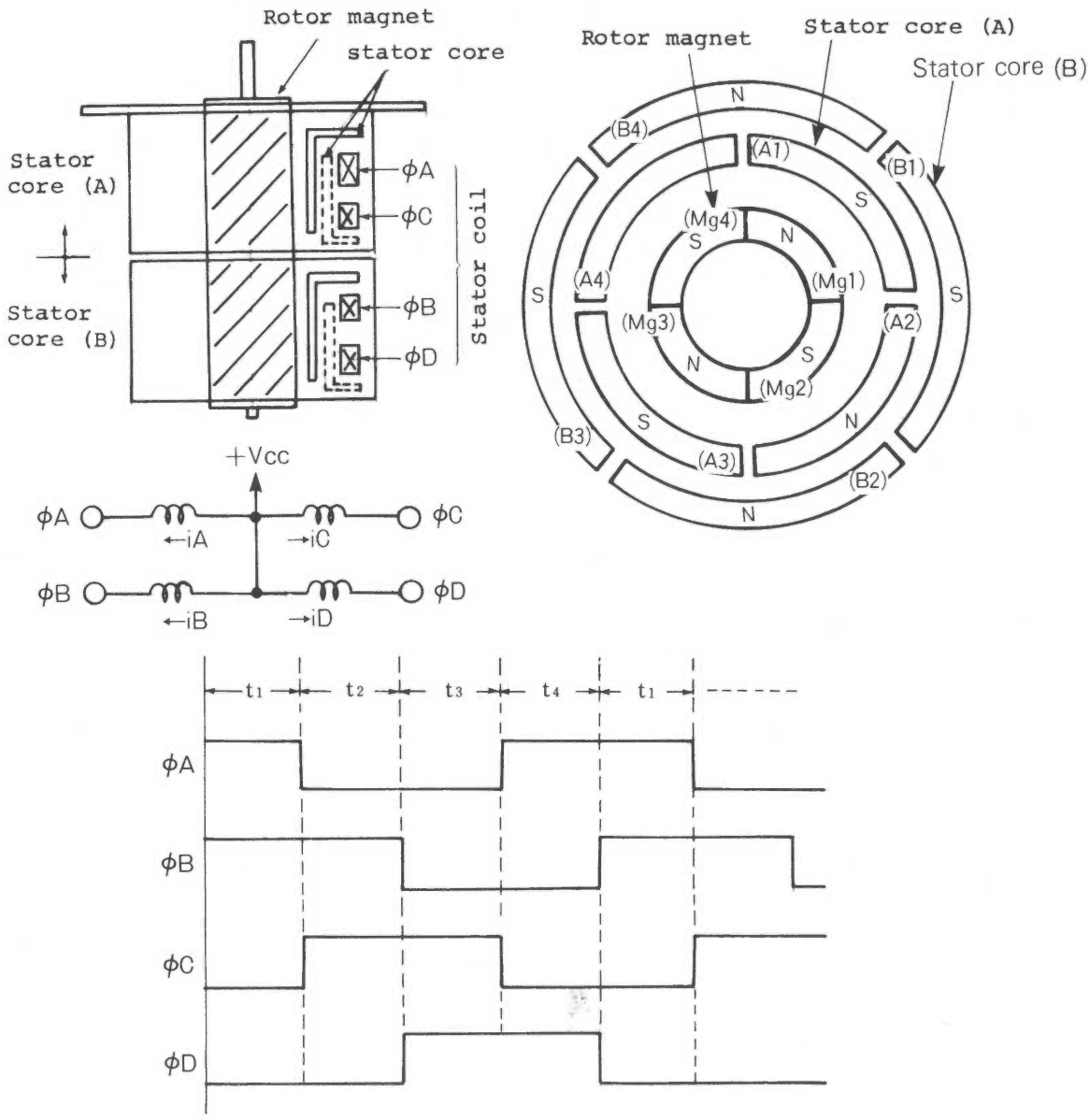


Fig. 5-8 Stepping motor and its drive pulse

Suppose that the rotor magnet and stator core are as shown in Fig. 5-8.

Then in t1 timing of 4-phase pulse, exciting current "ic" and "iD" flows into stator coils øC and øD. Suppose that stator coils (A1) and (B1) are excited in S pole due to iC and iD, then the rotor magnet rotates 45° clockwise.

Next, iD and iA flow in t2 timing. S pole remains at (B1) due to iD, but N pole is excited at (A1) due to iA.

In other words, S pole is excited at (A2). Accordingly, the rotor magnet rotates 45° clockwise in t2 timing. Current iA and iB flow in t3 timing.

S pole remains at (A2) due to iA, and S pole is excited at (B2) due to iB, and further the rotor magnet rotates 45° in the same direction. (In this timing, Mg1 comes to the position of Mg2.)

Similarly, the rotor magnet rotates 45° in t4 timing, and after that, it repeats rotating 45° each time the drive pulse changes, and the motor makes one turn in 8 steps.

Since an actual stepping motor is 12-pole 24 slots, the rotation angle per step is 15°. The stepping motor circuit and EO port output waveform of MN1400 are shown in Fig. 5-9.

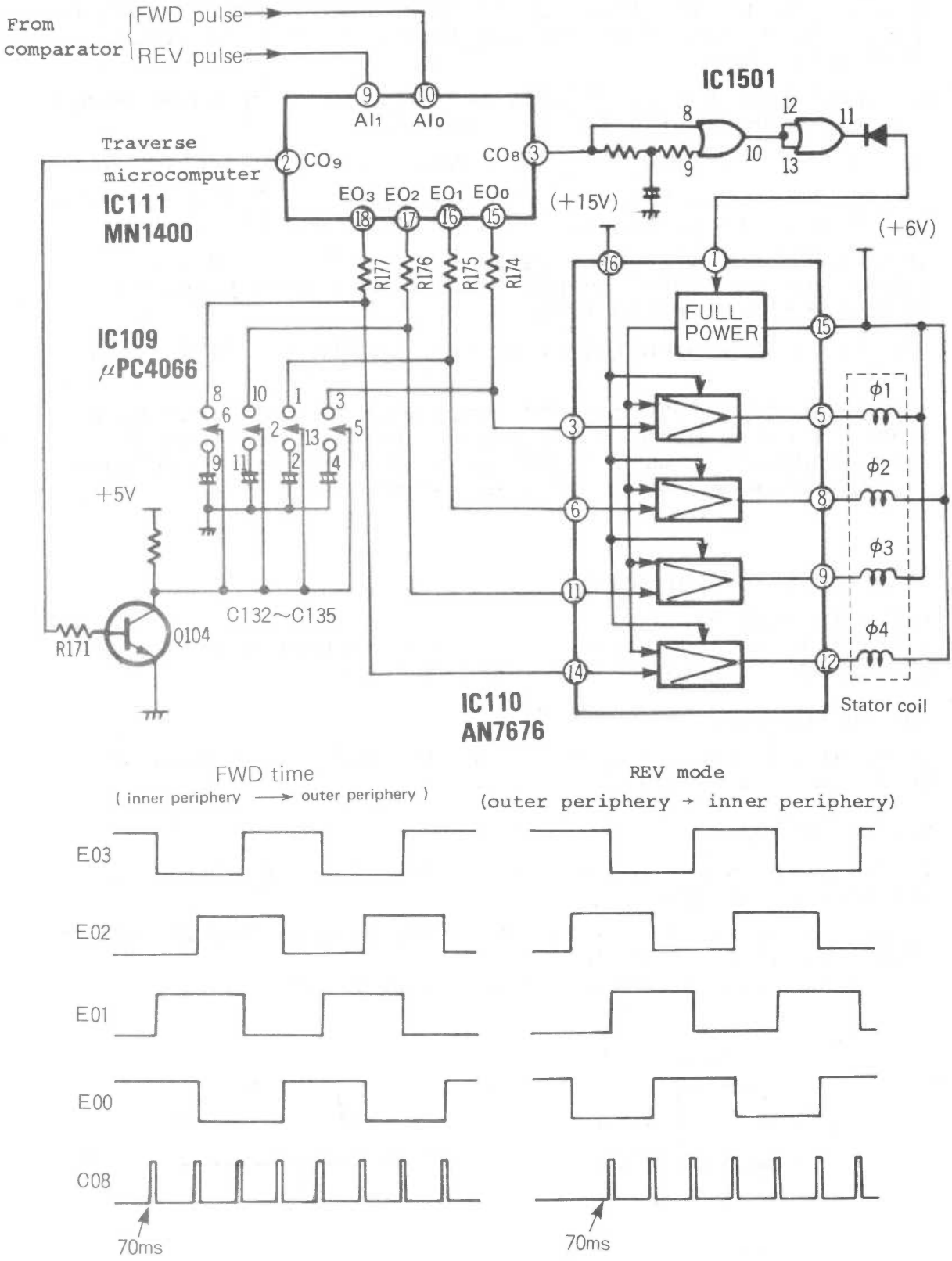


Fig. 5-9 Stepping motor circuit

IC110 (AN7676) is a stepping motor drive IC. The 4-phase pulse waveforms from traverse microcomputer (MN1400) during FWD and REV modes of stepping motor are as shown in Fig. 5-9, so that the rotating magnetic field of stator core is reversed.

.At input terminal of AN7676, the 4-phase drive pulse waveform is made trapezoidal by C132 - C135.

(Q104 is OFF during PLAY and manual search low-speed mode.)

During FWD mode, drive pulse changes as 9 → 3 → 6 → C → 9 ... in HEX indication with E03 as MSB, and E00 as LSB.

During REV mode, it changes as 9 → C → 6 → 3 → 9 ... MN1400 pin (3) (C08) output makes AN7676 full power to increase the starting torque.

Therefore, the stepping motor repeats Start → Hold operation.

Also, pin (2) (C09) goes "H" only when the traverse mode moves at extra-high speed, and changes the drive pulse from trapezoidal wave to rectangular wave thereby releasing the slow up motion of stepping motor.

° Other functions of MN1400

Refer to Fig. 5-2.
Pin (5) (C06) and pin (6) (C05) generates negative pulses in timing of starting the stepping motor.

During FWD mode ...

It delivers output pulses to pin (6) (C05) in timing of MN1400 pin (3) (C08).

During REV mode ...

It delivers output pulses to pin (5) (C06) in timing of MN1400 pin (3) (C08).

These pulses become the clock for counter in MN6610 respectively as SNSA and SNSB.
(For operation of MN6610, refer to page 118.)

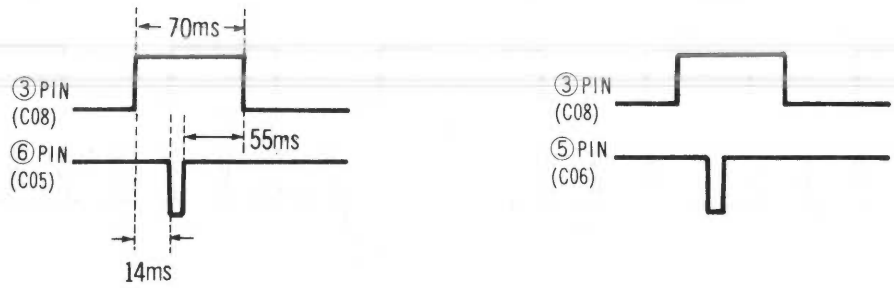


Fig. 5-10 PU position counter clock

Pin (26) (D03) goes "H" only when the set is in PLAY mode, and then fine servo is selected in CLV servo circuit. (For CLV servo, refer to page 66.)

Pin (25) (D02) goes "H" only when the set is in PLAY and manual search low-speed modes.

Pin (3) (C08) and pin (22) (SNSA) operate in relation with each other.

Q103 operates so that jump signal will not be applied to IC103 (AN7674) in traverse start timing even when system microcomputer delivers jump pulse output to IC103.

Finally, the function of IC1206 gate circuit is explained although it is not directly related with the function of MN1400.

The mode command signal from system microcomputer is applied to B10, B11, and B12 and "L" during stop and pause modes.

IC1206 operates receiving these signals as input. Therefore, the gate output in the above-mentioned mode is at "H" and plays the same role as FCN signal.

The explanations given so far are mainly for PLAY mode, and the functions of MN1400 in other traverse modes are shown in Table 5-1.

Traverse microcomputer IN/OUT port / Set mode		B port input: Input terminal from system microcomputer (MN1564PCE)				D port output: CLV	D port output: RF ON/OFF	D port output: Low pass filter ON/kHz	D port output: Low pass filter ON/OFF	C port output: SENS A Traverse move distance sensor output (forward)	C port output: SENS B Traverse move distance sensor output (reverse)	C port output: Motor full power control output	C port output: Trapezoidal wave control output	E port output: Stepping motor rotation control output			
		⑪	⑫	⑬	⑭	㉖	㉕	㉔	㉓	⑥	⑤	③	②	⑱	⑰	⑯	⑮
		BI3	BI2	BI1	BI0	D03	D02	D01	D00	C05	C06	C08	C09	E03	E02	E01	E00
STOP		0	0	0	0	0	0	1	1	1	1	0	0	Previous value hold			
PLAY	(Inner periphery)	0	0	0	1	1	1	0	1	When A port input is 1101, ⊓ pulse; When A port input is 1100, 1110, 1111 } 1	When A port input is 1110, ⊓ pulse; When A port input is 1100, 1101, 1111 } 1	C05 or C06 is: 14ms, 55ms, 70ms	0	It changes syncronizing with ⊓ of C05: 9, C Forward 3, 6, FWD		It changes synchronizing with ⊓ of C06: 9, C Reverse 3, 6, REV	
PLAY	(Outer periphery)	0	0	1	0	1	1	1	1								
Manual search	Low-speed (内周)	0	0	1	1	0	1	0	1	Same as { PLAY–1, PLAY–2 }	Same as { PLAY–1, PLAY–2 }	Same as { PLAY–1, PLAY–2 }	0	Same as { PLAY–1, PLAY–2 }			
	Low-speed FWD (outer)	0	1	0	0	0	1	1	1								
Low-speed FWD		0	1	0	1	0	0	1	0	← 550ms →	1	C05 is: 14ms, 55ms	0	It changes synchronizing with ⊓ of C05: 9, C Forward 3, 6, FWD			
Manual search high-speed FWD		0	1	1	0	0	0	1	0	← 16ms →	1	1	0				
Extra-high speed FWD		0	1	1	1	0	0	1	0	← 5 mS →	1	1	1				
PAUSE		1	0	0	0	0	1	1	1	1	1	0	0	Previous value hold			
Manual search	Low-speed REV (inner)	1	0	1	1	0	1	0	1	Same as { PLAY-1, PLAY-2 }	Same as { PLAY–1, PLAY–2 }	Same as { PLAY–1, PLAY–2 }	0	Same as { PLAY–1, PLAY–2 }			
	Low-speed REV (outer)	1	1	0	0	0	1	1	1								
Low-speed REV		1	1	0	1	0	0	1	0	1	← 550ms →	C06 is	0	It changes syncronizing with ⊓ of C06: 9, C Reverse 3, 6, REV			
Manual search high-speed REV		1	1	1	0	0	0	1	0	1	← 16 ms →	1	0				
Extra-high speed REV		1	1	1	1	0	0	1	0	1	← 5 ms →	1	1				

Table 5-1 Operations of traverse microcomputer (MN1400PCA) according to system microcomputer commands

6. CLV servo circuit

6–1. Function of CLV servo

Unlike the constant speed CAV (constant-angular velocity) system of conventional analog player, the CLV (constant-linear-velocity) system is used for CD control in which recording sensitivity is constant in any position of the disc.

Therefore, the turntable speed varies according to the playback track position. The recording speed of disc ranges from 1.2 m/s to 1.4 m/s in the specification. The CLV servo compares the reference clock frequency divided from X'tal with the synchronizing signal detected from the disc in order to control the rotational speed.

6–2. Construction of CLV servo

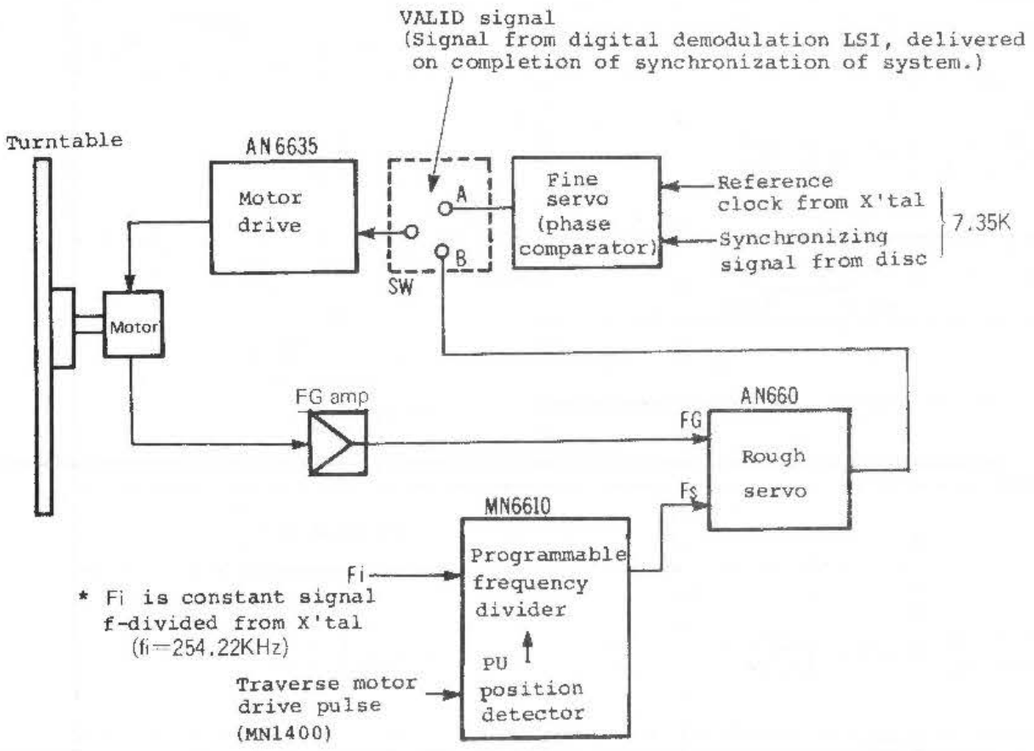


Fig. 6-1 Block diagram of CLV servo

The CLV servo of SL-P10 consists of Rough and Fine servo circuits, which can be selected by the switch shown in Fig. 6-1. (Fine servo ..... A; Rough servo ..... B)

The system follows Rough servo → Fine servo processes until complete synchronization.

Function of Rough servo

If the turntable speed is greatly different from the speed corresponding to the playback track position, the demodulation circuit is unable to detect the synchronizing signal from the disc, and then CLV servo cannot be set up.

Therefore, the rough servo is provided to control the speed so that the demodulation circuit is able to operate.

The rough servo is interlocked with the optical PU position (to count the drive pulses of traverse motor) to compare the varying reference signal fs and FG, thereby controlling the rotation.

* fs is the signal obtained by treating fi with programmable frequency divider, and it is the reference signal in rough servo circuit.
  The division ratio of programmable frequency divider is set according to the amount of traverse movement converted by MN6610.

Function of Fine servo

When the rotational speed is high enough for demodulation circuit operation, the selection switch is shifted from Rough to Fine servo by the VALID signal.

Fine servo compares the reference clock from X'tal with the synchronizing signal detected from the disc, thereby controlling the rotational speed. Therefore, if the linear speed is 1.25 m/s on the disc, then the signal is automatically played back at the linear speed of 1.25 m/s.

6–3. CLV servo circuit operation

The actual circuit of CLV servo is shown in Fig. 6-5.

- Spindle motor drive circuit

IC301 (AN6635) is the drive IC for spindle motor.
Pins (10) and (11) of this IC are the reference voltage and control voltage terminals for motor control.
In this unit, pin (11) is the reference voltage terminal that is adjusted to 6.3 V by VR301.
The control voltage of pin (10) is supplied through the analog switch of IC303 (MN4066B). Also, pin (9) of IC301 is ON/OFF terminal of IC and it is operated with open terminal (the inverter in the previous stage is open collector type) and its function stops at "L".

- Rough servo circuit

IC302 (AN660) is the control IC for rough servo.
The reference signal fs of rough servo is applied to pin (1) of this IC, and comparison signal FG is applied to pin (16) from pin (1) of IC312.
PT is equivalent to FG of spindle motor. The output of IC is speed control voltage at pin (8) and phase control voltage at pin (4), which are mixed by R309 and R312 before going into pin (6), and taken out of pin (7) as control voltage.

The control voltage is put into pin (1) of IC303 (MN4066B) to set up rough servo when pin (13) is at "H".

IC302 pin (13) is the reference voltage terminal of rough servo. The reference voltage is necessary to make a voltage in direct proportion to fs.

The circuit to meet the purpose is F-V change-over circuit consisting of IC309 (A), Q301, D202, 204. The F-V changeover circuit is shown in Fig. 6-2.

VR304 is used to adjust the time of one-shot multi IC309 (1/2) so that the voltage of IC302 pin (13) is about 5 V at 500 r.p.m. and about 2 V at 200 r.p.m.

VR303 is adjusted to 6 V to determine the synchronizing point of rough servo.

* The period of fs is longer on the outer periphery side.

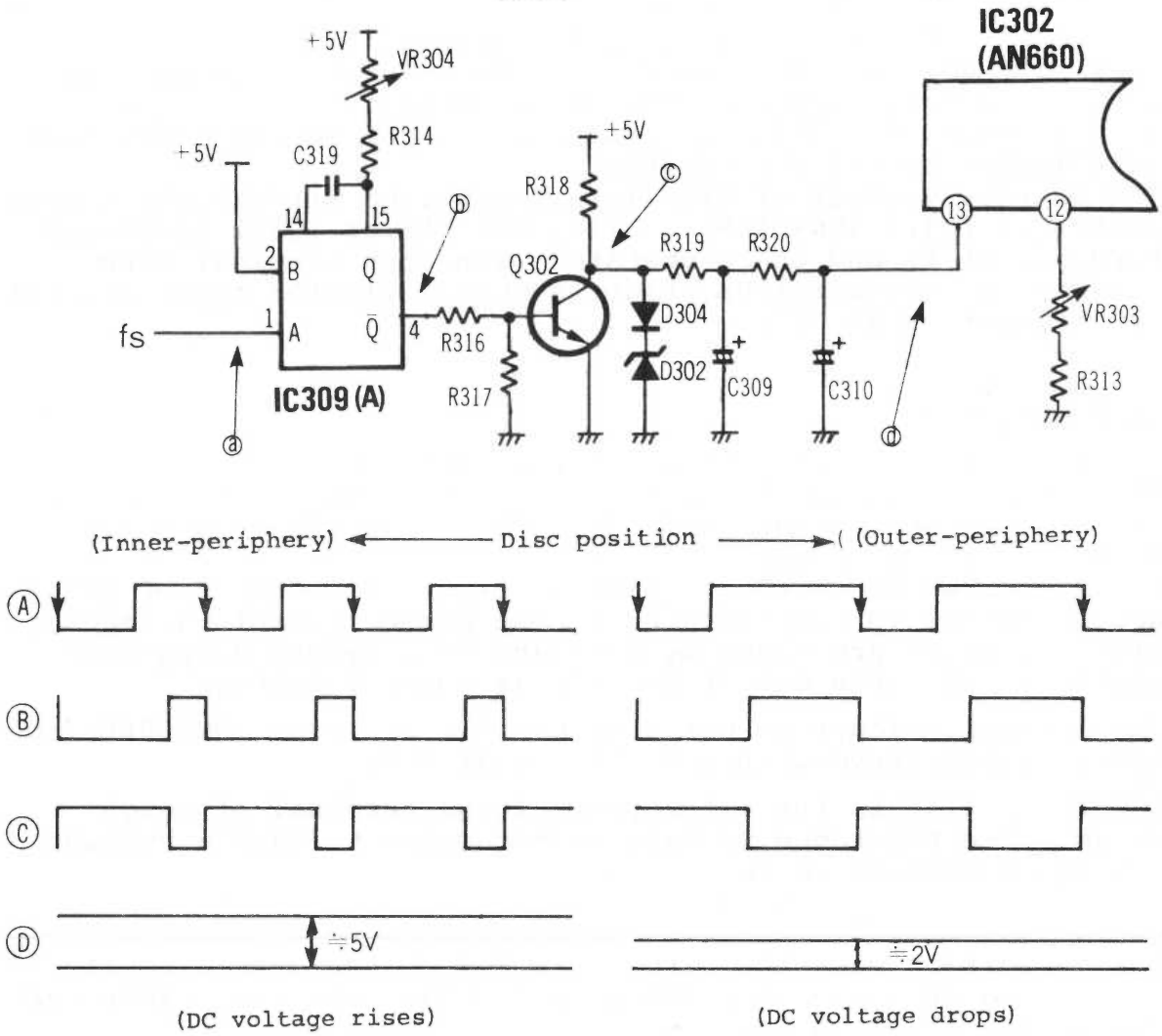


Fig. 6-2 Generation of rough servo reference voltage

- Fine servo

IC304 (TC5081) is the phase comparator for fine servo. During fine servo operation, the servo is activated with the 2 signals from demodulation LSI.

FCLK -------- Reference signal from X'tal through frequency division (7.35 K)

CLDCK ------- Comparison signal detected from disc (7.35 K)

The 2 signals enter IC304 pins (7) and (8) from which the error signal is delivered to pin (3).

The error signal is DC-converted at IC311 (AN6552) into control voltage and put into IC303 (MN4066B) pin (4), setting up fine servo when pin (5) is at "H".

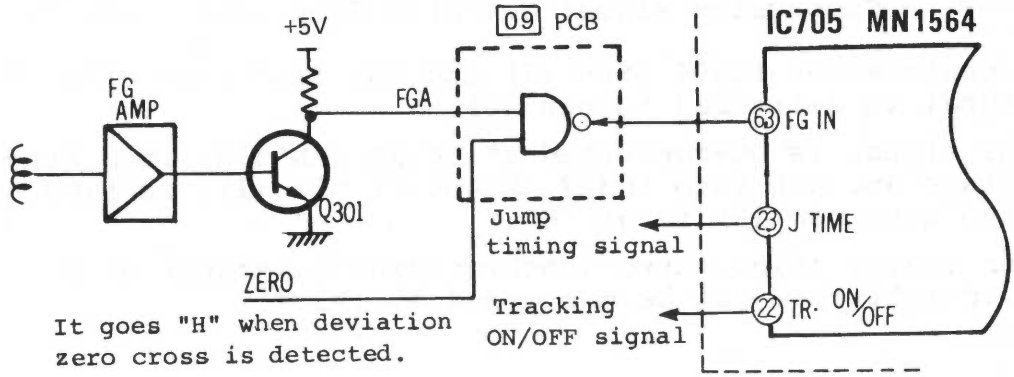
The error signal (fine servo synchronizing waveform) with fine servo activated can be monitored by TP307.

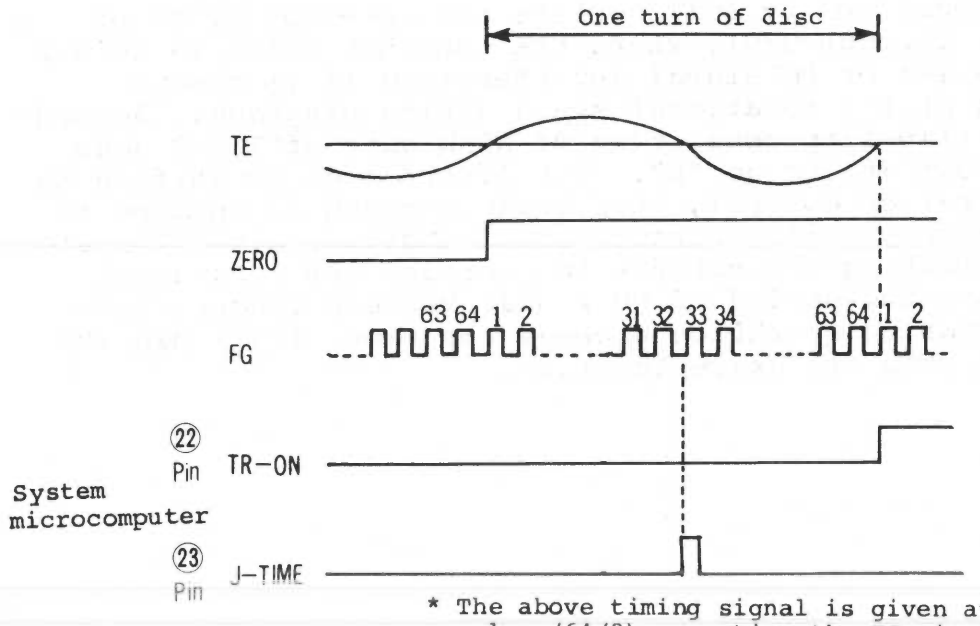
- FG circuit

IC312 (AN6552) is the FG signal amplifier.
FG signal is used for 3 purposes in the system.
The first is comparison signal for rough servo. IC302 pin (16) corresponds to this purpose. The second is spindle drive IC function stop.

FG signal amplified by IC312 enters the one-shot multi of IC309 (1/2) through Q301, where the one-shot pulse is longer than the period of FG signal and therefore it is always retriggered at the rotational speed during playback. Accordingly, the flip-flop consisting of NAND gate of IC308 does not cause pin (6) to go "L". But if the mode is shifted to stop in operation control, then brake command is applied to IC301 (AN6635) pin (10) through IC303 (MN4066) pins (10) and (11), thus braking the spindle to decrease the rotational speed. Then, the period of FG signal becomes longer, and when retriggering operation exceeds the time, IC301 pin (9) goes "L" to stop the drive function.

The last one is the signal taken out of Q301 collector as FGA. The signal finally goes into the system microcomputer. The system microcomputer counts the FG signal (64 pulses/turn) to determine the output timing of pins (22) and (23).





* The above timing signal is given at the 32nd pulse (64/2), counting the FG signal from deviation zero cross.

Fig. 6-3 Use of FG signal P49

• Servo selection circuit

The control voltage applied to pin (10) of IC301 (AN6635) can be changed over in 3 modes by analog switch IC303 (MN4066B).

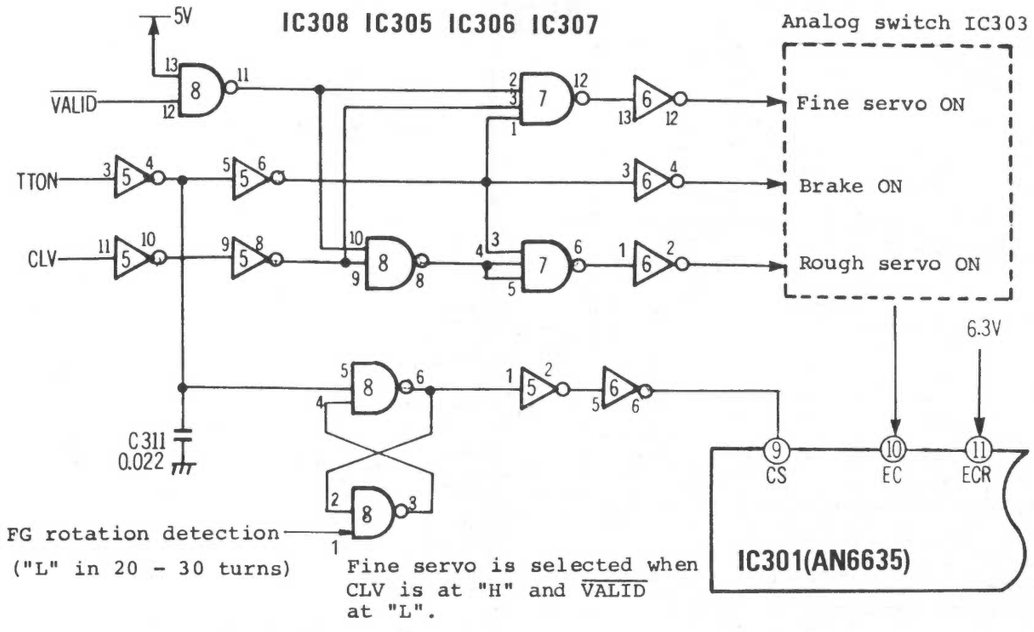


Fig. 6-4 Servo selection circuit

$\overline{\text{VALID}}$ ..... Output from demodulation LSI (MN6611). Effective when demodulation period completion signal is at "L".

TTON ..... Output from system microcomputer (MN1564). Effective when turntable rotation command signal is at "H".

CLV ..... Output from traverse microcomputer (MN1400). "H" only in PLAY mode.

Stop → Rough servo

CLV is at "H".

When TTON signal is at "H", IC306 pin (12) "L", IC306 pin (4) "L", IC306 pin (2) "H" and IC301 pin (9) "H", then the spindle motor rotates and the rough servo operates.

Rough servo → Fine servo

CLV is at "H".

When $\overline{\text{VALID}}$ signal changes from "H" to "L", then IC306 pin (12) "H" and IC306 pin (2) "L", and the fine servo operates. In this case, the system is shifted to PLAY mode.

PLAY to STOP

CLV is at "L".

When TTON signal is at "L", IC306 pin (4) goes "H", braking the spindle. [Pin (10) is lowered in EC.]

As the spindle is braked lowering the rotational speed, causing the FG period to become longer, then IC306 pin (9) goes "L" to stop the drive function of IC.

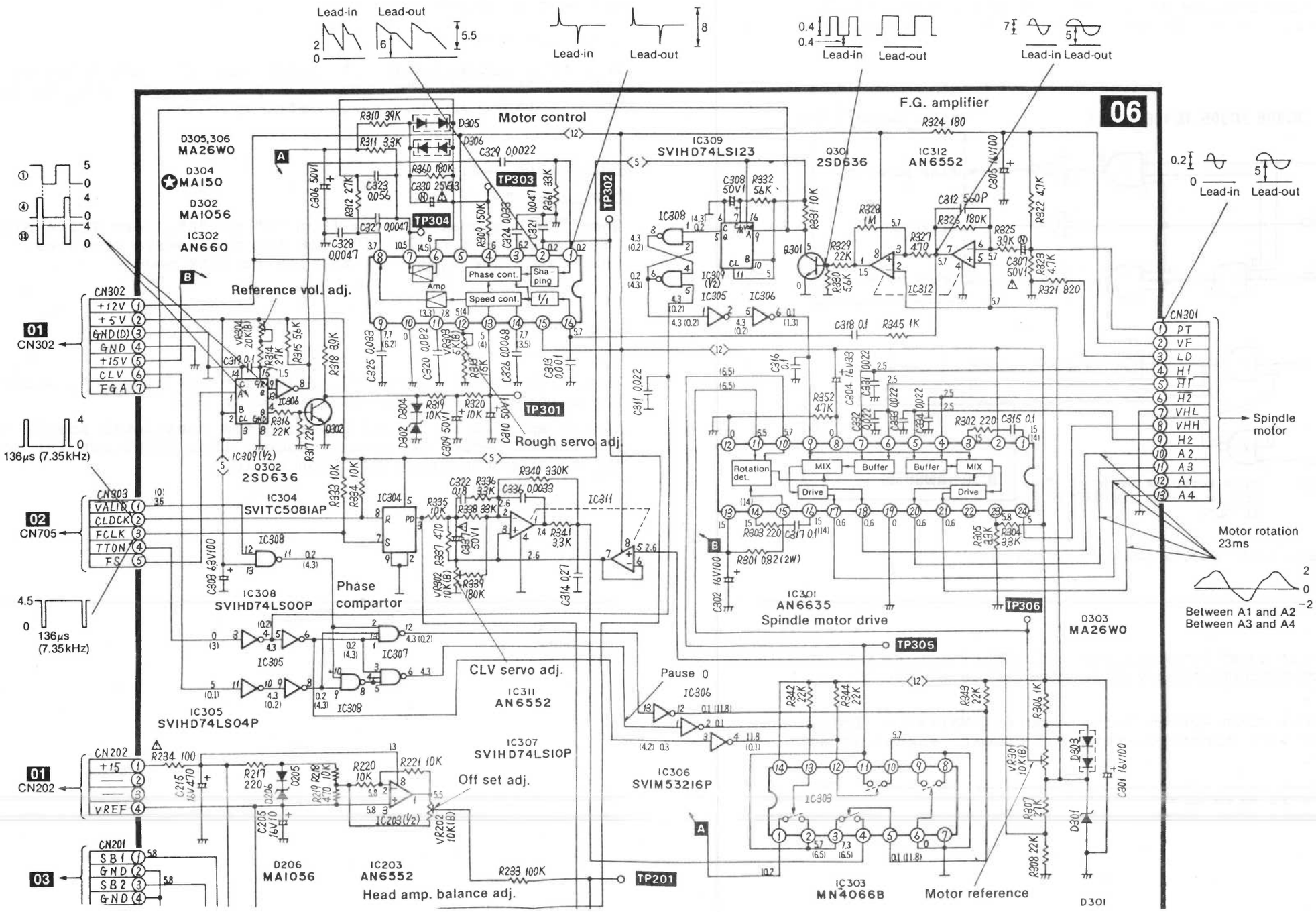


Fig. 6-5 Actual circuit of CLV servo.

7. RF data pick-out circuit

7–1. Roles of RF data pick-out circuit

This circuit is located in the middle of optical PU and digital processing circuit, and takes two different roles.

The first role is RF signal waveform shaping. The signal recorded on the disc is digital signal of 4.32 MHz bit rate, and the output waveform of optical PU obtained through reproduction is continuous analog signal as shown in Fig. 7-1. Therefore, it is necessary to shape the waveform into the form of digital signal. The second role is to generate PCK (clock signal). PCK is a bit rate signal synchronizing with the signal reproduced from the disc.

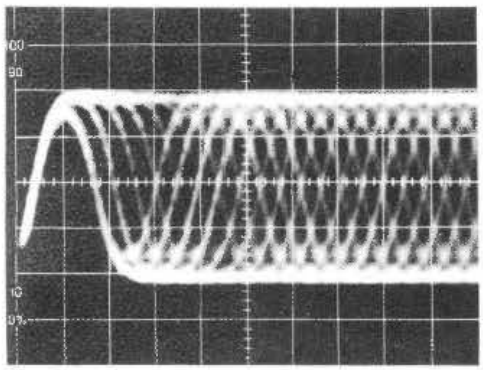


Fig. 7–1

The signal reproduced from the disc has some jitter until being stored into the memory. Therefore, clock signal synchronizing with the reproduced signal is required so that the digital processor is able to correctly receive the data. PCK is made by use of PLL circuit.

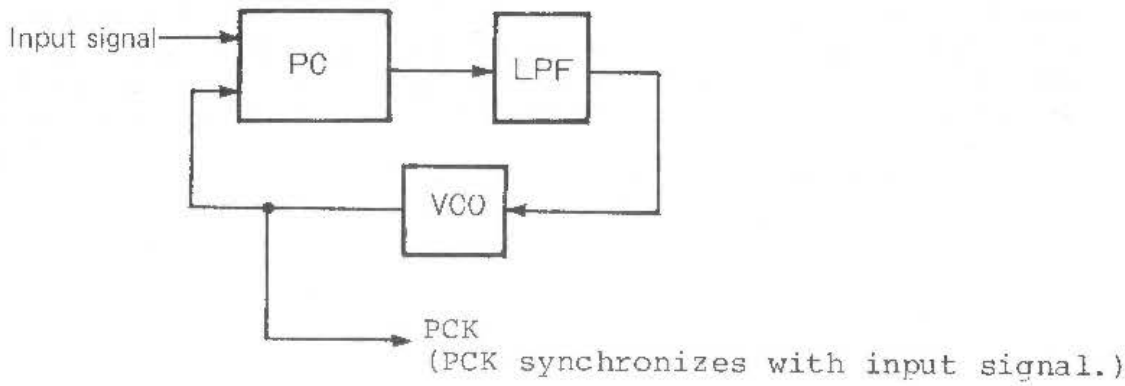
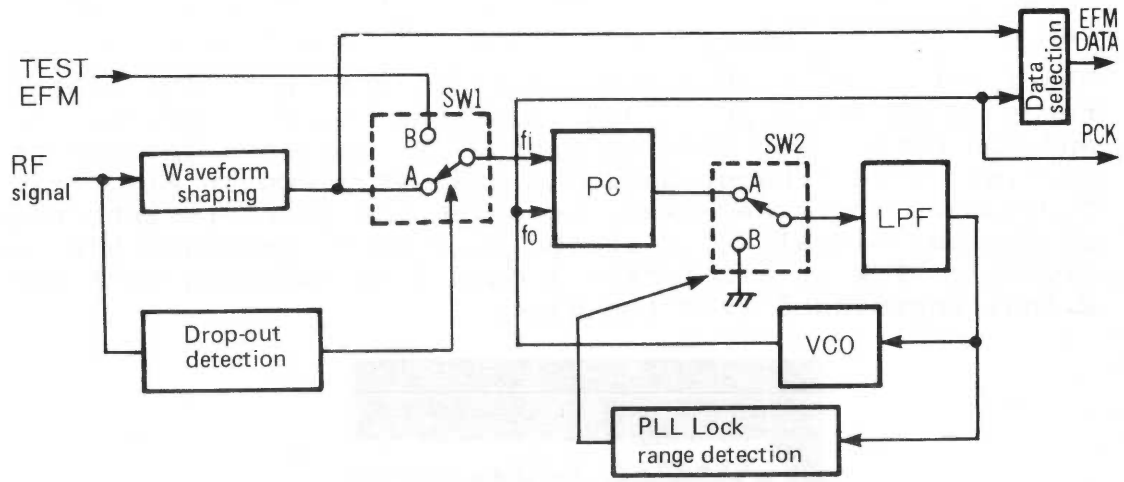


Fig. 7-2 PLL circuit

7–2. Configuration of RF data pick-out circuit



*SW1 ... Connected to B when drop-out is detected.
SW2 ... Connected to B when it is outside the PLL lock range.

Fig. 7-3 Block diagram of data pick-out circuit

The block diagram of data pick-out circuit is shown in Fig. 7-3. The RF signal from optical PU first enters the waveform shaping circuit.

Next, the signal passes through two SW circuits; both are connected to terminal A during normal playback; and the signal enters PC (phase comparator) of PLL circuit. The VCO free run of PLL is bit rate signal, and fi = fo when PLL is locked, therefore PCK synchronizes with the input signal.

PCK controlled by PLL is used to pick out data from RF signal whose waveform has been shaped. SW_1 temporarily holds PLL by switching the data so that PLL is not disturbed in case of drop-out. SW_2 shifts PLL to search mode for re-lock if PLL comes outside the lock range for some reason.

7–3. RF data pick-out circuit operation (I) .... 08 P.C.B. (only Domestic Model)

The optical circuit of RF data pick-out (I) is shown in Fig. 7–12

RF signal waveform shaping circuit

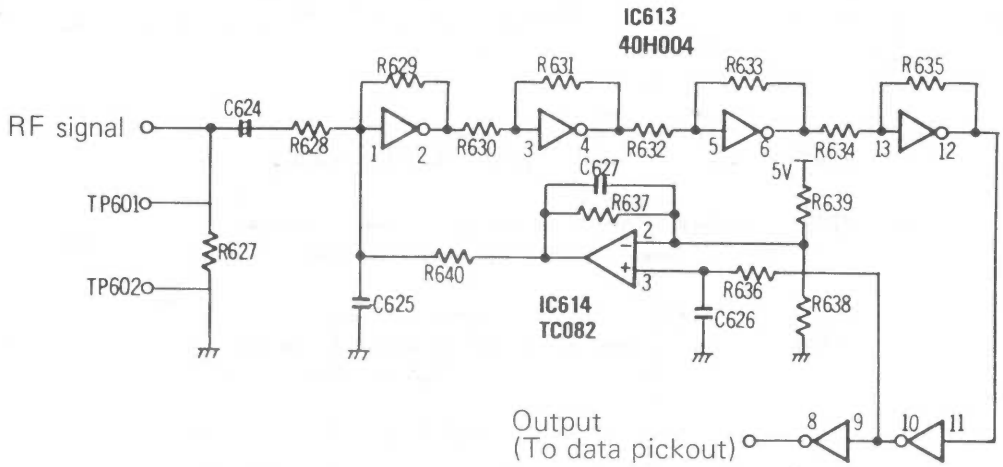


Fig. 7-4 RF signal waveform shaping circuit

PLL circuit (PCK generating circuit)

The PCK generating circuit is shown in Fig. 7-7. IC611 (74CS 157) is an IC equivalent to SW_1 shown in the block diagram. In normal playback mode, playback signal with waveform shaped at pin (11) (input A) is obtained at pin (9) (output). IC603 (A) (B) and IC604 (A) are the playback signal edge detection circuit, which takes out the edge at IC603 and its width is changed to 0.5T at IC604.

*1T is 4.32 MHz, and EFM data of playback signal is modulated at 3T - 11T.

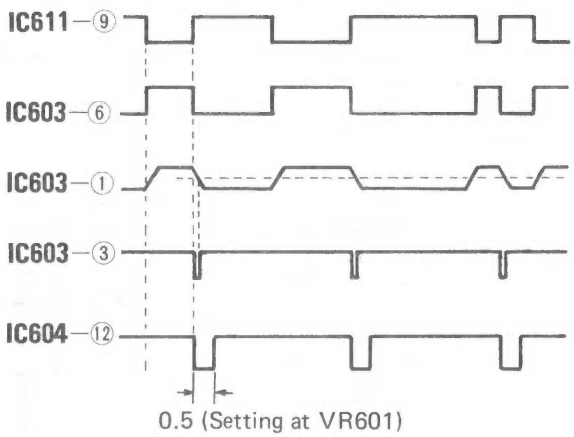


Fig. 7-5 Edge pulse generation

IC609 (74S124) is VOC of PLL, and the frequency of output pin (10) changes according to the DC voltage of pin (1) (FC input). The free-run frequency of VCO is about 17.28 MHz. This output is subjected to 1/4 frequency division at IC606, changing to PCK of about 4.32 MHz (= 1T).

IC605 (A) is PC (phase comparator) and are controlled by PCK (= 1T) and edge pulse (= 0.5T). It is illustrated in Fig. 7-6.

PLL is locked when the phase difference of PCK and 0.5T is 90°. (Area is equalized at ◌ mark.)

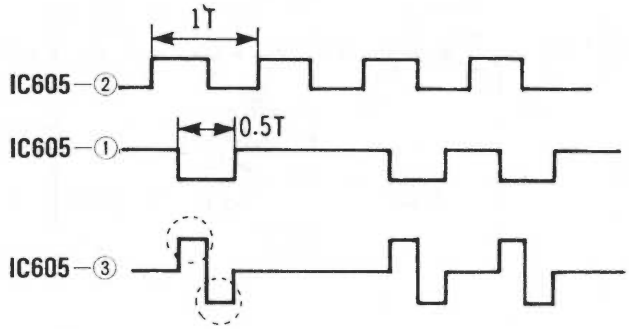


Fig. 7-6 Phase comparison

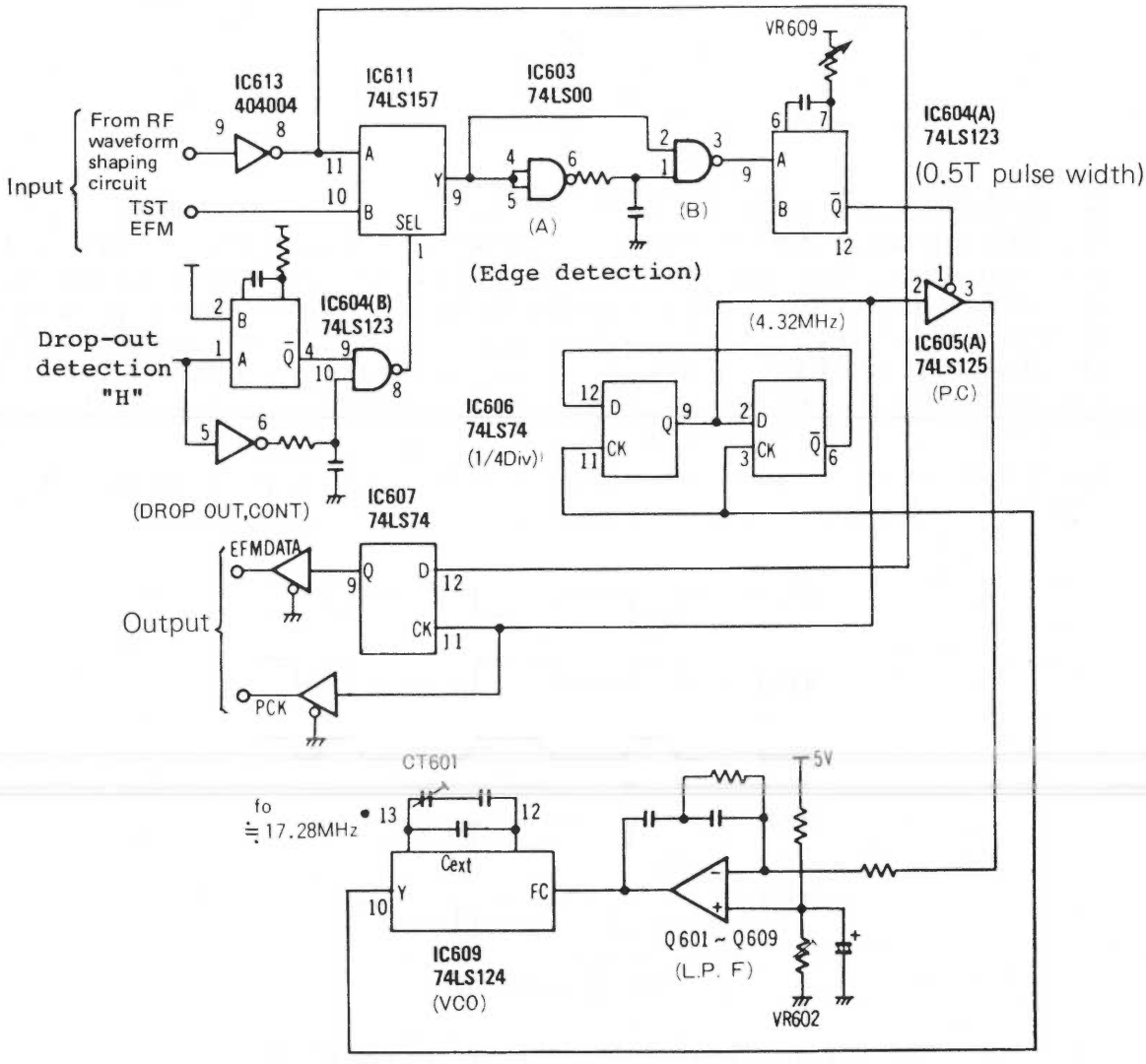


Fig. 7-7 PCK generating circuit

* For simplifying the circuitry, it is partially omitted or equivalent circuits are used.

Q601 - 604 set up LPF, which changes the output difference of PC into DC to control pin (1) (FC input) of VCD. LPF has 2 types of time constant which are selected by use of analog switch IC602 so that quick response is obtained for PLL in search mode and stable response in play mode.

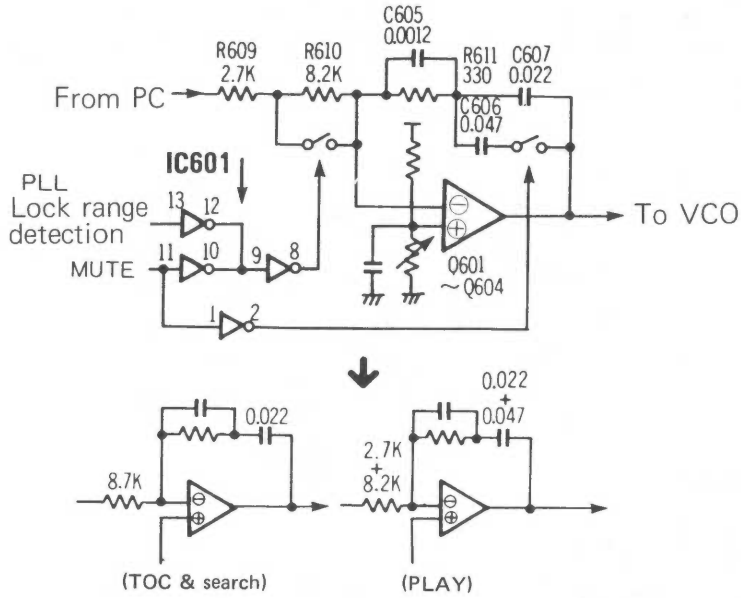


Fig. 7-8 LPF circuit

° MUTE

The muting signal is identical with the audio muting signal at "H" delivered from system microcomputer.

° PLL lock range detection

Output level is "H" in search mode when PLL is outside the lock range. It is "L" in lock mode.

PLL lock range detection circuit

The PLL lock range detection circuit is shown in Fig. 7-10.

IC608 (TC810) is a comparator which controls the input voltage of VCO.

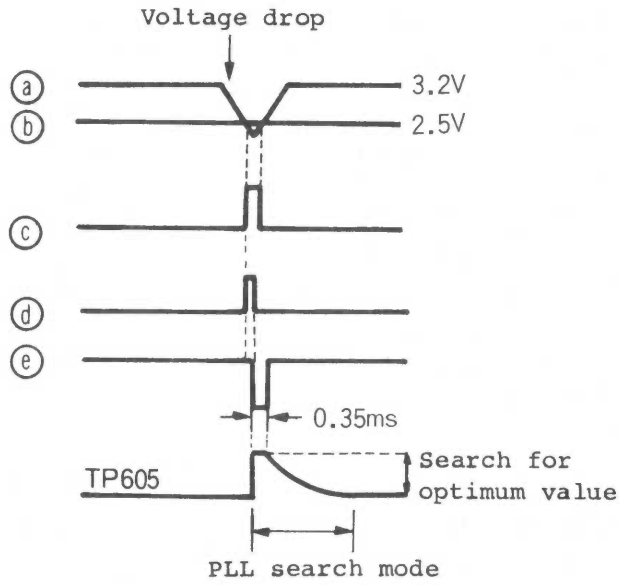


Fig. 7-9 PLL search

In normal playback mode, the input of IC608 is in the relation of (-) > (+), and IC610 pin 4 ($\overline{Q}$) is at "H", and IC605 (A) is performing phase comparison.

If the input voltage of VCO drops for some reason, causing the input of IC608 to (+) > (-), then IC605 (B) operates for the time [0.35 ms at pin (4)] set by IC610, therefore, the voltage of TP605 rises; as (+5 V) IC605 (B) is released, the voltage will gradually lower. Thus, when the optimum value is detected, PLL is locked again.

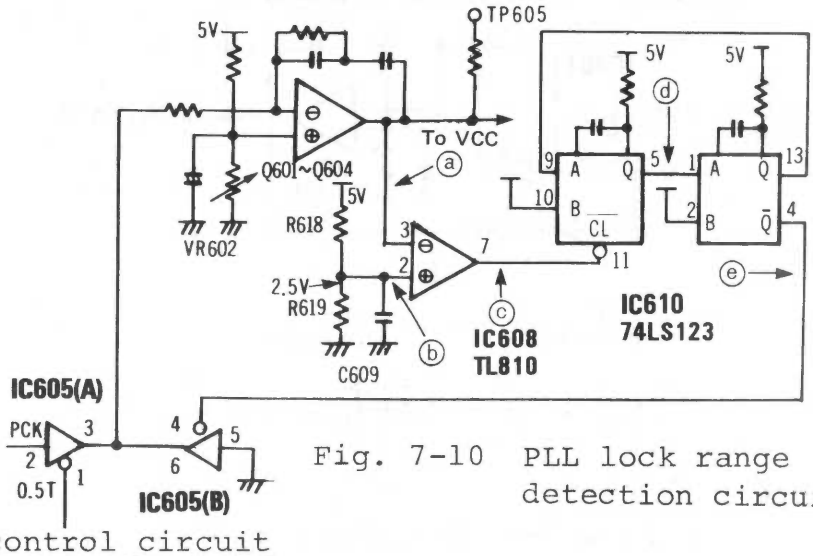


Fig. 7-10 PLL lock range detection circuit

Drop-out control circuit

Drop-out control circuit is shown in Fig. 7-11. IC611 (74LS 157) works for drop-out control. IC pin (1) (SEL terminal) delivers input B [pin (10)] when at "H" and input A [pin (11)] when at "L" to Y terminal [pin (9)].

If RF signal is missing due to drop-out, then 0.5T edge cannot be detected at PLL does not operate.

Accordingly, in case of drop-out, the input is shifted to T·EFM signal by the drop-out detection signal (refer to the section of Drop-out detection circuit on page 68.)

T·EFM signal is pure electrical EFM data made by demodulation LSI.

That is, during drop-out, PCK is properly controlled through substitution with T·EFM, while the correcting circuit of demodulation LSI will take care of data missing.

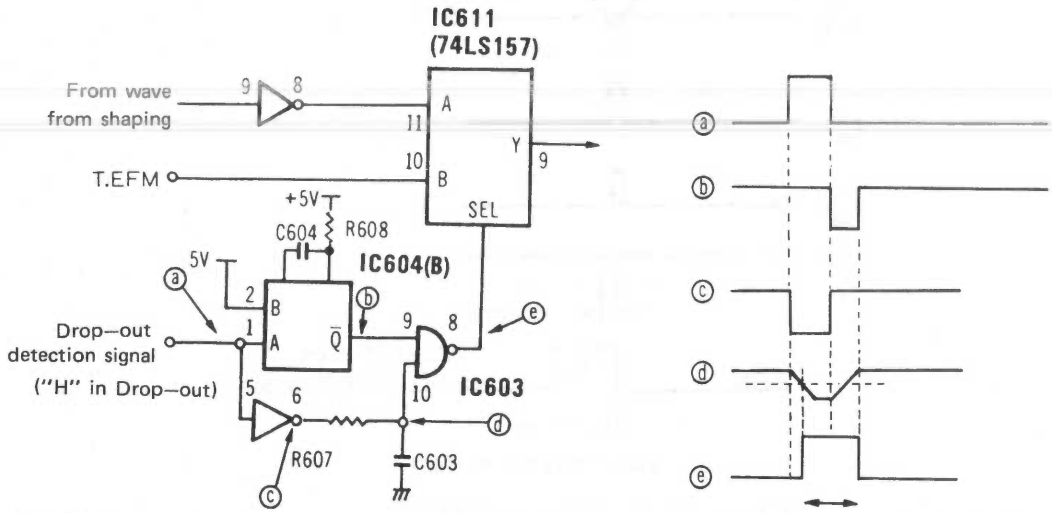


Fig. 7-11 Drop out control circuit T·EFM is applied during this range.

RF data pick-out circuit

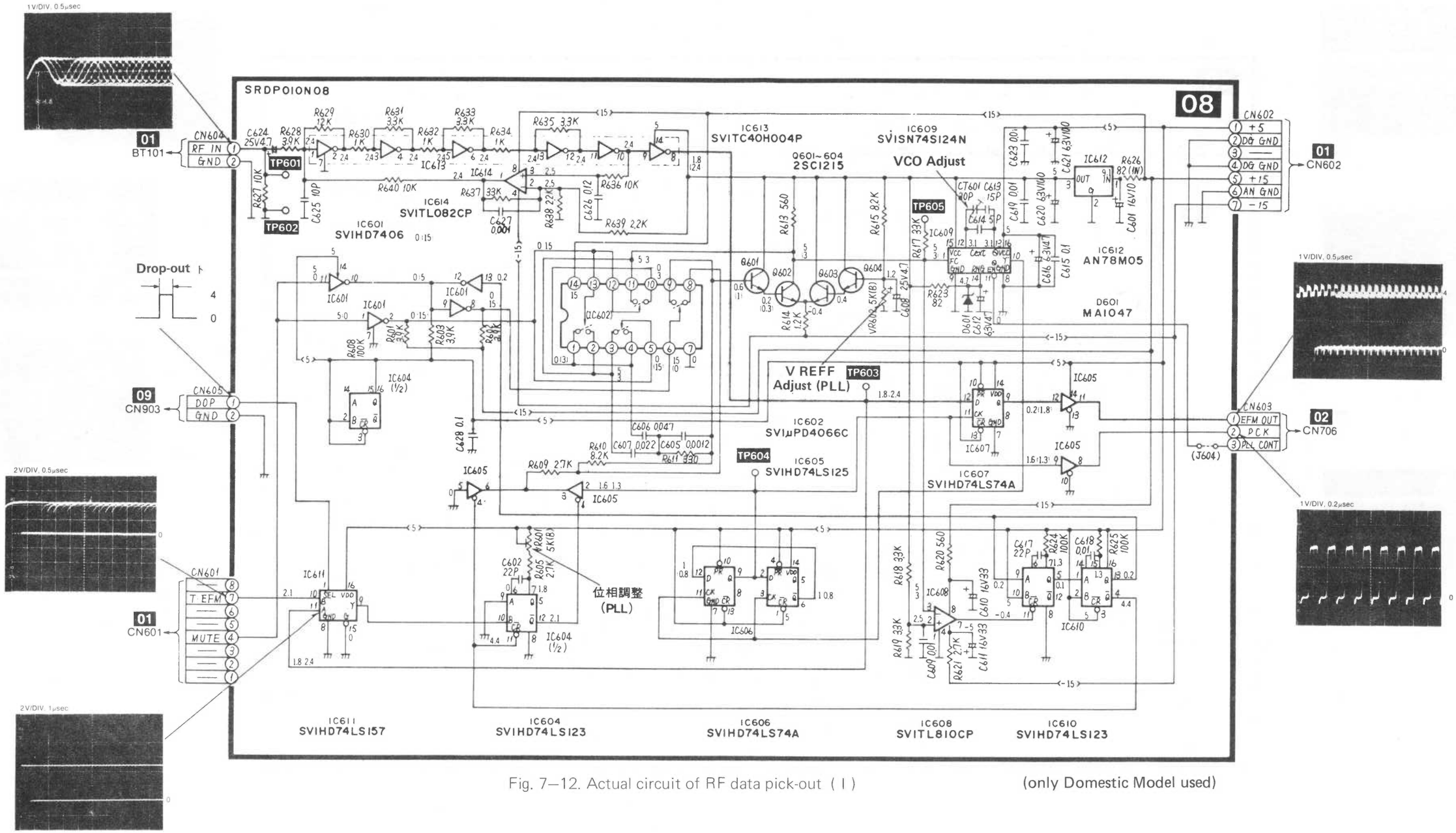


Fig. 7–12. Actual circuit of RF data pick-out (I) (only Domestic Model used)

RF data pick-out circuit

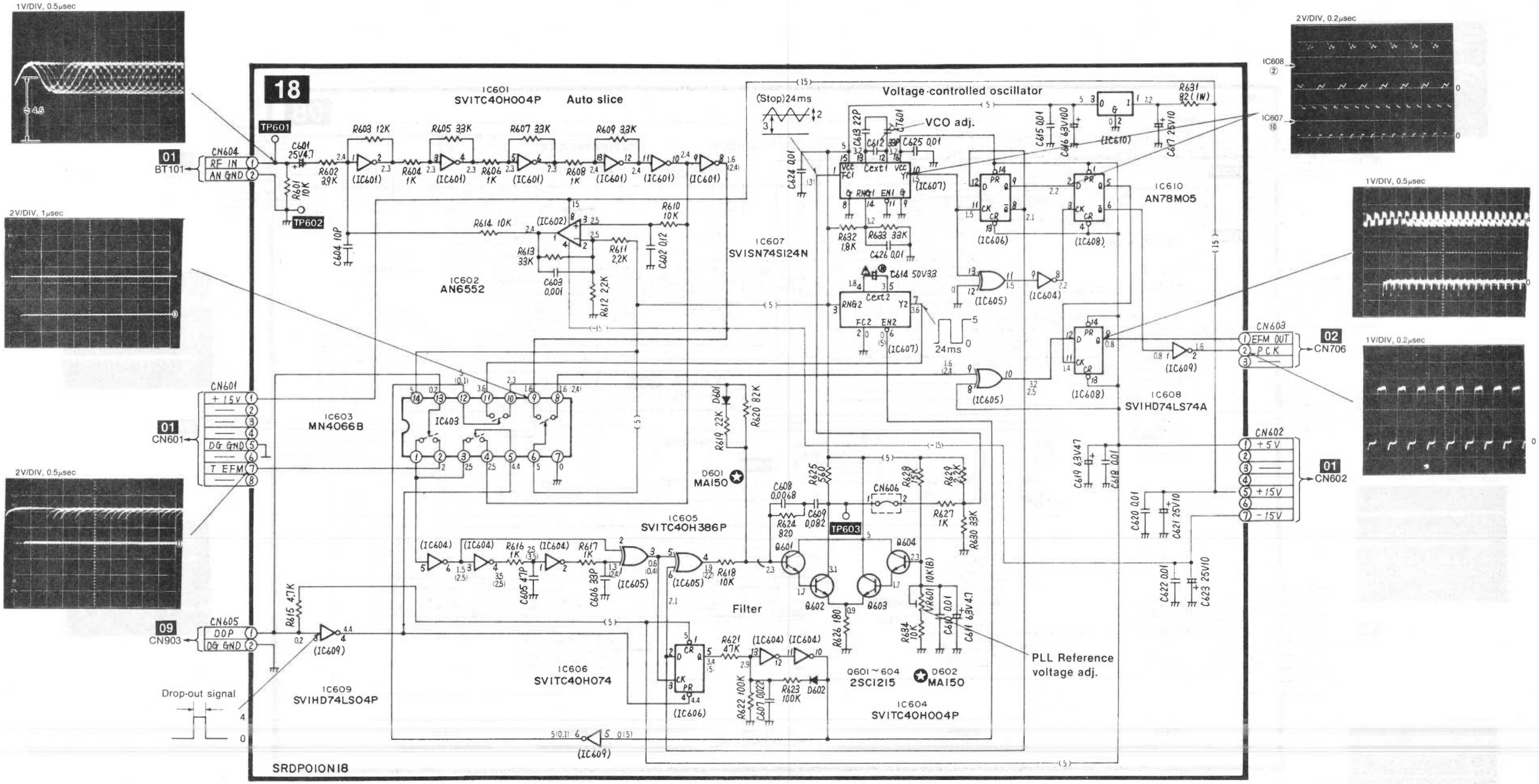


Fig. 7–13. Actual circuit of RF data pick-out (II)

7–4. RF data pick-out circuit operation (II) .... [18] P.C.B. (Exs)

The actual circuit of RF data pick-out (II) is shown in Fig. 7–14.

RF signal waveform shaping circuit

IC601 (40H004) serves to shape the waves of RF signal from optical PU while amplifying the signal. IC602 serves to check the integrated value (DC) of wave-shaped RF signal and to feed it back to IC601-pin (1) so that the value is always 1/2 VCC.

If the DC part of IC601-pin (1) is deflected to higher voltage, it will result in pin (3) ↘ pin (5) ↗ pin (13) ↘ pin (11) ↗ pin (10) ↘, thereby controlling the positive (+) input of IC602. Becuase the negative (-) input is constant, the feedback voltage to IC601-pin (1) serves to make up for the alteration of DC voltage of input RF signal.

As a result, the alteration of DC level generated in the course of disc manufacture or optical PU is absorbed to restore the correct digital signal.

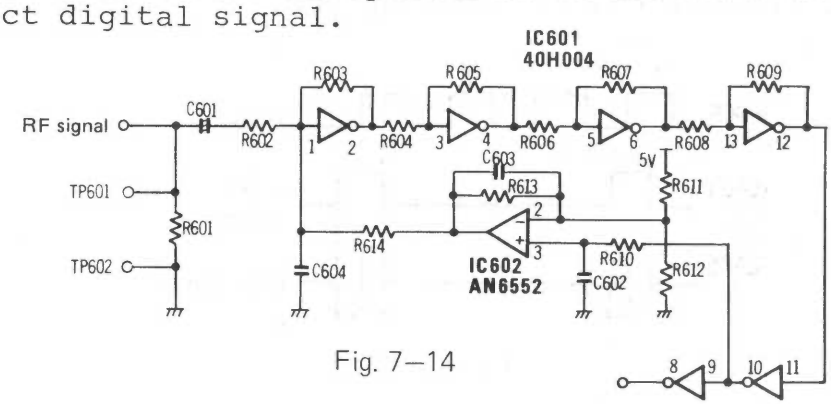


Fig. 7–14

PLL circuit (PCK generating circuit)

IC603 (MN4066B) pins (1) - (2) and (3) - (4) are equivalent to SW1 shown in the block diagram. In normal playback mode, playback signal with shaped waveform is obtained at IC604 pin (5). (Drop-out detection signal is applied to IC609.)

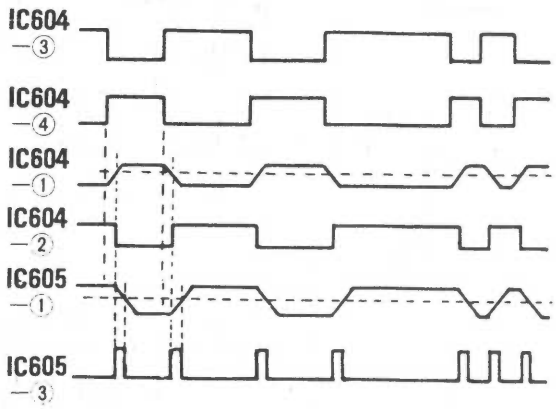


Fig. 7-15 Edge pulse generation

IC604 (A) (B) and IC605 (A) are playback signal edge detection circuit, and its width is changed to 0.5T according to the constant of CR to take out the edge. It is illustrated in Fig. 7–15.

* 1T is 4.32 MHz, and EFM data of playback signal is modulated at 3T - 11T.

IC607 (74S124) (A) is changed in frequency of output pin (10) according to the PC voltage of pin (1) (FC input) by VCO of PLL.

The free-run frequency of VCO is about 8.64 MHz. It changes into PCK of about 4.32 MHz (= 1T) through 1/2 frequency division at IC606.

IC605 (A) compares PCK (= 1T) and edge pulse (= 0.5T) and PC (phase comparator). It is illustrated in Fig. 7–16.

PLL is locked when phase difference between PCK and 0.5T is 90°. (Area is equalized at ◯ marks.)

Q601 - Q604 set up LPF and changes the output difference of PC into DC to control the FC input of VCO.

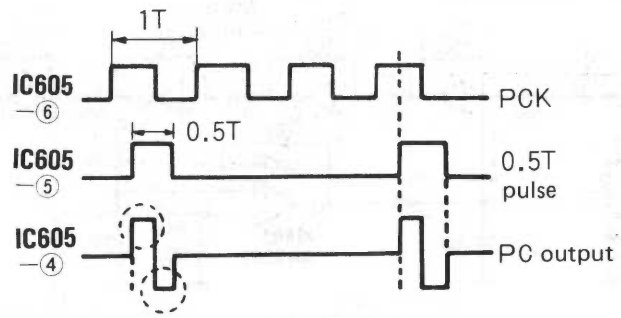
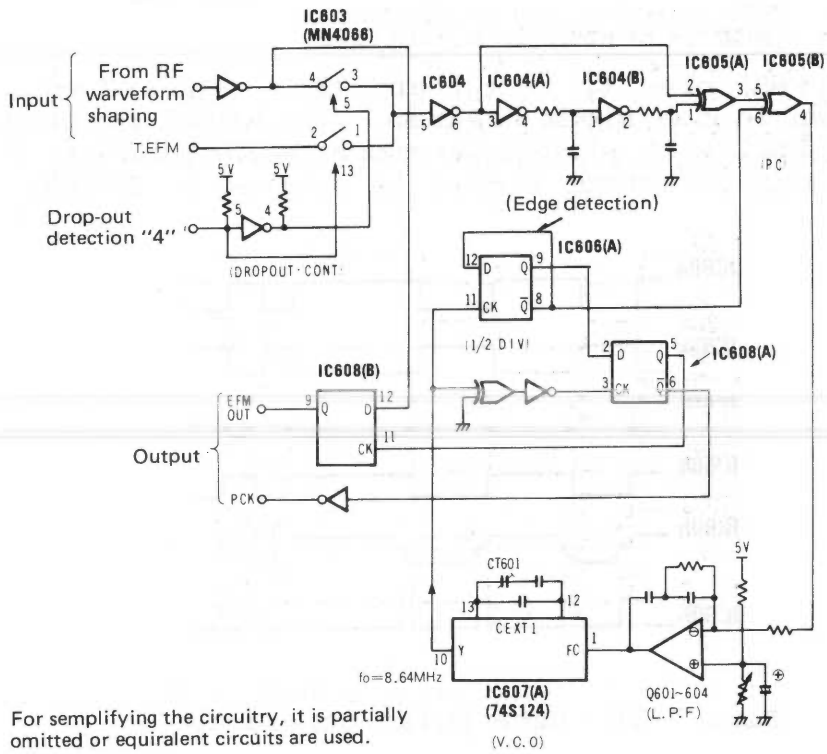


Fig. 7–16



For semplifying the circuitry, it is partially omitted or equiralent circuits are used.

Fig.7–17

PLL lock range detection and search circuit

IC606 (40H074) (B) controls the relationship between edge pulse and PC phases. It is illustrated in Fig. 7-18.

In normal playback, the signal is picked out at the rise of edge pulse whose phase difference from PCK is 90°, therefore the output level is "H" constant and IC604 pin (12) is "L" and IC604 pin (10) "H", then search oscillation circuit does not operate.

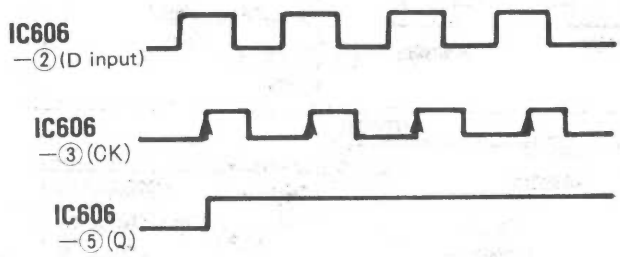


Fig. 7-18 (a)

In case of high-speed search, PLL comes outside the lock range, causing the input phase relation of IC606 (B) to be disturbed, then the output at IC606 pin (5) (Q output) is wrong, but it is filtered by C607 so that the level of IC604 pin (13) becomes "L" and IC604 pin (10), "L" as well.

As a result, the search oscillator consisting of IC607 (74S 124) (B) is shifted to oscillation mode. Then, analog switch IC603 pins (11) - (10) turn ON due to IC609 (A), and FC input of VCO is swept to detect the optimum value, then PLL is locked again.

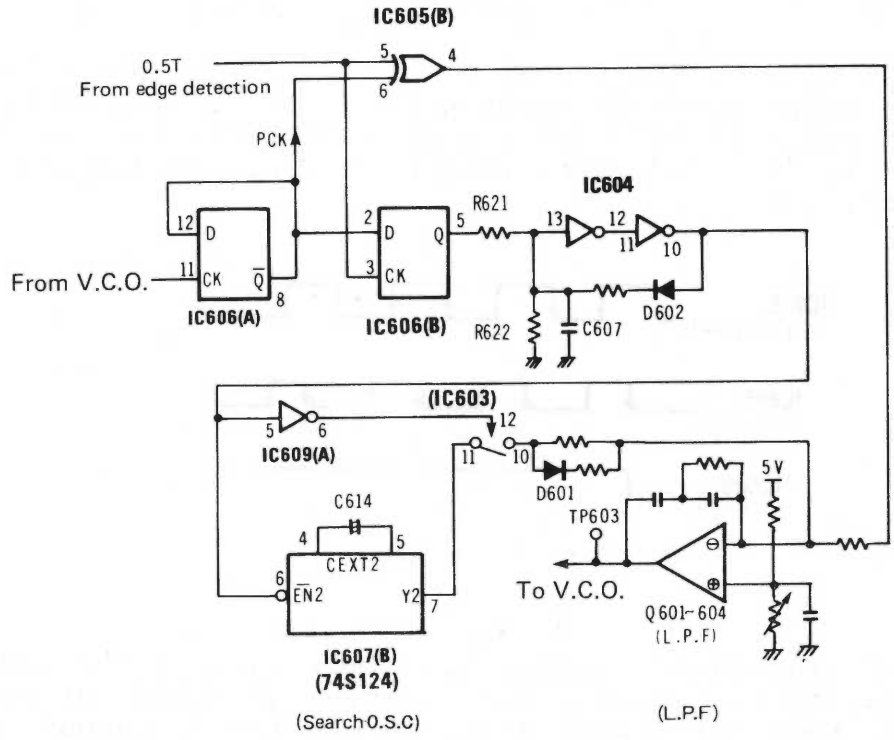
Drop-out control circuit

IC603 (MN4066B) pins (1) - (2) and (3) - (4) are drop-out control circuit. If RF signal is missing due to drop-out, then 0.5T edge pulse cannot be detected and PLL does not operate. So, in case of drop-out, it is remedied through the following operation.

Drop-out detection signal ("H" in drop-out mode) is applied to CN605 pin (1). (Refer to the section of Drop-out detection circuit on page 68.) Thus, during normal playback mode, RF signal with shaped waveform is selected. T·EFM signal is selected in drop-out mode.

T·EFM signal is pure electrical EFM data mode by demodulation LSI.

That is, during drop-out, PCK is properly controlled through substitution with T.EFM, while the correcting circuit of demodulation LSI will take care of data missing.


IC605(B)
0.5T
From edge detection
PCK
From V.C.O.
IC606(A)
IC606(B)
R621
IC604
R622
C607
D602
(IC603)
IC609(A)
D601
TP603
5V
C614
CEXT2
EN2
Y2
IC607(B)
(74S124)
To V.C.O.
Q601~604
(L.P.F)
(Search O.S.C)
(L.P.F)

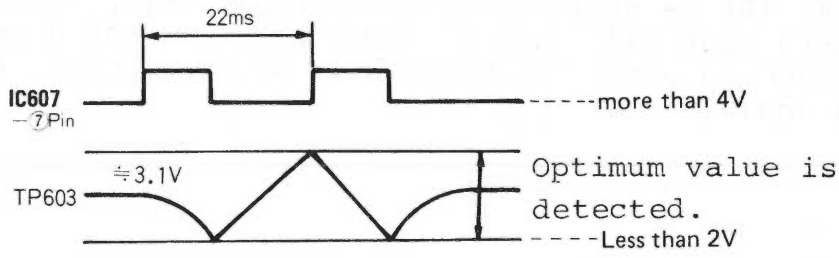

22ms
IC607
7 Pin
-----more than 4V
≒3.1V
TP603
Optimum value is
detected.
----Less than 2V

Fig. 7-18 (b)

8. Drop-out detection circuit

8–1. Role of drop-out detection circuit

This circuit detects whether drop-out has occurred in RF signal. The output is used for input data selection of RF data pick-out circuit to attain the hold operation of PLL in order to prevent the bit clock from being disturbed.

8–2. Configuration of drop-out detection circuit

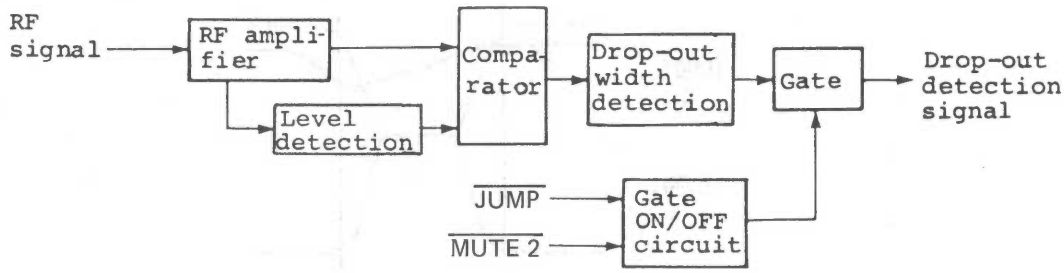


Fig. 8-1 Block diagram of drop-out detection circuit

The block diagram of drop-out detection circuit is shown in Fig. 8-1.

The input is RF signal. It is first subjected to RF amplification and level detection. After that, drop-out detection signal is generated by the combination of comparator and one-shot multi.

A gate circuit is the output circuit that controls the detection signal to decide whether it is delivered to the data pick-out circuit in the next stage.

When the detection signal is delivered with the gate closed, PLL operates in hold mode. (Refer to the section of RF data pick-out circuit on page 70.)

8–3. Drop-out detection circuit operation

The actual circuit of drop-out detection is shown in Fig. 8–5.

Drop-out detection circuit

Q901 - Q904 and IC901 perform RF amplification and level detection.

IC901 applies RF signal to pin (2) (plus input), and the signal (RF level converted to DC) to pin (3) (minus input) for the purpose of comparison. It is illustrated in Fig. 8-2.

The drop-out is generated when the input voltage is in the relation of (-) > (+).

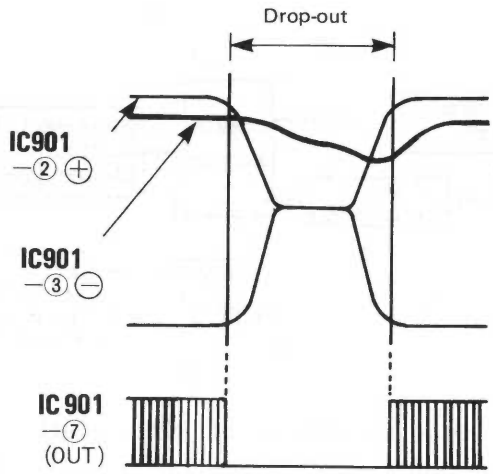


Fig. 8-2 Drop-out detection

IC902 (74LS123) is one-shot multi where the width of drop-out is decided. The time constant of IC902 (A) is 14 μs - 20 μs (adjusted by VR901).

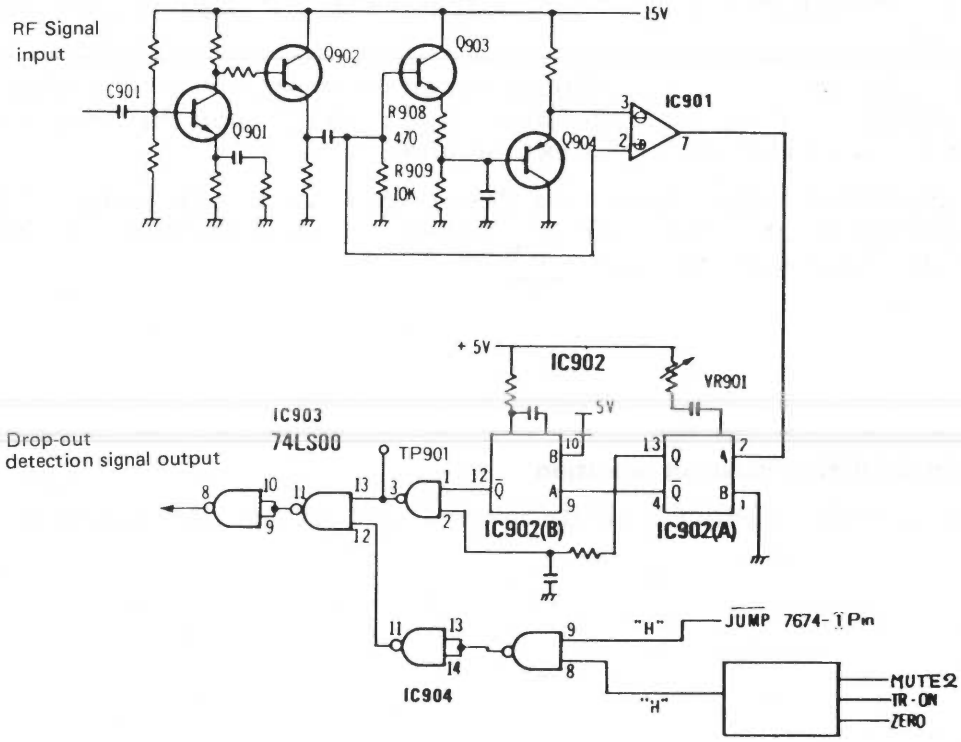


Fig. 8-3 Drop-out detection circuit

The RF signal of reproduced data is subjected to EFM modulation at 3T - 11T. 1T is about 0.23 μs (=4.32 MHz), therefore, the data ranges from 0.7 μs to 2.5 μs. Accordingly, IC902 (A) is always re-triggered when data exists, and the level of pin (13) (Q output) is "H".

If IC902 (A) is not re-triggered, drop-out detection signal is delivered as shown in Fig. 8–4. IC902 (B) operates so that the gate will not open for 1 ms after re-triggering.

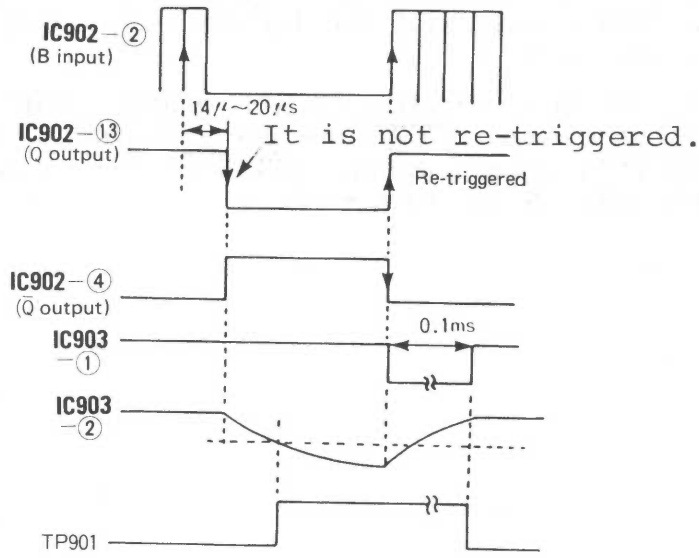
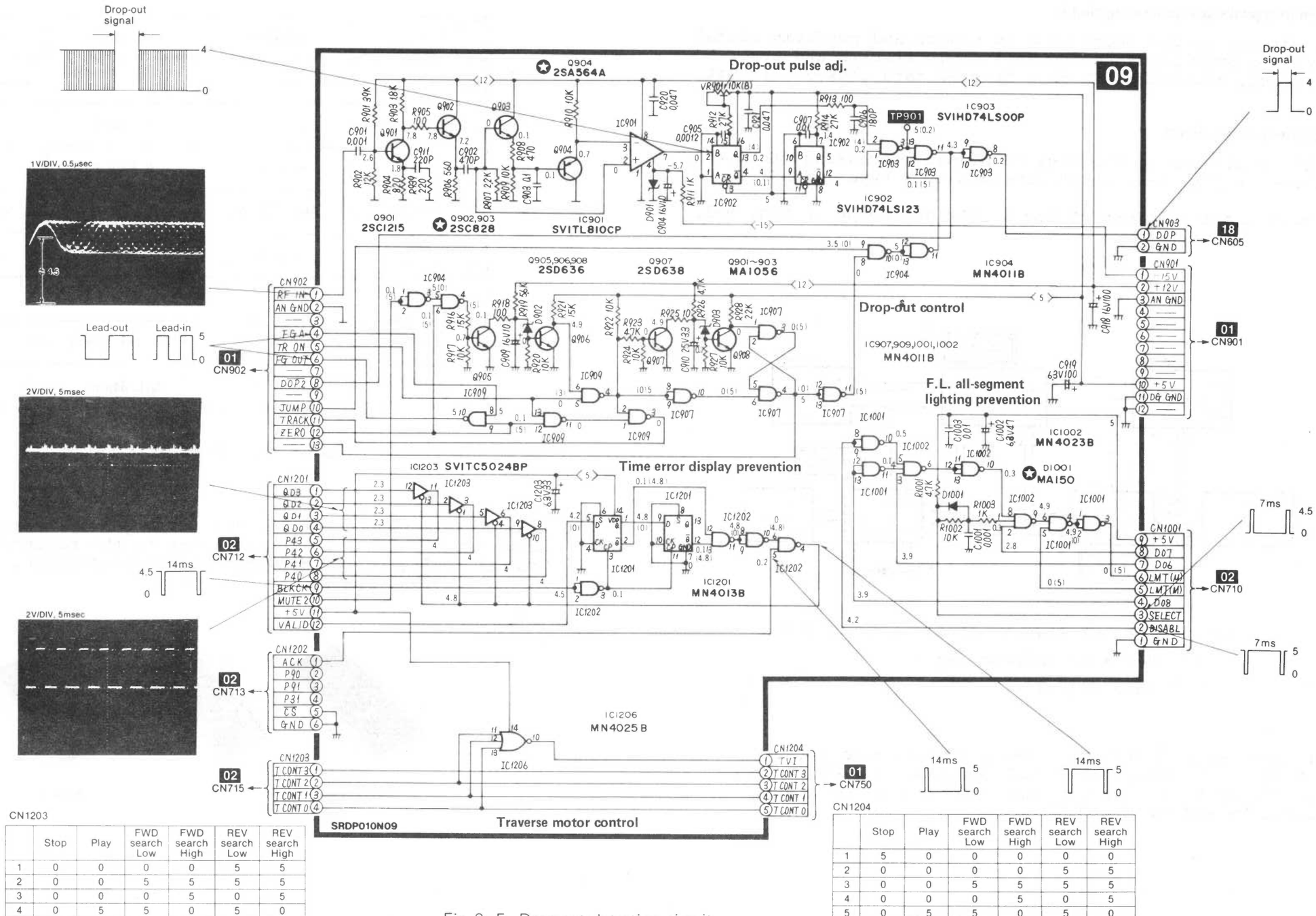


Fig. 8–4

Drop-out detection signal ON/OFF circuit

IC903 pin (12) is at "H" and delivers the drop-out detection signal to the data pick-out circuit. It holds PLL to prevent PCK from being disturbed. However, if the drop-out width exceeds the correction range of LSI or the tracking servo is intentionally released by system microcomputer (track jump like access, etc.), PLL, if held, will not be shifted to search mode and not re-locked. (If PLL is held for long, the system will disorderly operate because of digital muting.) In that case, the circuit is controlled so that drop-out detection signal will not be delivered. It is ON/OFF signal --- IC903 pin (12).

IC904 pins (8) and (9) are ON/OFF signal input; pin (9) detects input signal ($\overline{\text{JUMP}}$) --- intentional track jump, and pin (8) detects input signal ($\overline{\text{MUTE 2}}$) --- digital muting due to excessive range of drop-out.



CN1203

	Stop	Play	FWD search Low	FWD search High	REV search Low	REV search High
1	0	0	0	0	5	5
2	0	0	5	5	5	5
3	0	0	0	5	0	5
4	0	5	5	0	5	0

CN1204

	Stop	Play	FWD search Low	FWD search High	REV search Low	REV search High
1	5	0	0	0	0	0
2	0	0	0	0	5	5
3	0	0	5	5	5	5
4	0	0	0	5	0	5
5	0	5	5	0	5	0

Fig. 8–5. Drop-out detection circuit

9. Digital signal processing circuit

9–1. Function of digital signal processing circuit

This circuit is the heart of a DC player and performs signal processing such as EFM demodulation, interleave and error correction, receiving EFM data from RF data pick-up circuit.

9–2. Configuration of the circuit

The block diagram of the digital signal processing circuit is shown in Fig. 9-1, which consists of 3 types of LSI.

The main specifications of the 3 LSIs are shown in Fig. 9-1.

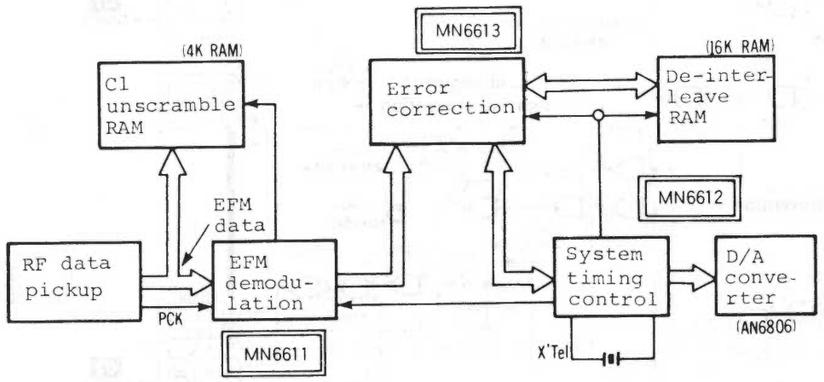


Fig. 9-1 Block diagram of digital circuit

→ Clock or address signal

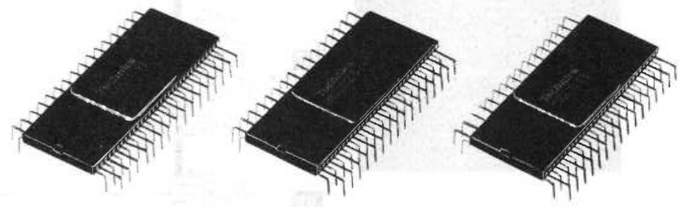
⇨ Data signal

* Signal processing by PCK (bit synchronizing clock) is up to writing into 4 KRAM, and X'tal frequency dividing clock is used for reading. Accordingly, jitter part of signal reproduced by RAM is absorbed.

	MN6611	MN6612	MN6613
Main function	EFM demodulation	System timing generation	Error correction
Process	N—MOS		
Chip size	6.0×5.3	6.4×6.6	7.1×6.8
No. of elements	About 13,000	About 17,000	About 20,000
Operating frequency	6 MHz	8.64MHz	2.16MHz
Input/output level	TTL compatible		
Power supply	+5V UM-1 power source		
Shape	QIL 64pin		

Table 9-1 Spec of 3 LSI's

Before explaining about the digital signal processing circuit consisting of the 3 LSI's, we refer to the recording system (signal configuration and processing) to describe the function of the playback system.



MN6611 MN6612 MN6613

9–3. Signal processing in recording system

— Encoder —

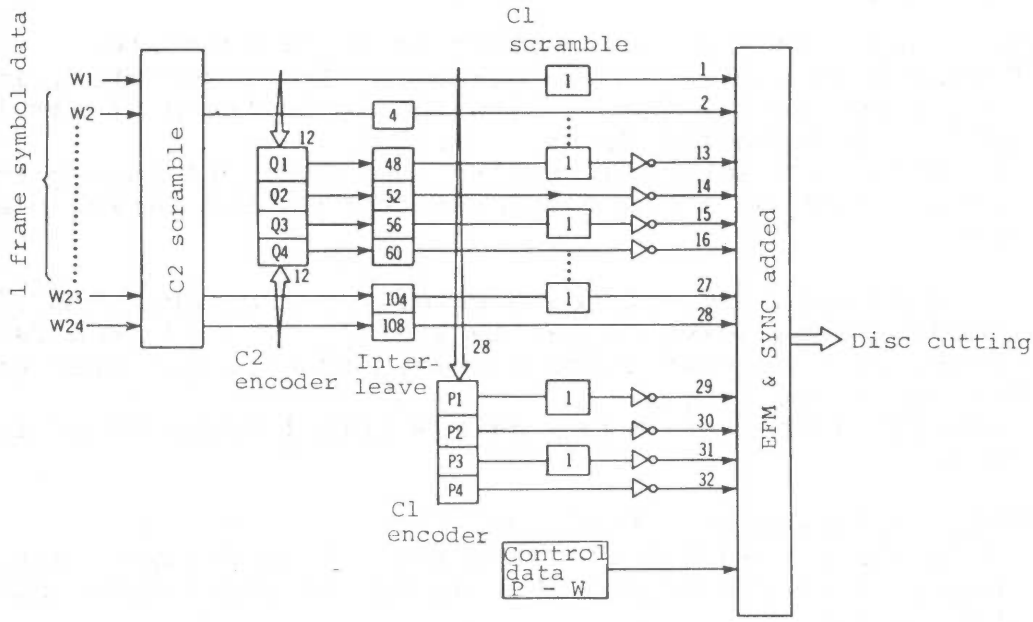


Fig. 9–2. Signal Processing in recording system

Signal processing in recording system

The block diagram of CD is shown in Fig. 9-3. A breif explanation is given in the following.

(1) Sampling frequency of CD is 44.1 kHz. For quantizing, it is A-D converted to 16 bits per sample.

Next, the 16 bits are divided into the upper 8 bits and lower 8 bits.

* 1-sample 16-bit is called "data word", and 1-symbol 8-bit is "symbol data".
That is, 2 symbols make 1 data word.

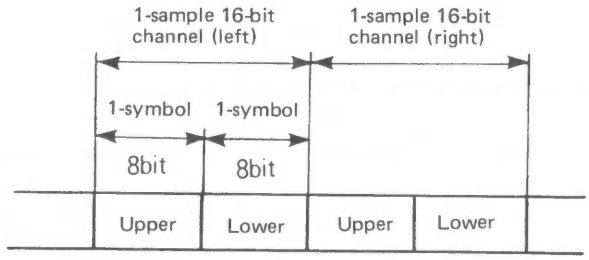


Fig. 9-3 Symbol data and data word

(2) Regarding the frames for signal processing, one frame consists of 12 sample data (6 each for R and L). That is, 24 symbol data make 1 frame, and W1 - W24 in Fig. 9-4 correspond to it.

(3) W1 - W24 data are first subjected to C2 scramble. Scramble is similar to interleave. In C2 scramble, it is delayed over 2 frames alternately in terms of sample data. (Independent R, L)
The effect of scramble results in signal processing for facilitation of average value interpolation during playback.

(4) After C2 scramble, the data enters C2 encoder. The C2 encoder makes 4-symbol parity signals Q1 - Q2 from 24-symbol data by reed solomon code, and arranges them at the center of frame.
Here the number of symbol data within 1 frame is 28 in total.

(5) It is followed by interleave.
As is evident in the illustration, it is delayed over 4 frames up to 108 frames as against 28-symbol data including Q parity.

(6) C1 encoder makes 4-symbol parity signals P1 - P4 from 28-symbol data, re-arranged through interleave, by reed solomon code, and arranges them at the end of the frame.
Here the number of symbol data within 1 frame is 32 in total. (Refer to Fig. 9-4.)

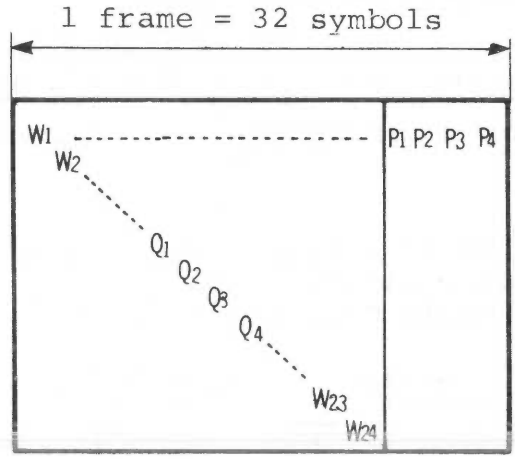


Fig. 9-4 Configuration of CIRC symbols

* 4-symbol parity of P1 - P4 is added to 28 symbols in 1 frame horizontally, and 4-symbol parity of Q1 - Q4 is added to 24 symbols aslant in the middle of frame.

(7) In C1 scramble, only even-number symbols of 32-symbol data in 1 frame are delayed to the next frame.
The effect of C1 scramble results in signal processing for improving the ability to detect errors that occur at random relatively in a short time.

(8) Control data P - W are also called sub-codes or user's bits, and include time information for random access and display, consisting of 1 symbol (8 bits).
The signals are arranged at the head of the frame.
With the control signal applied, the number of symbol data in 1 frame is 33 in total.
The detail of control data is explained on page 98.

(9) Finally, the 1-frame symbol data are subjected to EFM modulation and are recorded on the disc with frame synchronizing signal added.
The details of EFM modulation is explained in the next paragraph.

In the above-mentioned recording signal processing operation, Q parity is made in the earlier stage of interleave, and P parity is made in the latter stage.
Each of these is intended to improve the error correction ability, and this system is called CIRC (Cross-Interleave Reed Solomon Code).

EFM modulation

EFM modulation is a new modulation system for CD which converts symbol data bits (8 bits) to channel bits (14 bits), and EFM stands for Eight to Fourteen Modulation.

EFM is necessary because it is unable to define the arrangement of data bits, that is, "1" and "0", without modulation of symbol data. For example, if "1" or "0" continue very long, then the data is DC, making it impossible to generate self-clock at the tracking servo (activated by use of pit) or the playback system.

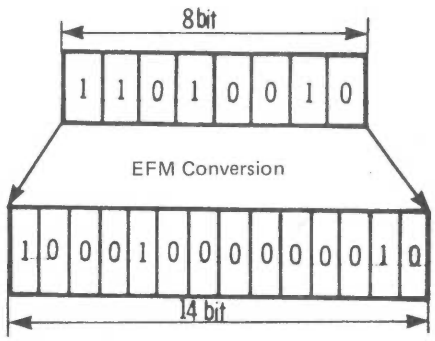
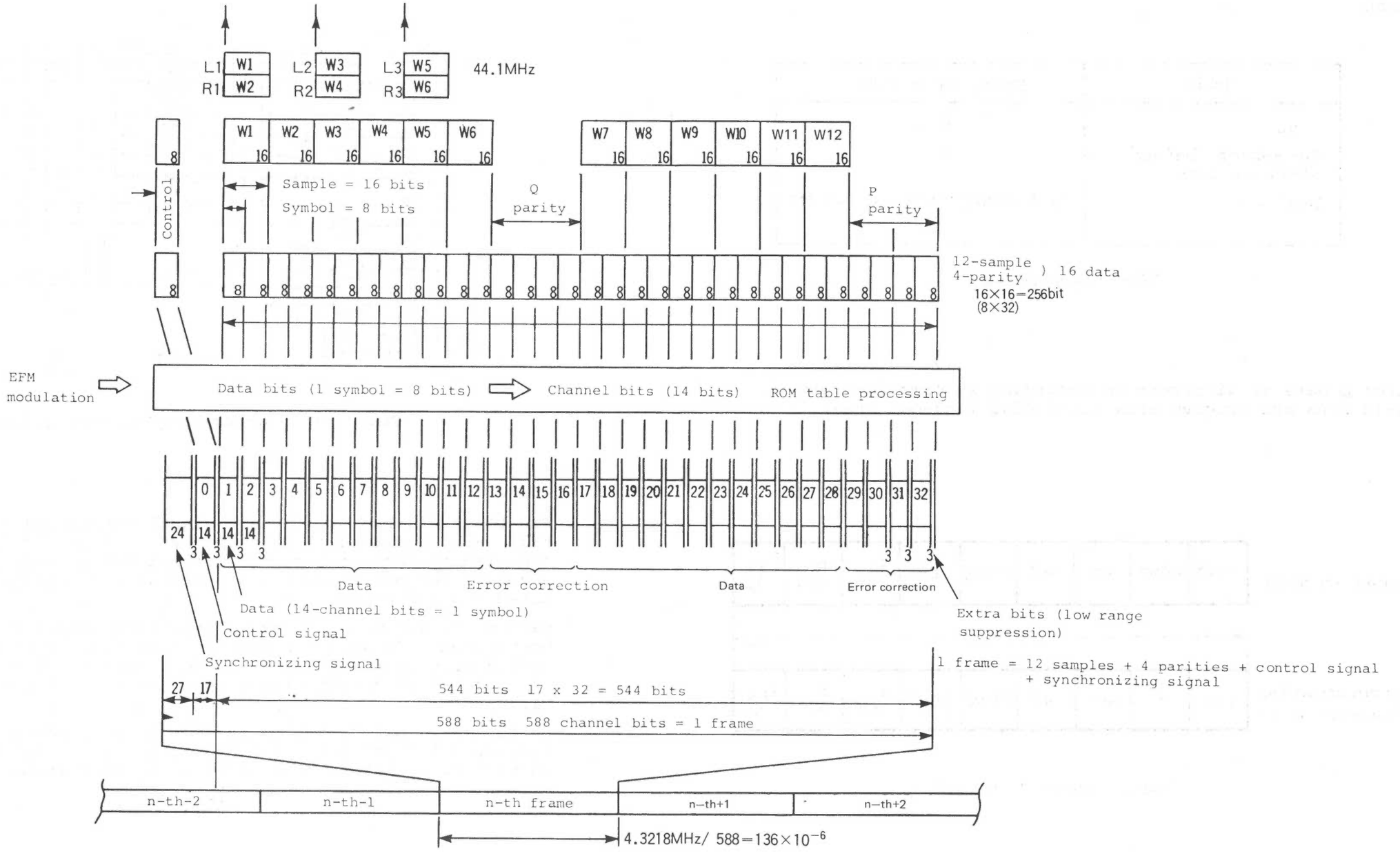


Fig. 9-5 EFM modulation

If "1" or "0" are frequently inverted, it will be necessary to greatly reduced the diameter of laser beam spot.
Therefore, the signal recorded on the disc must be such that "1" or "0" are inverted at proper intervals and that the DC component is as less as possible.
There are 256 combinations in 8 bits that is 2^8, and 16384 combinations in 14 bits that is 2^{14}.
In EFM, there are 2 < 10 "0's" between "1" and "1" in the bits row. The pattern selected from among 2^{14} is composed with the data pattern of 2^8.
Accordingly, the signal recorded is formed to have 3T - 11T (T is "1" and 1 clock after EFM is 4.32 MHz.)

9–4. Shows the processes up to recording signal format



* The 3 bits out of the 14 bits are called extra bits which serve as a liaison to maintain the EFM level even through the data.

Fig. 9-6 CD signal format

Control data

Control P data is a signal to distinguish between tune and blank.

Mode	State of P data
Tune	0
Two seconds before start of tune	1
Lead-in out	1, 0 changeover at 0.5 Hz

Table 1 = Control P data

Control Q data is different in recording information between lead-in area and program area (including lead-out area).

Lead-in area	T.NO	POINT	MIN	SEC	FRAME	ZERO	P MIN	P SEC	P FRAME
	← 8 × 9 = 72bit →								
Program area/ Lead-out area	T.NO	X	MIN	SEC	FRAME	ZERO	A MIN	A SEC	A FRAME

Table 2 = Control Q dara data

9–5. Playback signal processing

— Decoder —

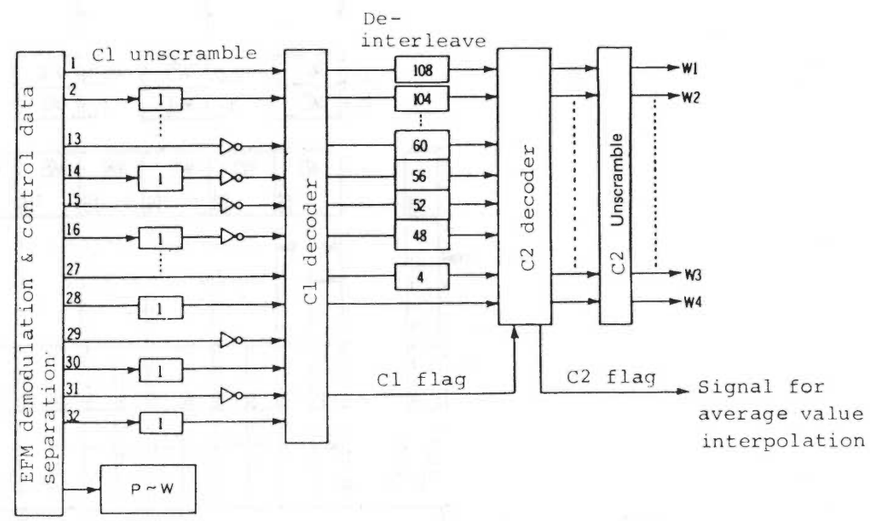


Fig. 9-7 Playback signal processing

The block diagram of playback signal processing is shown in Fig. 9-7. Playback signal processing is in the direction opposite to that of recording signal processing. C1 and C2 encoders for parity making are replaced by decoders for error detection and correction.

Each of C1 and C2 decoders is capable of error detection and correction. Data that cannot be corrected by C1 decoder is marked with C1 flag, and it is delivered to C2 decoder after the process of de-interleave in order to make further correction.

As for data that cannot be corrected by C2 decoder, the average value obtained from adjacent data is subjected to interpolation after the process of C2 unscramble.

9–6. Playback Mode circuit

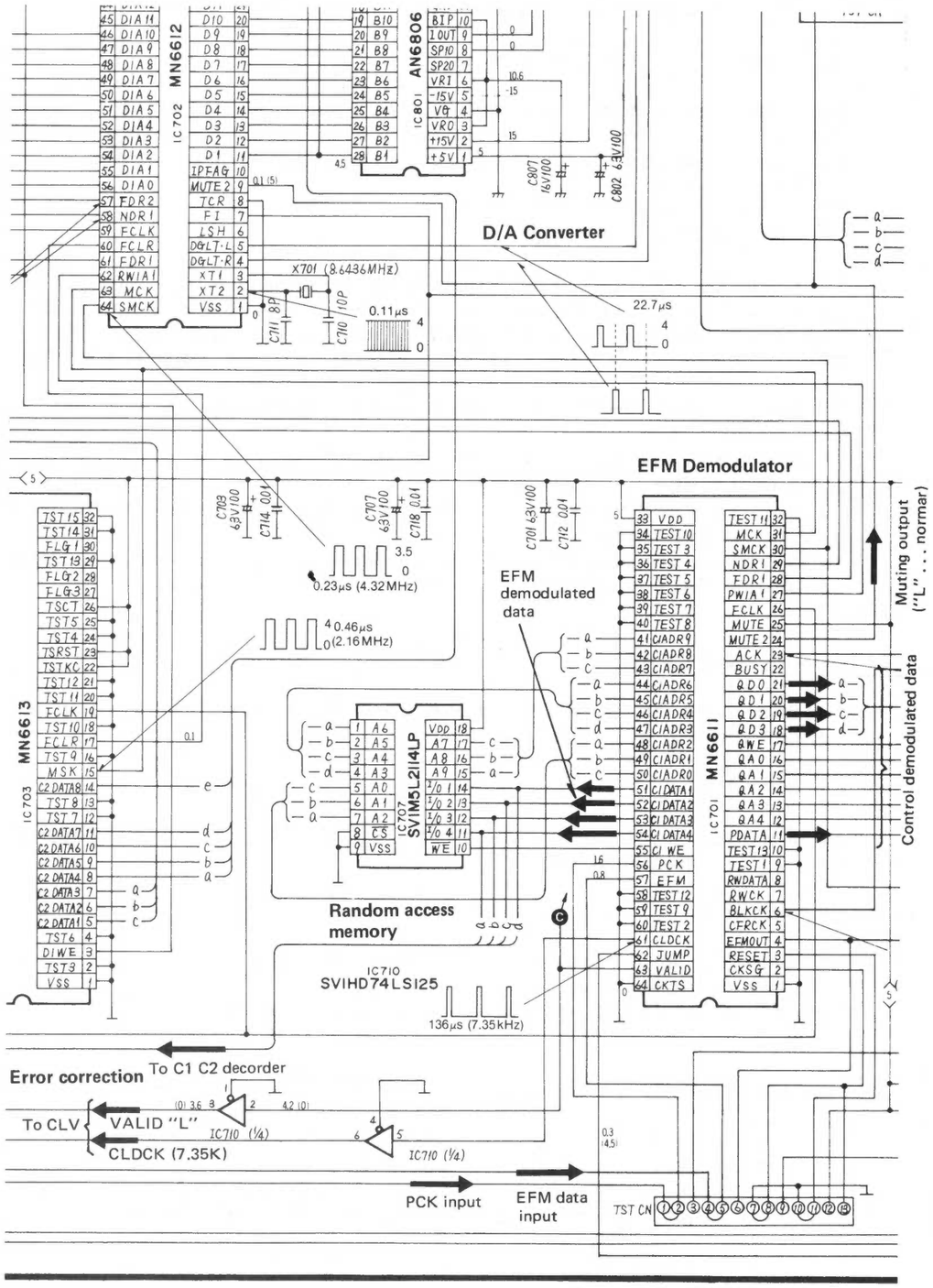


Fig. 9–8. MN6611 with other circuit

Operation of MN6611

MN6611 functions to perform EFM demodulation, C1 unscramble and jitter absorption, demodulation of control data, and CLV servo control signal generation.

(1) EFM demodulation

EFM data of wave-shaped RF signals are latched every 14 bits by use of extracting clock PCK to change it to the original 8-bit data.

(2) C1 unscramble

In the case of optical disk, random short errors are generated more often than in PCM tape. So, time axis of C1 and C2 unscramble is controlled to cope with these short errors. Furthermore, in C1 unscramble, jitter absorption is performed as well as writing by extracting clock and reading by crystal clock.

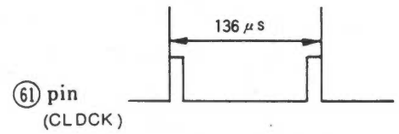
(3) Demodulation of control data

Control data is subjected to EFM modulation the same as other symbols and is recorded.
Sub-code decoder detects synchronizing signal out of 14 bits before EFM demodulation and demodulates P, Q data and transfers it to system microcomputer.

(4) Generation of CLV servo control signal

CLV servo control signal is generated by detecting frame-synchronized signal out of EFM data. The roles of MN6611-pin 61 (CLDCK) and pin 63 ($\overline{\text{VALID}}$) corresponds to it.

CLDCK is frame-synchronized PCK, and $\overline{\text{VALID}}$ is the flag signal that indicates synchronization of the demodulation system. These signals enter the CLV servo circuit and are used as servo control signals. (Refer to CLV servo on P76.)



(1) Above-mentioned frame signal is generated when synchronized.

(2) "L" when synchronized and "H" if not synchronized.

Also, pin 24 ($\overline{\text{MUTE2}}$) of MN6611 generates muting signal and delivers "H" output in normal play mode. The signal is used to decide whether the data is delivered to DA converter. (It controls MN6612.)

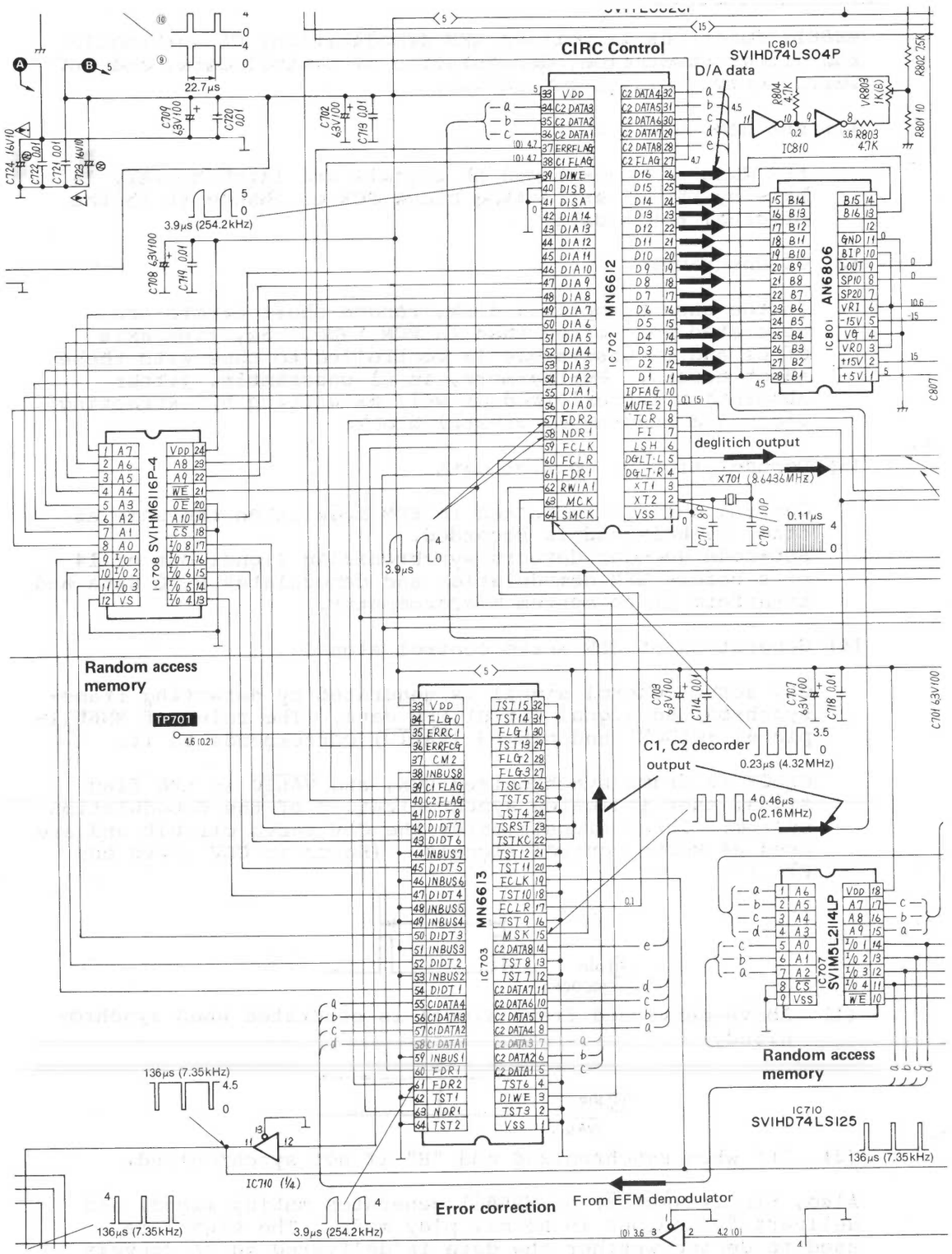


Fig. 9–9. MN6612, 6613 with other circuit

Operation of MN6612

MN6612 functions to perform generation of system timing, de-interleave, C2 unscramble and mean value interpolation.

(1) Generation of system timing

Various basic timing signals used in MN6612, MN6611 and MN6613 are generated on the basis of 2.16 MHz clock obtained through frequency dividing of 8.64 MHz clock oscillated by crystal oscillator.

(2) De-interleave

This is to control the time axis to change the data interleave during recording back to the original arrangement. The data are handled between MN6613 and external RAM. MN6612 generates the address signal of the external RAM.

(3) C2 unscramble and mean value interpolation

This is to control the time axis to change the C2 data scrambled during recording back to the original arrangement. Also performed is data conversion for the purpose of digital/analog conversion.
Mean value interpolation is to make mean value data from adjacent data with respect to uncorrected data.

Operation of MN6613

MN6613 functions to perform error detection and correction as C1 decoder and C2 decoder.

(1) C1 decoder

It detects and corrects errors by parity P signal from data after C1 unscramble.

(2) C2 decoder

It detects and corrects errors by parity Q signal from data after de-interleave.
The flow chart of error correction is shown in Fig. 9-10.

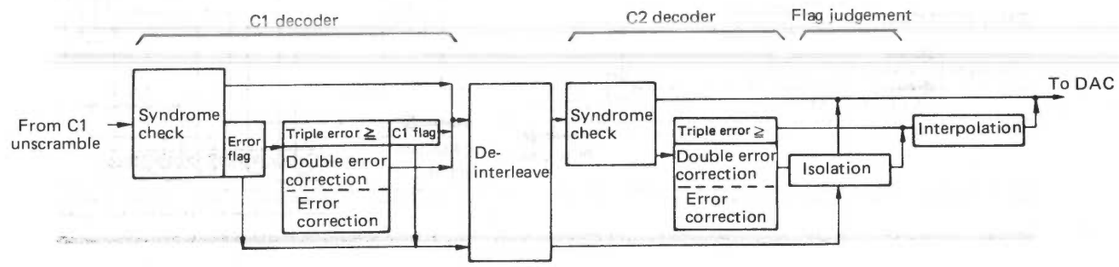


Fig. 9-10 Error correction flow chart

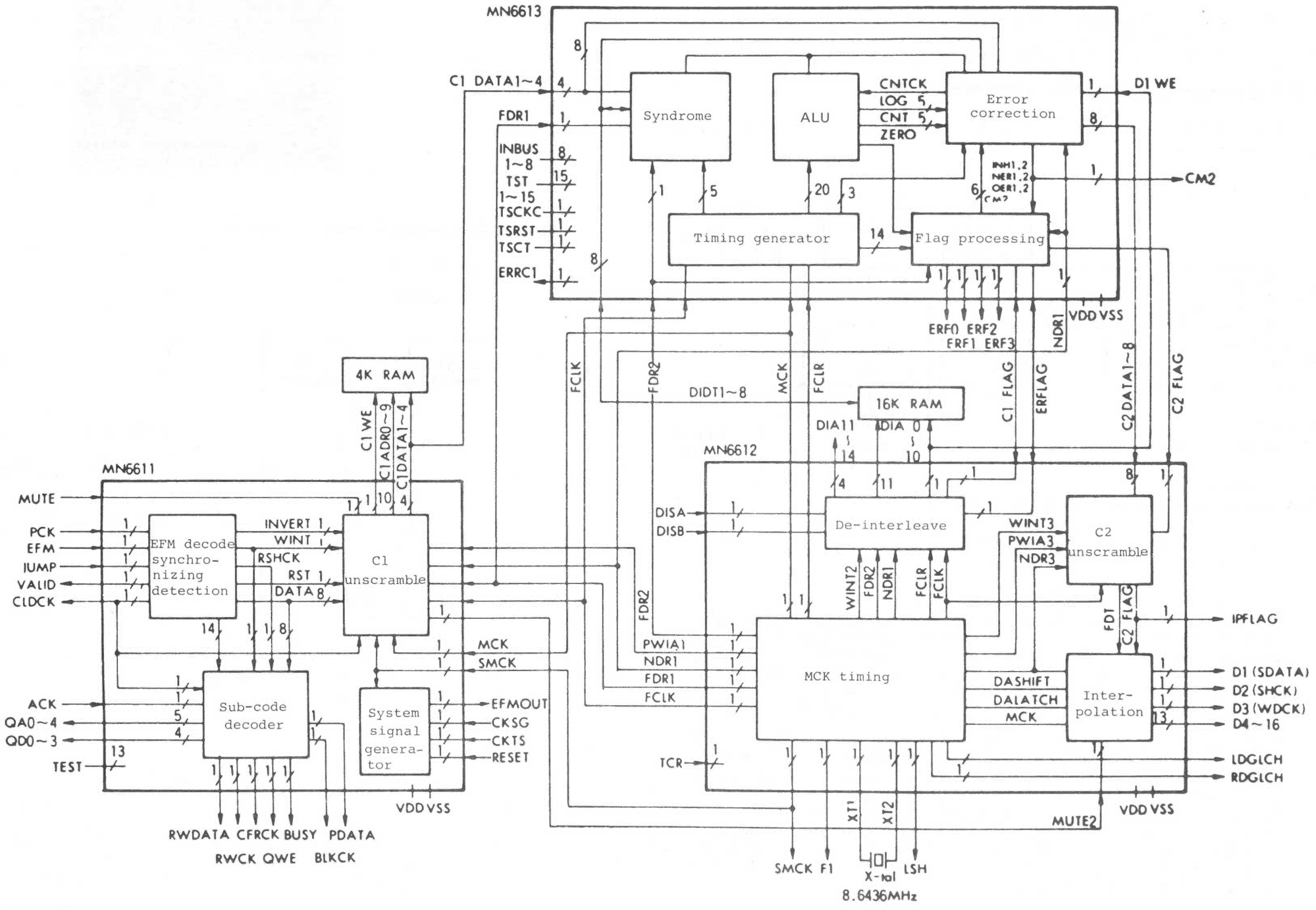


Fig. 9-11 Digigal signal processing LSI block

10. D/A Conversion and Audio circuit

10–1. D/A conversion and function of audio circuit

EFM demodulated and error-corrected digital signals are converted to analog signals by the digital signal processing circuit, and the signals are delivered to LINE OUT.

10–2. D/A conversion and audio circuit configuration

The block diagram of D/A and audio circuit is shown in Fig. 10-1.

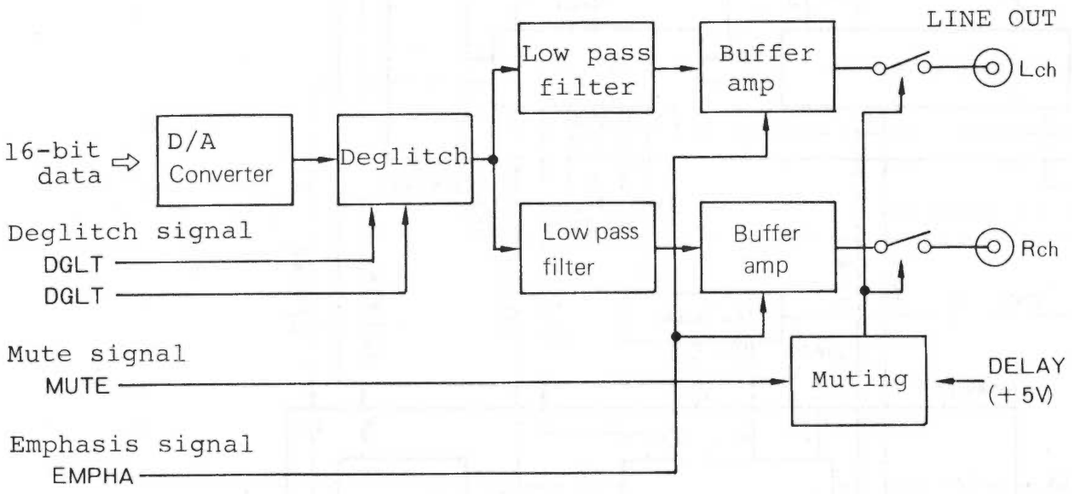
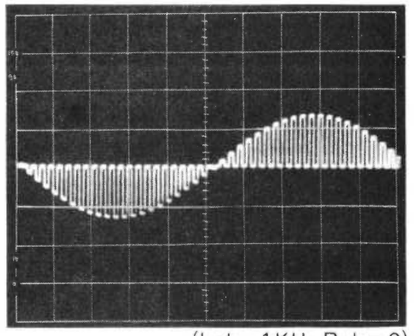


Fig. 10-1 D/A and Audio block

The parallel 16-bit data signal input from the digital signal processing circuit is converted to PAM signal as in Fig. 10-2 by the D/A converter. The PAM signal has both L and R channel components, and is separated into Lch and Rch signals by the deglitch circuit. The separation control select signal is deglitch (DGLT) signal.

Each of the separated signals is restored to the original analog signal through attenuation of frequencies higher than 20 kHz by the low pass filter, and is delivered to LINE OUT by the buffer amplifier.
The muting circuit is controlled with delayed +5 power supply and mute signal of system microcomputer, and prevents shock noise during power ON and set mode changeover. Also, the emphasis signal serves to turn ON/OFF the de-emphasis located in the buffer amp.



(Lch=1KHz,Rch=0)

Fig. 10–2. RAM signal

10–3. D/A conversion and audio circuit operation

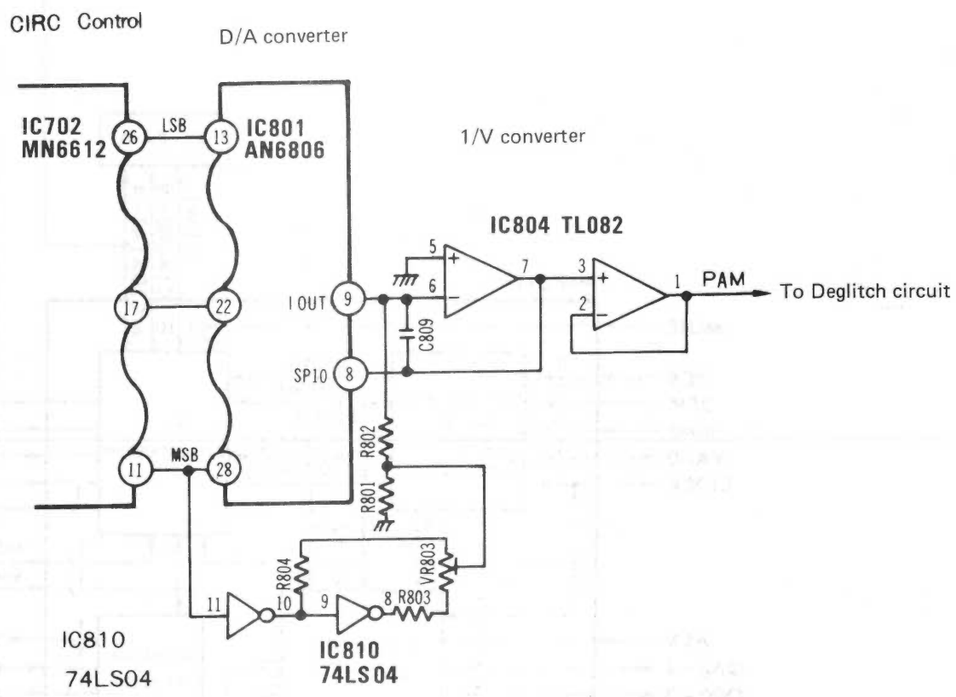


Fig. 10–3. D/A converter circuit

When 16-bit parallel data are put in from IC801 pin 13 (LSB) - pin 28 (MSB), IC801 (D/A converter) delivers a current value to IC801 pin 9 in its data transfer cycle (44.1 kHz x 2) according to the input data. Next, the current output is put into the I/V conversion circuit consisting of IC804 where it is converted into a voltage value and is delivered to the deglitch circuit.
The output signal delivered in this way is PAM signal.

Deglitch Circuit

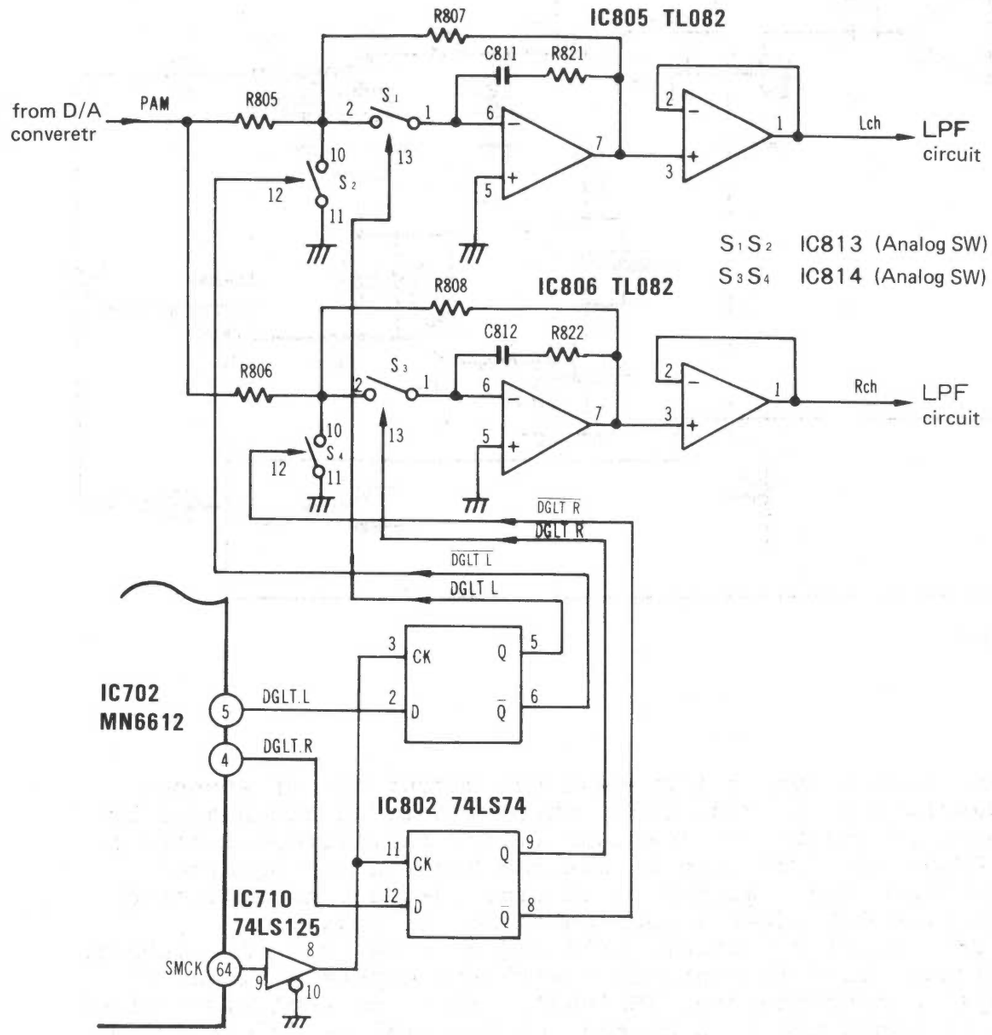


Fig. 10—4. Deglitch Circuit

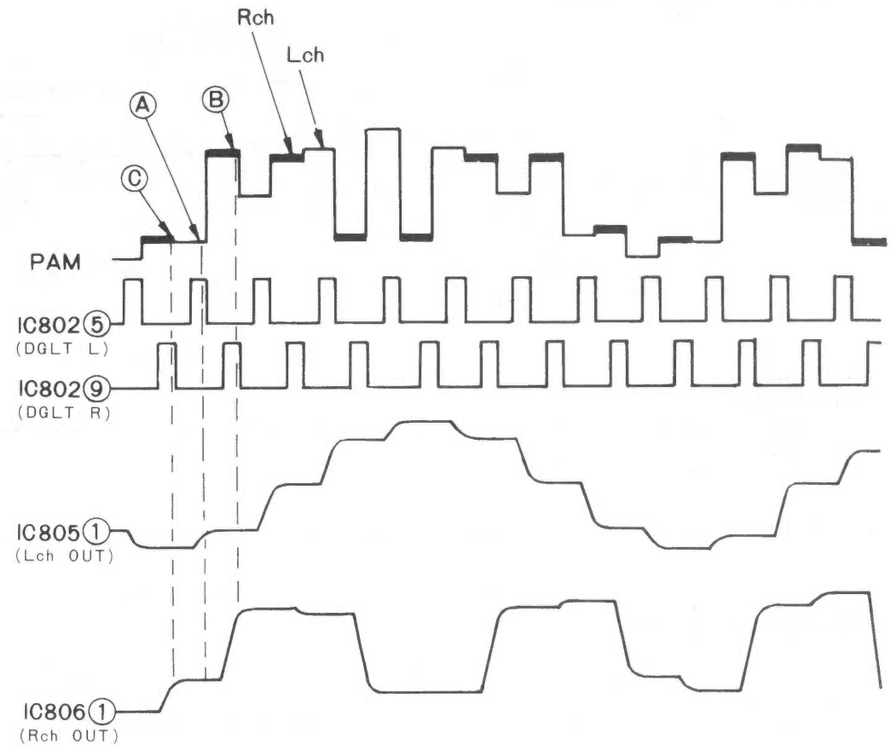


Fig. 10—5. Deglitch timing chart

PAM signal from D/A converter circuit is separated into Lch and Rch signal by the switching circuit consisting of IC802, 805, 806 and S1 - S4 (IC813, 814).
The separation mechanism is explained in the following. Suppose the PAM signal input in the circuit of Fig.10-4 is at point (A) of Fig. 10-5 in terms of time axis, then IC802 pin (5) is at "H" and pin (6) at "L", therefore S1 turns ON and S2 OFF. Accordingly, the signal at poin A of input PAM signal passes through S1 and is delivered to IC805 pin (1) (Lch OUT). In this case, S3 is OFF and S4 is ON, therefore the input PAM signal is not delivered to IC805 pin (1) (Rch OUT), and the previous state (signal at point C) is held by C812. Next, suppose the PAM signal is at point B in terms of time axis, then the operations of S1 - S4 at point A are reversed. So, the signal at B of PAM signal is delivered to IC806 pin (1) (Rch OUT), while IC805 pin (1) (Lch OUT) holds the previous state (signal at point A).

L.P.F./Buffer Amp Circuit

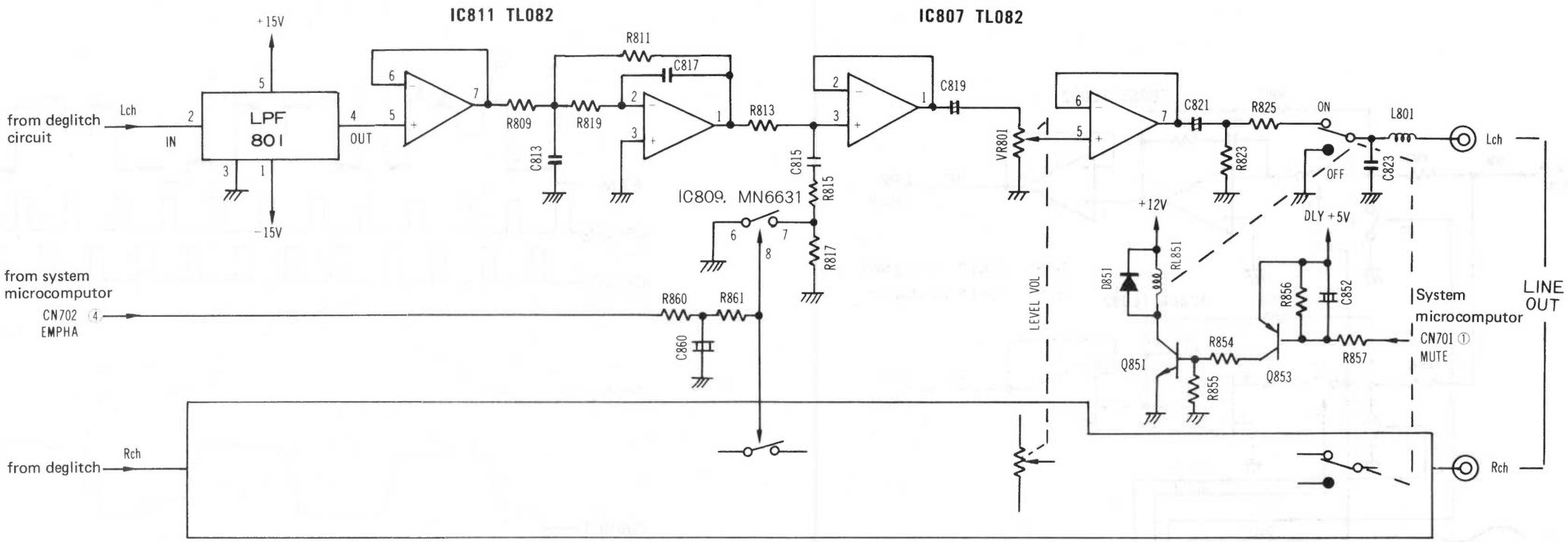


Fig. 10–6. L.P.F Buffer circuit

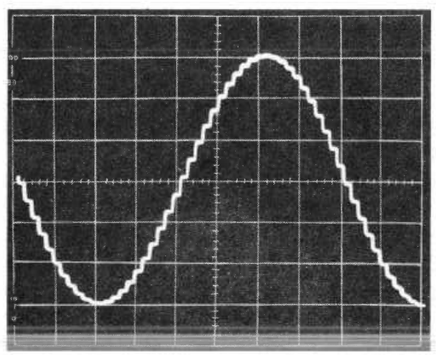


Fig. 10–7. LPF801②pin input waveform

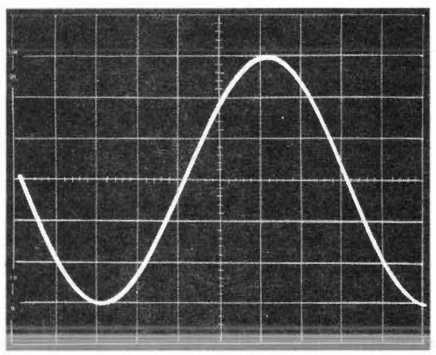


Fig. 10–8. IC811①pin output waveform

The signal output from deglitch circuit is of stepped waveform as in Fig. 10-7, therefore it is attenuated by over 20 kHz by the low pass filter circuit consisting of LPF801 and IC811 and is changed back to the original recorded audio signal as in Fig. 10-8 and is delivered to LINE OUT after impedance change by IC807.
IC807 (analog switch), C815 and R815 set up a de-emphasis circuit that is controlled with the emphasis signal of system microcomputer (MN1564). When the emphasis control data contained in Q channel of the disk is "0001", CN702 pin (4) goes "H" to de-emphasize the output signal delivered to IC811 pin (1).
RL851 (relay), Q851 and 853 set up a muting circuit that is controlled with the mute signal of system microcomputer and DLY+5V. DLY+5V becomes +5 V about 140 ms after power switch ON. Mute signal is at "L" in play mode but at "H" in other modes, turning RL851 (relay) OFF.

11. Operation control circuit

11–1. Role of operation control circuit

A great merit of CD is that random access is possible. Using control signal recorded in the disc, it is able to access the munite and second as well as tune No.

* SL-P10 was able to access the unit of second. It is further able to access the position up to the unit of frame (1/75 sec.) on the control signal.

Unlike the stylus of a conventional analog player, CD reads signal by use of laser beam.

Therefore, an optical servo circuit is built into the system, and various servo timings are required for correct application of laser spot to the specified position. The operation control circuit works as a control center for the whole system.

11–2. Configuration of operation control circuit

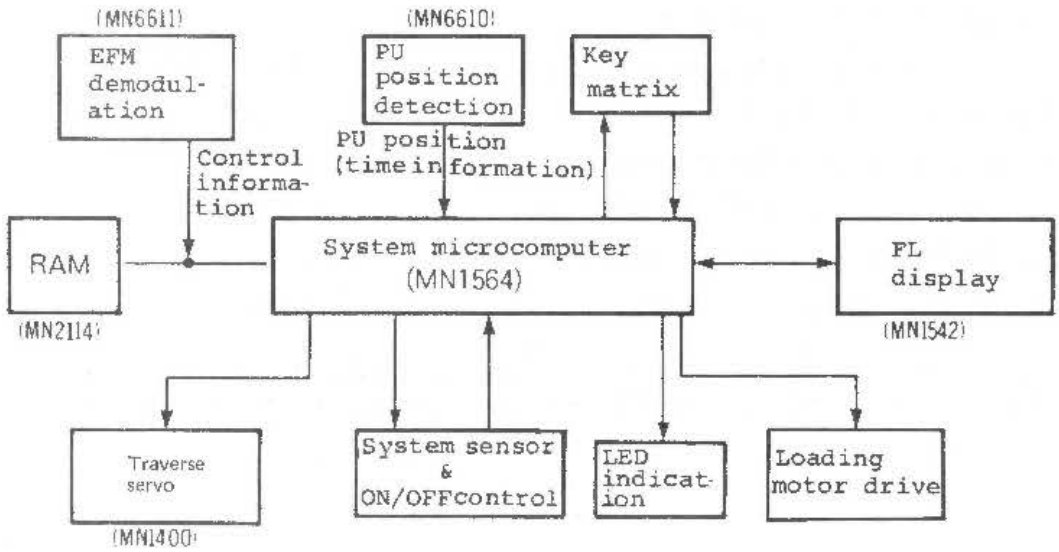


Fig. 11-1 Block diagram of operation control circuit

The block diagram of operation control circuit is shown in Fig. 11-1.

The operation control circuit has system microcomputer (MN 1564) as the main component. LSI MN6611 demodulates control information from EFM data and transfers it to system microcomputer (and RAM).

MN6610 converts PU position into time information.

The system microcomputer uses these signals to control the traverse servo microcomputer (MN1400) thus operating the random access and controlling the display microcomputer (MN 1542) to display the play time and bar graph.

Also, there are sensor and timing ON/OFF signals as follows:

° Sensor

Disc check (DISC ON)	Confirming the insertion of disc into holder.
Innermost periphery detection (LMT SW)	Confirming PU in the innermost position of disc.
RF check (RF ON)	Confirming RF signal played back from PU.

° Timing ON/OFF signal

Laser ON & turntable rotation	(LD ON / TT ON)
Focus servo ON command	(FO ON)
Tracking servo ON command	(TR ON)
Track jump direction command	(J.F/R)
Muting relay ON/OFF command	(MUTE)
Emphasis ON/OFF command	(EMPHA)

There are also key matrix and LED indicating functions. The pin functions of MN1564 are shown in Table 11-1.

11–3. Operation control circuit operation

Key matrix circuit

The configuration of key matrix is shown in Fig. 11–2. The key matrix includes 6 scan outputs (P12, P13 and P60 - P63) and 4 key inputs (P70 - P73).

OPEN/SHUT is the microswitch in the loading mechanism that determines whether door is open or closed.

All the others are the keys on the front panel. HI is a 2-step key of forward (▶▶) and reverse (◀◀) of Search and it is ON when the key is depressed to high speed mode.

* In high-speed mode of search (▶▶), both FWD and HI are ON. In low-speed mode, only FWD is ON.

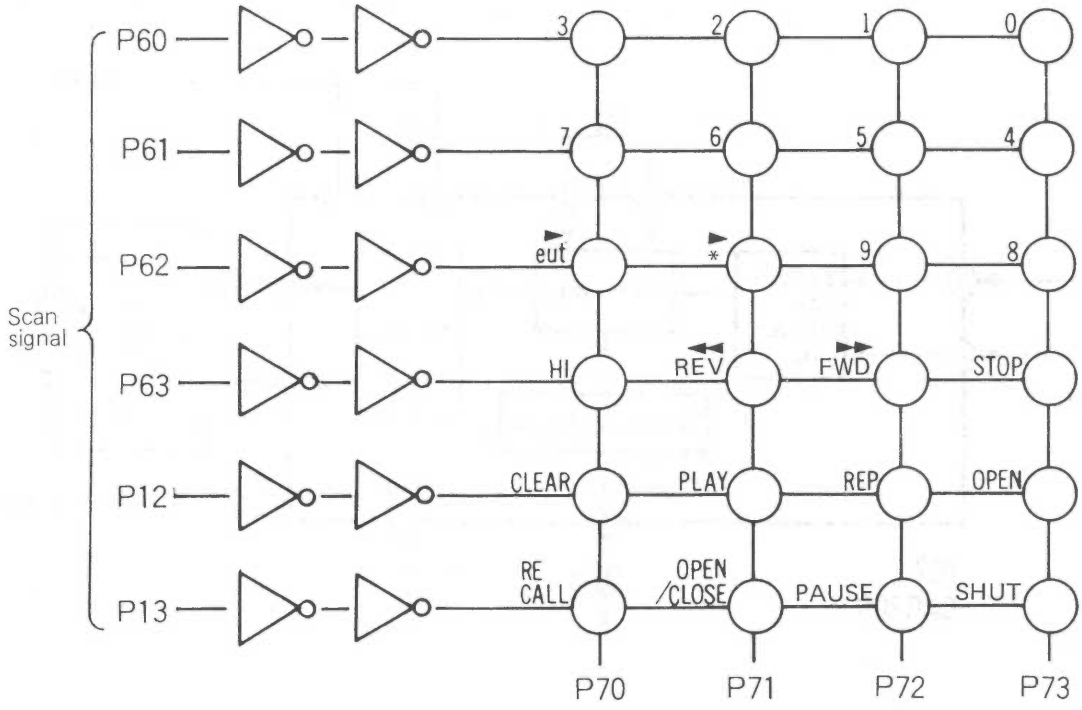


Fig. 11-2 Key matrix

Door motor drive circuit

The motor drive circuit is shown in Fig. 11-3.

IC7 (BA6209) is a drive IC.

The door can be operated by OPEN/CLOSE key.

"L" signal enters IC7 pin (5) in OPEN mode, then the voltage is 0 V at (P02) pin (2) and 8 V at pin (10).

"L" signal enters IC7 pin (6) in CLOSE mode, then the voltage is 8 V at (P03) pin (2) and 0 V at pin (10).

SL-P10 has auto loading function, and delivers CLOSE signal (P03) when disc sensor (refer to P96) is operated.

The loading mechanism is shown in Fig. 11-4.

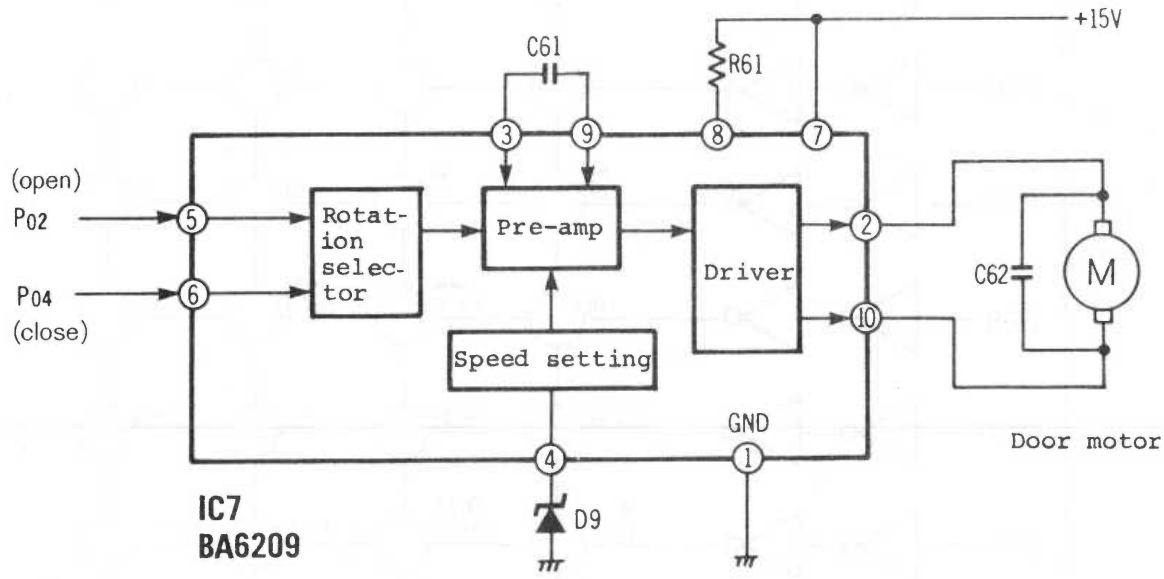


Fig. 11-3 Door motor drive circuit

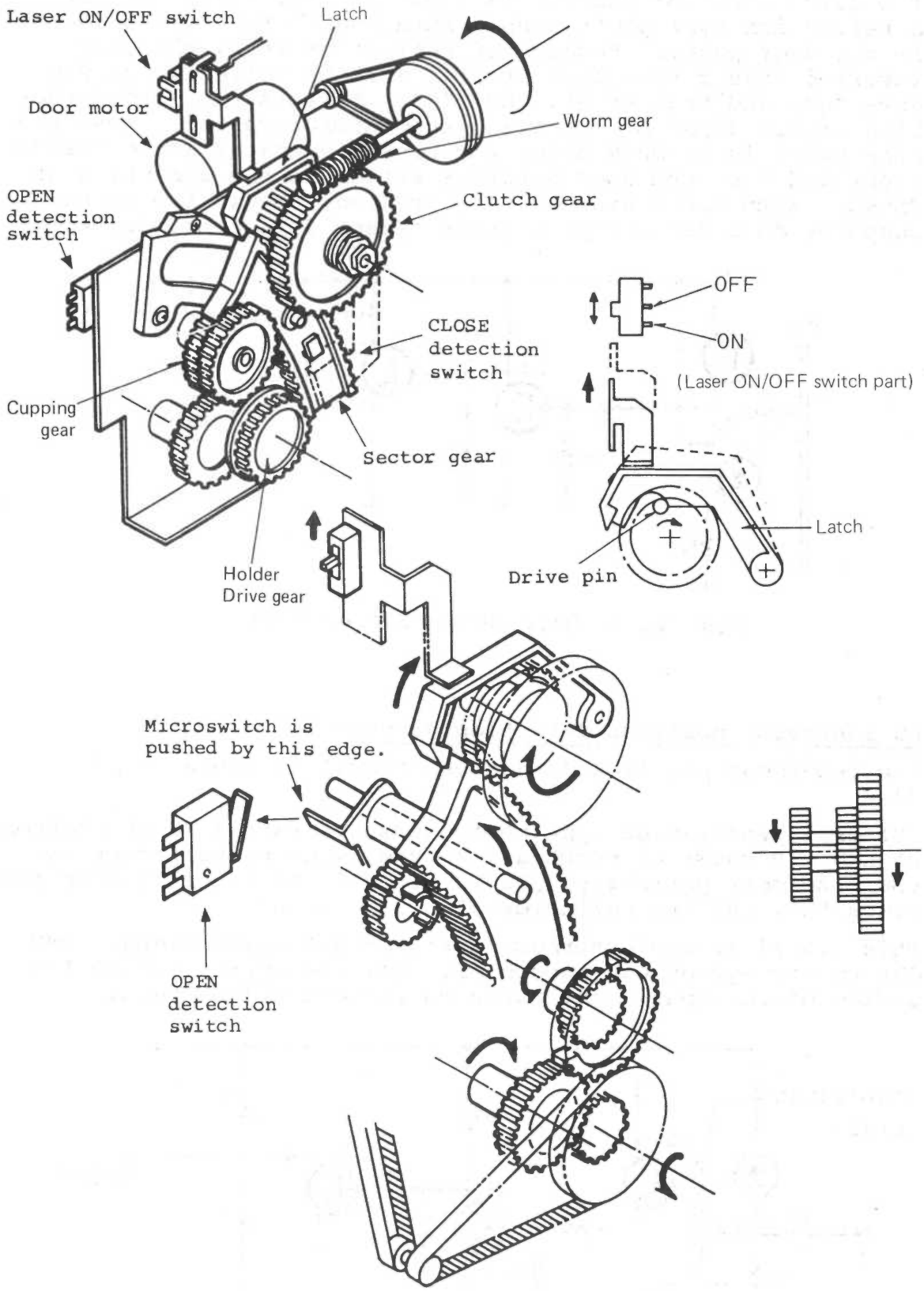


Fig. 11-4 Loading mechanism

Disc detection circuit

The disc detection circuit is shown in Fig. 11-5. PC2 is a reflection type photo sensor attached to the disc holder in the door panel. Because of reflection type, the disc inserted causes base bias to Q14, and the collector of Q14 goes "L", and that of Q15 goes "H". This is the disc detection signal (DISC ON) to the system microcomputer. When the door panel is in OPEN mode, the sensor operates (disc insertion) and then the door motor is driven in the direction of CLOSE. When the sensor is not operated, the system microcomputer does not accept signals except for open/close key.

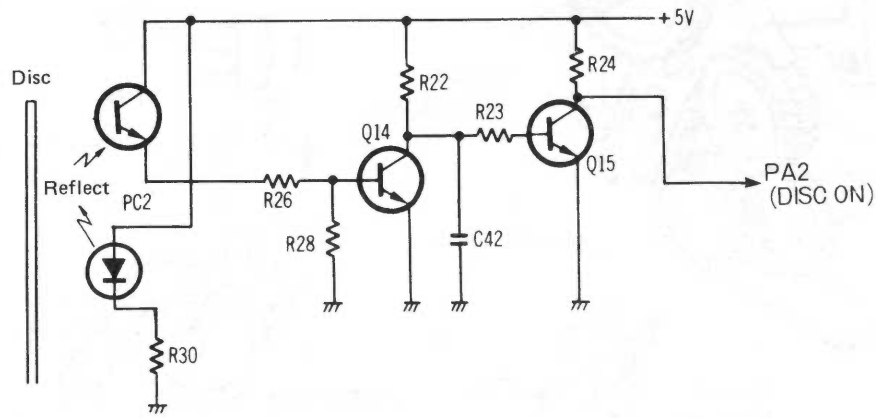


Fig. 11-5 Disc detection circuit

PU innermost position detection circuit

The innermost position detection circuit is shown in Fig. 11-6.

PC1 is a penetration type photo sensor attached to the bottom of LED. Because of penetration type, when pickup comes to the innermost periphery, Q12 is cut off and its collector becomes "H", and the collector of Q13 goes "L".

This signal is the innermost position detecting signal (LMT ON) to the system microcomputer. All the operations of the system microcomputer are based on the detection signal.

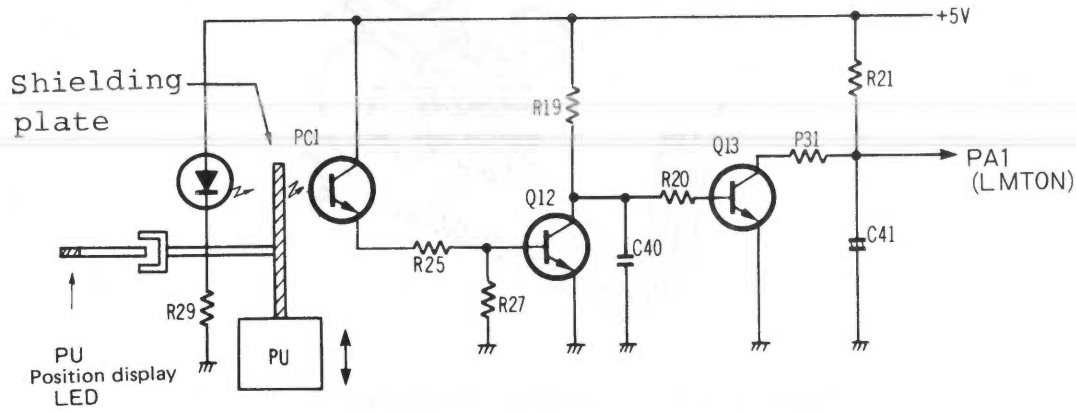


Fig. 11-6 PU innermost position detection circuit

Data transfer from MN6610 to system microcomputer

The data transferred from MN6610 to system microcomputer MN1654 are converted into time information for PU position. The data line on the circuit is the arrow-marked part shown in Fig. 11-8. This line is the bus line.

The operation of MN6610 is explained in the following. The inside block is shown in Fig. 11-9. Step pulses from traverse microcomputer (MN1400) are appplied to pins (7), (8) (SNSA, SNSB). The pulses are up-counted in forward direction and down-counted in reverse direction by the 10-bit counter. Also, the inner-most position detection signal is at pin (9) (LMT SW) and the counter operation starts with this signal.

The contents of the counter indicate the PU position but it is better to convert them into time information for random access or display, therefore ROM is used for data conversion. The output of ROM is taken out as 16-bit data, and the detail is shown below.

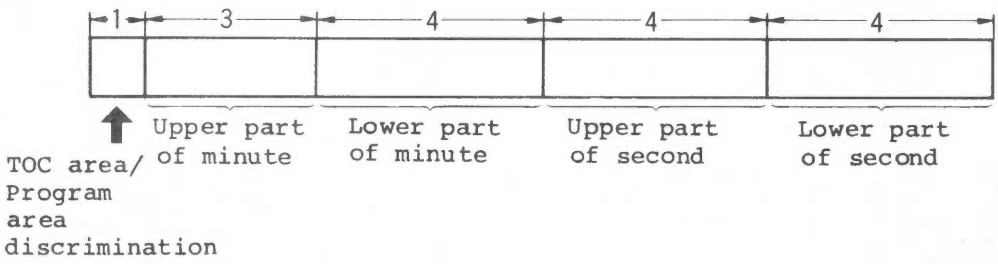


Fig. 11–7

The multiplexer has a function to deliver the 16-bit data separately 8 bits each. When pin (2) (DISABL) is at "L", pin (3) (SELECT) is at "L" and the minute data, at "H", then the data are transferred from pins (13) - (20) (D01 - D08) to system microcomputer.

When pin (2) (DISABL) is at "H", pins (13) - (20) (Do) parts are of high impedance to cope with bus line.

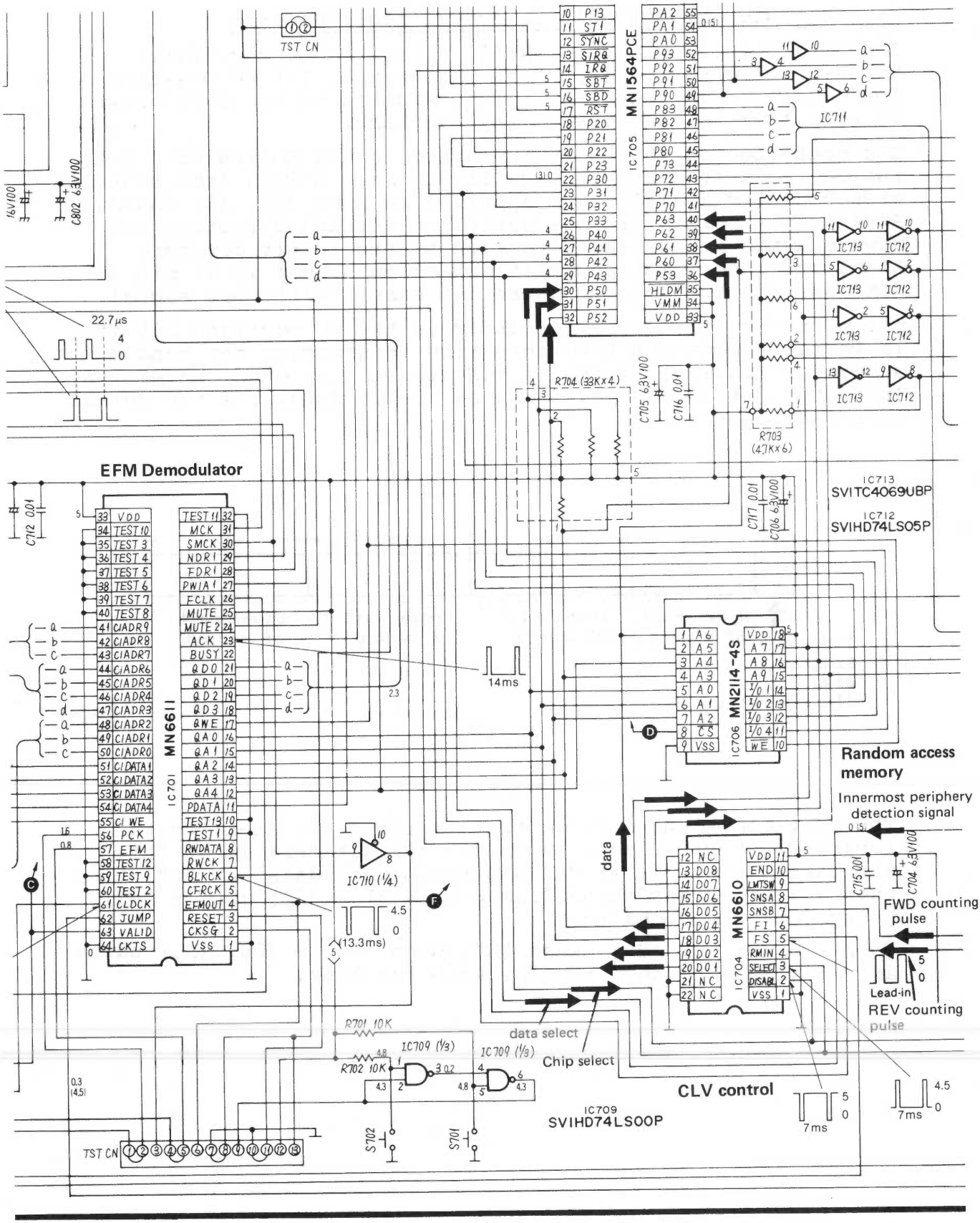


Fig. 11-8 Data transfer from MN6610

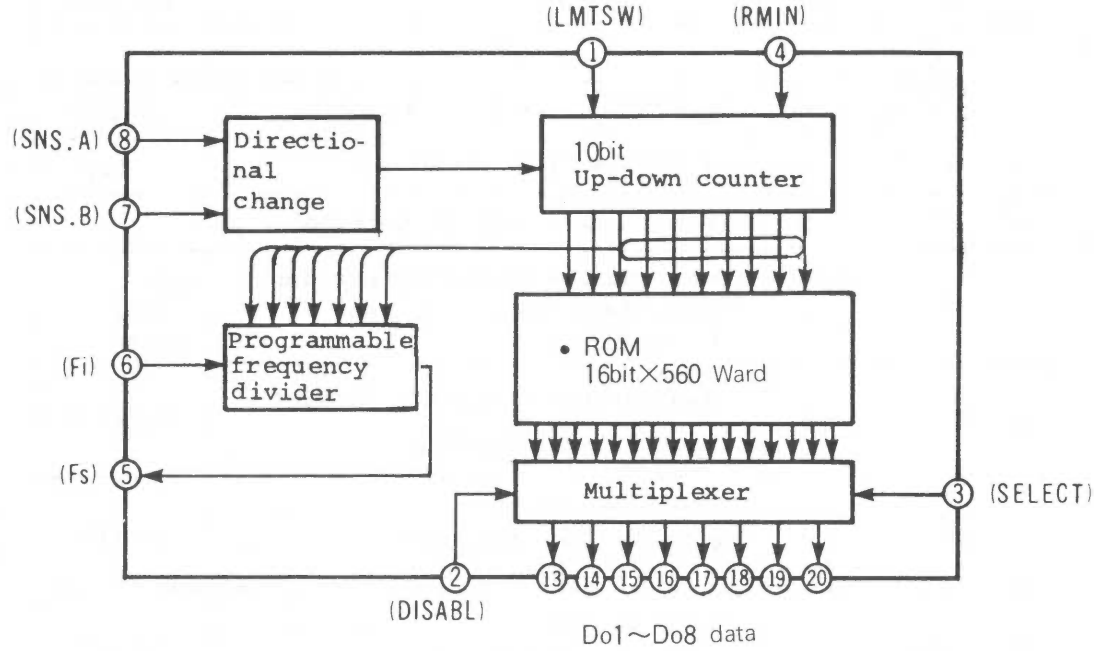


Fig. 11-9 Block diagram of MN6610

MN6610 is equipped with a programmable frequency divider. It generates standard frequency FS of rough servo in CLV. (Refer to CLV servo on P 48.)

Frequency (254.22 kHz) divided from X'tal in demodulation LSI is at pin (6) (FI), and the division ratio of frequency divider is set by use of the output of the 10-bit counter. Therefore, frequency being reversely proportional to disc diameter can be taken out of pin (5) (FS).

No.	Name of pin	I/O	Function	Remarks
1	VSS	I	GND	
2	DISABLE	I	Effective with chip select at "L"	MN1564
3	SELECT	I	Do part output selection	MN1564
4	RMIN	I	10-bit count initial setting	
5	FS	0	Programmable frequency divider output fs = fi/20 x R (mm) (R → radius)	CLV rough servo
6	FI	I	Programmable frequency divider input fi = 254.22 kHz	MN6612
7	SNSB	I	Count-down input ↓ count when SNSA "H"	MN1400
8	SNSA	I	Count-up input ↓ count when SNSB "H"	MN1400
9	LMTSW	I	10-bit count load input Effective at "L"	
10	END	0	End detection output by 10-bit counter End output at "L"	MN1564
11	VDD	I	Power supply +5 V	
12	NC		———	
13	D_{08}	0	Pu position data after changing to the time by ROM. (biteserial)	MN1564
20	D_{01}		D_{08}……MSB D_{01}…LSS	
21	NC		———	
22	NC		———	

	D_{08} ~ D_{05}	D_{04} ~ D_{01}
SELECT"L"	Upper "Min"	Lower "Min"
SELECT"H"	Upper "Sec"	Lower "Sec"

Table 11–2. The pin function of MN6610

Data transfer from MN6611 to system microcomputer

The data transferred from MN6611 to system microcomputer are control Q data demodulated from EFM data.

The control Q data are not directly transferred but they are once written into external RAM IC706 (MN2114) and are read by system microcomputer as needed.
(Both data and address lines are bus line system.) The data transfer between MN6611 -- external RAM -- system microcomputer is performed as in Fig. 11-10.

Writing ..... refer to Fig. 11-11.

° Control Q data enters MN2114 -- pins (11) - (14) (I/01 - I/04) from MN6611 -- pins (18) - (21) (QD0 - QD3).

° Address signals enter MN2114 -- pins (3) - (7) (A0 - A4) from MN6611 -- pins (12) - (16) (QA0 - QA4).

° Writing signal enters MN2114 -- pin (10) ($\overline{WE}$) from MN6611 -- pin (17) (QWE). ($\overline{WE}$ ... writes at "L".)

Reading ..... refer to Fig. 11-12.

° Control Q data enters MN1564 -- pins (26) - (29) (P40 - P43) from MN2114 -- pins (11) - (14) (I/01 - I/04).

° Address signals enter MN2114 -- pins (3) - (7) (A0 - A4) from MN1564 -- pin (9) (P12) and pins (30) - (32), (36) (P50 - P53).

° MN2114 -- pin (10) ($\overline{WE}$) is at "H" during reading.

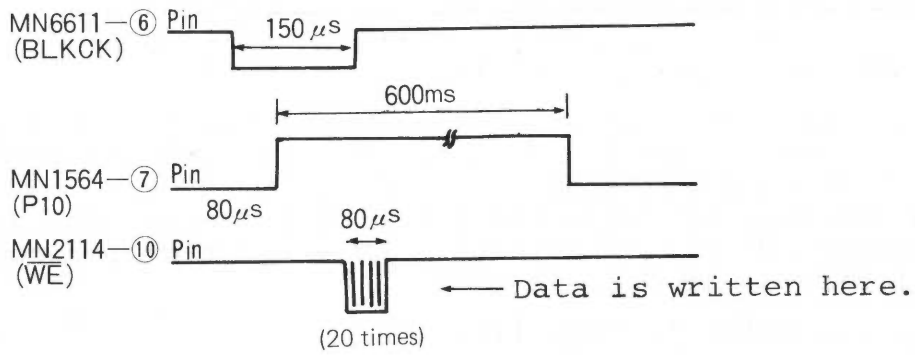
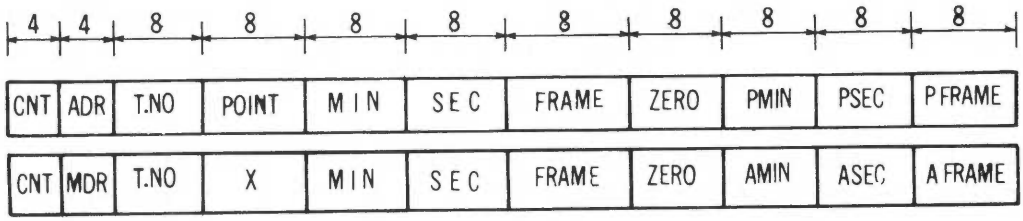


Fig. 11-10 Data transfer timing



NO	RAM address		Data
1	0	0	CNT
2	0	1	ADR
3	0	2	T.NO(U)
4	0	3	T.NO(L)
5	0	4	POINT(U) / X(U)
6	0	5	POINT(L) / X(L)
7	0	6	MIN(U)
8	0	7	MIN(L)
9	0	8	SEC(U)
10	0	9	SEC(L)
11	0	A	FRAME(U)
12	0	B	FRAME(L)
13	0	C	ZERO(U)
14	0	D	ZERO(L)
15	0	E	PMIN (U) / AMIN (U)
16	0	F	PMIN (L) / AMIN (L)
17	1	0	PSEC(U) / ASEC(U)
18	1	1	PSEC(L) / PSEC(L)
19	1	2	P FRAME(U) / A FRAME(U)
20	1	3	P FRAME(L) / A FRAME(L)

Table 11-3 RAM address signal

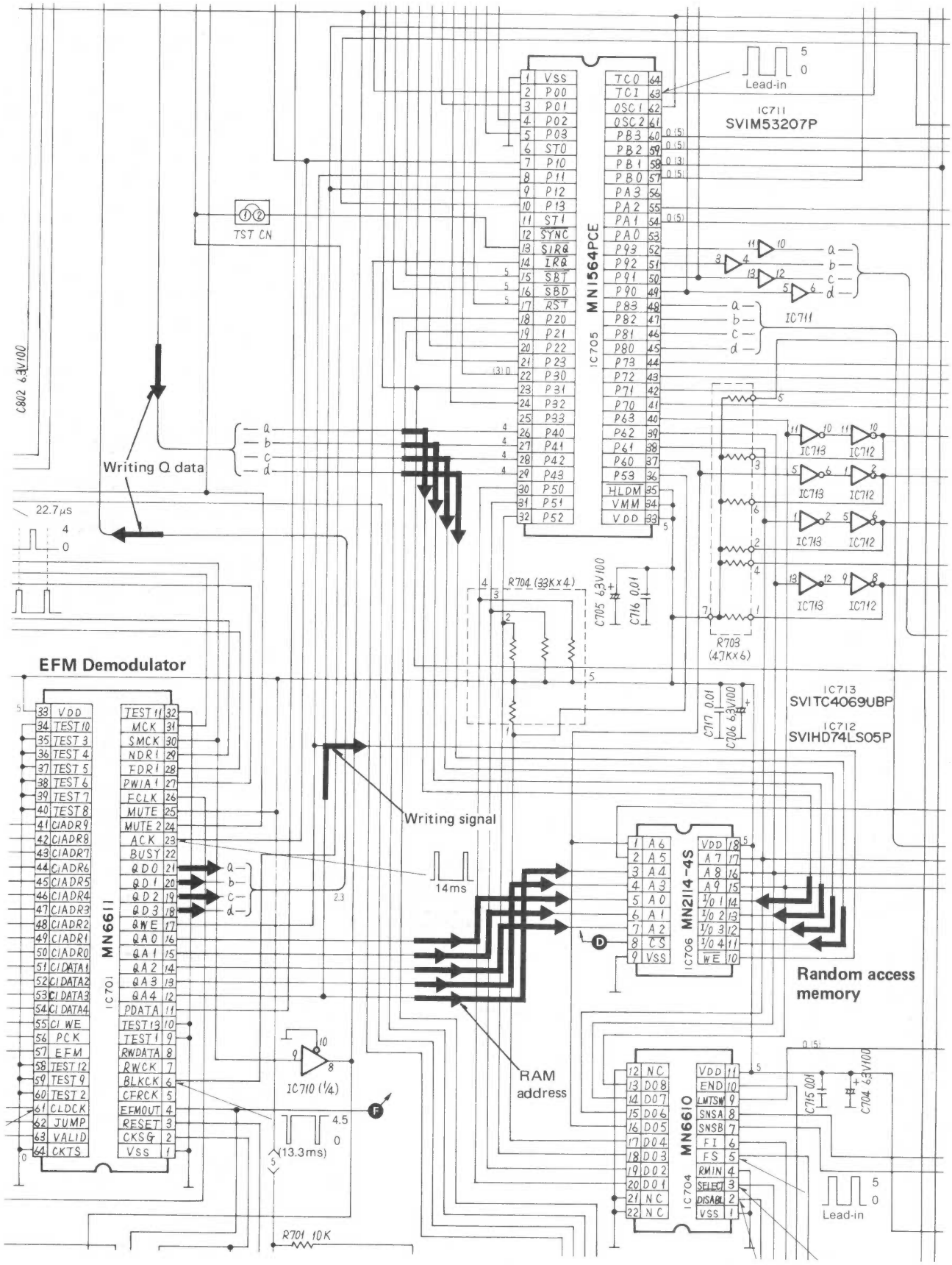


Fig. 11-11 Q data wriring

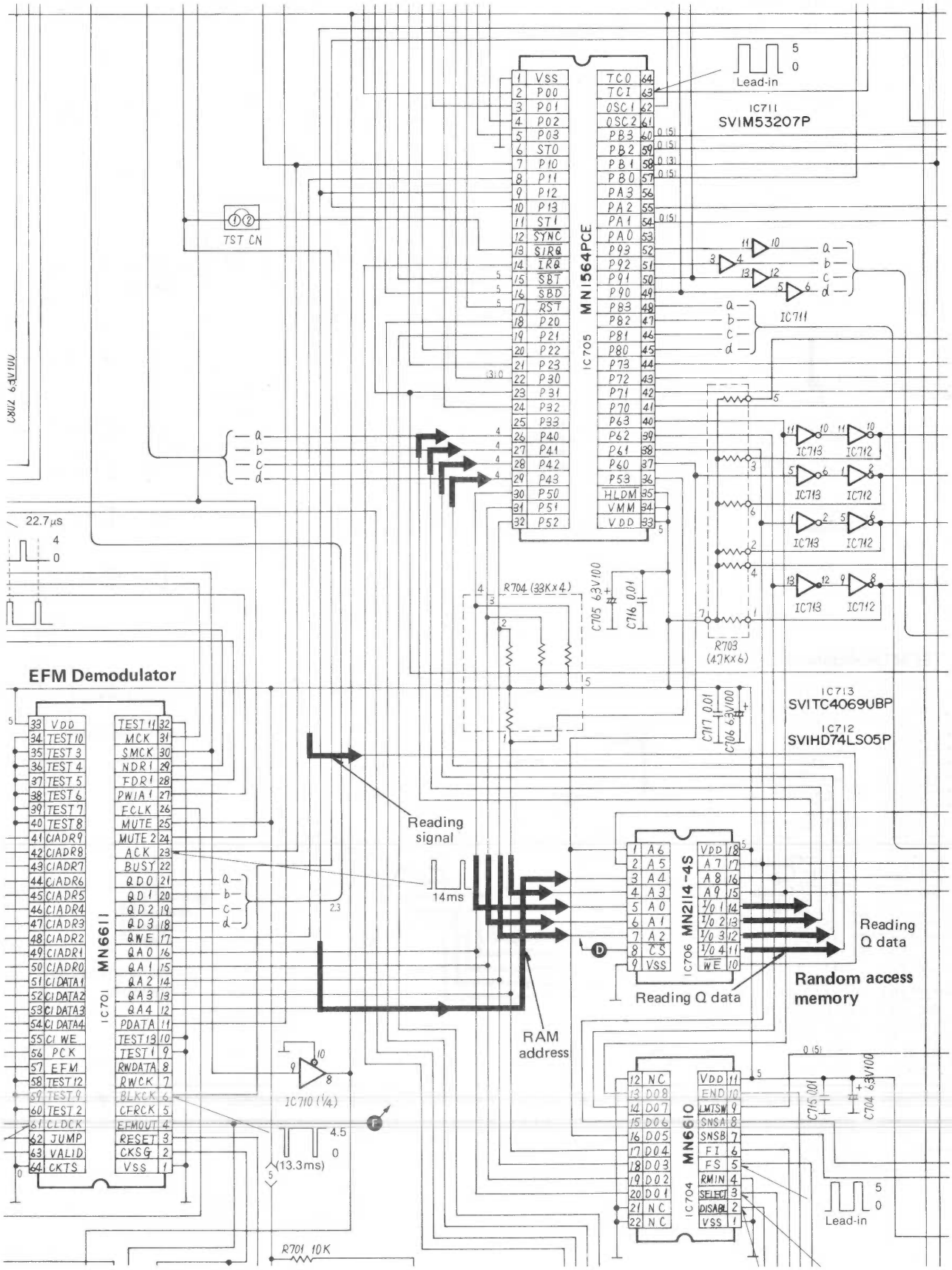


Fig. 11-12 Q data reading

Data transfer between system microcomputer and MN1542

Data transfer (MN1564 → MN1542) for display and its reception check signal (MN1542 → MN1564) are handled between system microcomputer and display microcomputer (MN1542).

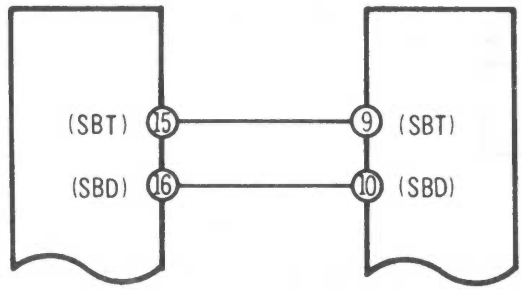


Fig. 11-13 Data transfer between MN1564 and MN1542

The input/output terminals between system and display microcomputers are shown in Fig. 11-13.

SBT ..... Data transfer clock (MN1564 → MN1542)
Check signal transfer clock (MN1542 → MN1562)

SBD ..... Data transfer line (MN1564 → MN1542)
Check signal line (MN1542 → MN1564)

Transfer method and timing

One unit for data transfer is 8 bits.

Check signal ("H" for all 8 bits) is delivered from display microcomputer every 8-bit data from system microcomputer.

The timing is shown in Fig. 11-14.

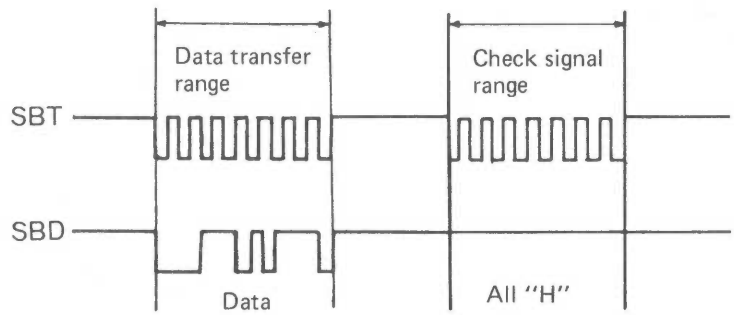


Fig. 11-14 Transfer timing

— Contents of data transferred —

The upper 4 bits of serial 8 bits are given for data No., and the lower 4 bits, for data.

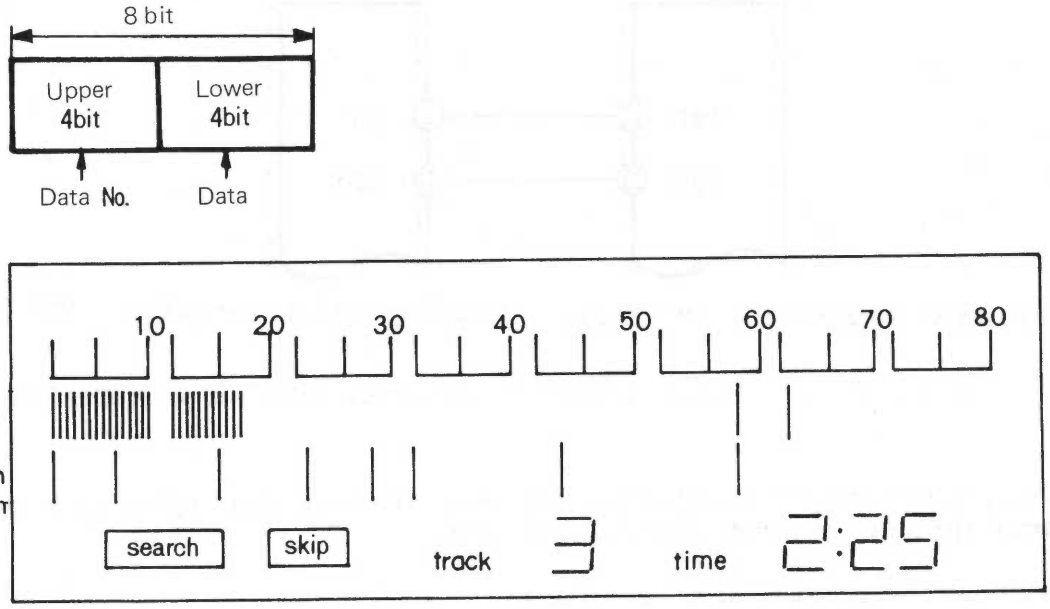


Fig. 11-15 Display

Display data in SL-P10 are as follows:

(1) 7-segment (track & time) display
(2) Time bar code display
(3) Location bar code display
(4) Selection bar code display
(5) Read-out position display
(6) Selection erase (end of 1 step of program)
(7) Group progam "-" display
(8) Program overflow "F" display
(9) Program error "E" display
(10) SKIP display
(11) SEARCH display
(12) SKIP·SEARCH display
(13) Complete erase (in EJECT mode)
(14) Selection and 7-segment erase (stop, clear)
(15) 7-segment erase (recall)

The following is the explanation of 7-segment display and time bar code display.

(1) 7-segment display

DATA NO	0	1	2	3	4	5	6
DATA	0	T.NO (U)	T.NO (L)	MIN (U)	MIN (L)	SEC (U)	SEC (L)

(2) Time bar code display

DATA NO	0	1	2
DATA	1	MIN (U)	MIN (L)

Data transfer for 7-segment display is in 7 bytes, and that for time bar code display, in 3 bytes.

When the upper 4 bits of the initial 8 bits are "0", the following 6 bytes are the data for 7-segment display if the lower 4 bits are also "0". In this case, if the lower 4 bits are "1", then the following 2 bytes are the data for time bar code display.

Other data are shown below.

(3) Location display

DATA NO	0	1	2
DATA	2	MIN (U)	MIN (L)

(4) Selection display

DATA NO	0	1	2
DATA	3	MIN (U)	MIN (L)

(5) Read out display

DATA NO	0	1	2
DATA	4	MIN (U)	MIN (L)

(6) Selection erase

DATA NO	0	1	2
DATA	5	MIN (U)	MIN (L)

(7) " — " Display

DATA NO	0	1
DATA	A	0

(8) " F " Display

DATA NO	0	1
DATA	A	1

(9) " E ' Display

DATA NO	0	1
DATA	A	2

(10) SKIP Display

DATA NO	0	1
DATA	A	3

(11) SEARCH Display

DATA NO	0	1
DATA	A	4

(12) SKIP/SEARCH Erase

DATA NO	0	1
DATA	A	5

(13) All Earse (EJECT)

DATA NO	0	1
DATA	A	6

(14) Selection 7 segments Earse

DATA NO	0	1
DATA	A	7

(15) 7 segments Earse

DATA NO	0	1
DATA	A	8

The operation after the display microcomputer (MN1542) receives the data is explained in the section of display circuit (refer to page 140.)

Pin functions of MN1564

No	Name of Pin	I/O	Function	Remarks
1	VSS	I	GND	
2	P00		P DATA ... control P signal.	
3	P01	O	Focus ON/OFF, ON at "H", OFF at "L"	Timing ON/OFF signal
4	P02		Door open command. Open at "L".	
5	P03		Door close command. Close at "L".	
6	STO		—	×
7	P10	O	ACK ... Q data writing timing.	
8	P11		WE ... Q data reading mode setting.	
9	P12	I / O	Q DADR ... Q data reading address signal output.	Bus line
10	P13		KSS ... Key matrix scan signal output.	
11	STI		—	×
12	$\overline{\text{SYNC}}$		—	
13	$\overline{\text{SIRQ}}$	I	BLOCK CK (Q data)	MU6611
14	$\overline{\text{IRQ}}$		END ... Disc program area over signal. Over at "L".	MU6610
15	$\overline{\text{SBT}}$	I / O	DISP CK ... Dispaly trans-fer clock input/ output.	Display micro-computer MN1542
16	$\overline{\text{SBD}}$		DISP DATA ... Display trans-fer data input/ output.	
17	$\overline{\text{RST}}$	I	RESET Effective at "L".	
18	P20	O	SELECT "L" ... MIN, "H" ... SEC	MN6610
19	P21		DISABLE Data output from MN6610 at "L".	
20	P22		PAUSE ON at "L"	Timing ON/OFF signal
21	P23		REPEAT ON at "L"	
22	P30		TRACKING ON/OFF ON ... "H", OFF ... "L"	
23	P31		JUMP TIMING command ⎍ in jump mode.	
24	P32		JUMP direction command. FWD at "H", REV at "L".	
25	P33		—	×
26	P40	I / O	QD 0	Bus line
27	P41		QD 1 Control Q data	
28	P42		QD 2	
29	P43		QD 3	
30	P50	I / O	Q DADR ... Q data reading address signal output.	Bus line
31	P51		CLV 1 ... PU position time conversion data input.	
32	P52			

No	Name of pin	I/O	Functions	Remarks
33	VDD	I	Power supply +5 V	
34	VMM		+5 V	
35	HLDM		+5 V	
36	P53	I / O	Same as P50 - P52.	
37	P60		ADR ... Memory address signal output.	Bus line
38	P61		CLV 2 ... PU position time conversion data input.	
39	P62		KSS ... Key matrix scan signal output.	
40	P63			
41	P70	I	KSI 0	
42	P71		KSI 1 Key matrix signal input.	
43	P72		KSI 2	
44	P73		KSI 3	
45	P80	O	TCNT 0	Traverse mocro-computer MN1400
46	P81		TCNT 1 Traverse microcomputer mode command	
47	P82		TCNT 2	
48	P83		TCNT 3	
49	P90		Search FWD (▷▷)	LED ON
50	P91		Search REV (◁◁) ON at "L"	
51	P92		STOP	
52	P93		PLAY	
53	PA 0	I	—	×
54	PA 1		LMT ON ... Disc innermost position detection. "L" in detection mode.	Sensor
55	PA 2		DISC ON ... Disc detection. "H" ... Disc ON.	
56	PA 3		—	
57	PB 0		RF ON LDST ... RF signal detection. "H" in detection mode.	
58	PB 1	O	TT/LD ON ... Turntable & laser diode.	Timing ON/OFF signal
59	PB 2		MUTE ON ... Muting relay ON/OFF. ON at "L".	
60	PB 3		EMPHA ON ... De-emphasis SW ON/OFF. ON at "L".	
61	OSC 2		—	×
62	OSC 1	I	SMCK ... 4.32 MHz input	
63	TCI		FG ... FG input signal 64 pulses/turn.	
64	TCO	O	—	×

Table 11. 1 MN1564

System microcomputer and various timing signals

The system microcomputer delivers various timing signals according to the modes. The relations with modes are shown in Table 11-5.

No.	Traverse mode		T·CNT (to traverse micon) ㊽	㊼	㊻	㊺	LD/TT ON ㊽	FO ON ③	TR ON ㉒	J F/R ㉔	JAMP TIMING ㉓	Remarks
1	STOP		L	L	L	L	L	L	L	—	L	
2	PLAY(inner periphery)		L	L	L	H	H	H	H	—		Inner and outer peripheries are changed over at 40-min position.
3	PLAY (outer periphery)		L	L	H	L				—		
4	Manual search	Low speed FWD (inner periphery)	L	L	H	H				H	Jump pulse (Upper part of AM1N + 4) Read 2 kick forward	Manual search low speed mode is a state with FWD search key depressed 1 step during PLAY.
5		Low speed FWD (outer periphery)	L	H	L	L						
6	Low speed FWD		L	H	L	H	L	L	L	—	L	Only search key is depressed by 1 step.
7	Manual search High speed FWD		L	H	H	L	PLY + FWD_2 ····· "H" FWD_2 ····· "L"		40ms 40ms FWD_2 ····· "L"	—		° Search key is depressed 2 steps during PLAY. ° Only search key is depressed 2 steps.
8	Extra-high speed FWD		L	H	H	H			L	—		Random access (rough search)
9	PAUSE		H	L	L	L					Jump pulse 1 turn 1 kick back	1 kick back at deviation zero crossing point
10	Manual search	Low speed REV (inner periphery)	H	L	H	H	H	H	H	L	Jump pulse (Upper part of AM1N + 4) Read 3 kick back	Random access (fine search)
11		Low speed REV (outer periphery)	H	H	L	L						
12	Low speed REV		H	H	L	H	L	L	L	—	L	
13	Manual search High speed REV		H	H	H	L	PLY + REV_2 ····· "H" REV_2 ····· "L"		40ms 40ms REV_2 ····· "L"	—		
14	Extra-high speed REV		H	H	H	H	アクセス ····· "H" EJ ····· "L"		L	—		° Random access (rough search) ° EJECT return

Table 11-5 System timing signal

System operation up to TOC reading

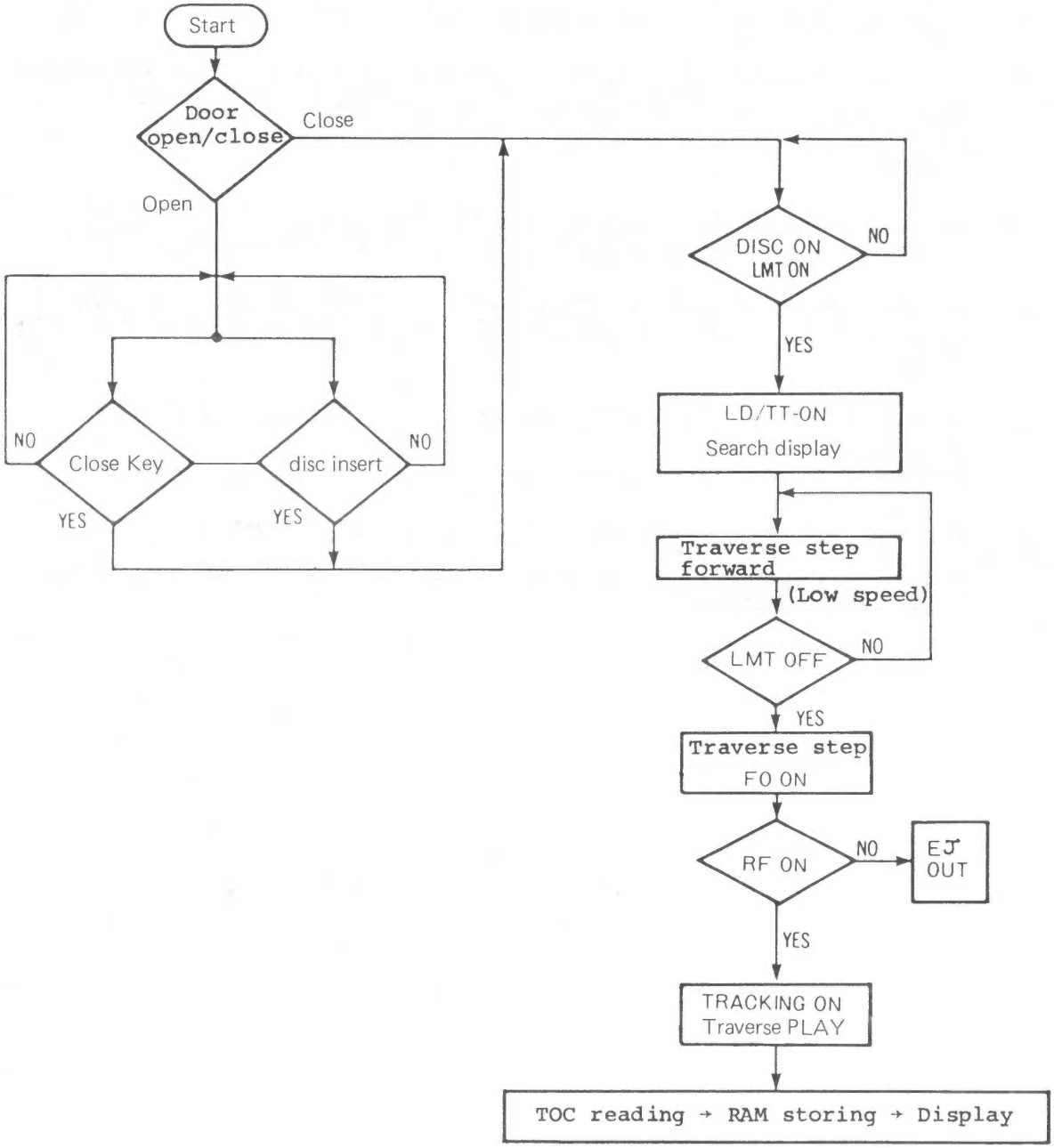


Fig. 11-16 Flow chart up to TOC reading

The operation up to TOC reading is shown in Fig. 11-16.

(1) Door open/close is done by micro-switch in key matrix.

(2) Door is closed with disc inserted or closed key depressed. LD ON and TT ON are delivered when both DISC ON and LMT ON sensor signals are received by system microcomputer.

(3) With traverse step forward and LMT OFF sensor signal confirmed, then traverse steps and FO ON is delivered.

(4) FO ON causes focus search, and with RF ON sensor signal confirmed, TR ON is delivered, shifting traverse to play mode.

(5) Servo is completed with TR ON, then TOC is read and displayed.
After TOC reading, LD/TT ON, FO ON and TR ON are OFF.

(6) During TOC reading, only PLAY key is accepted.

* Pause repeat key is also accepted but it is released on TOC display.

System operation after TOC reading

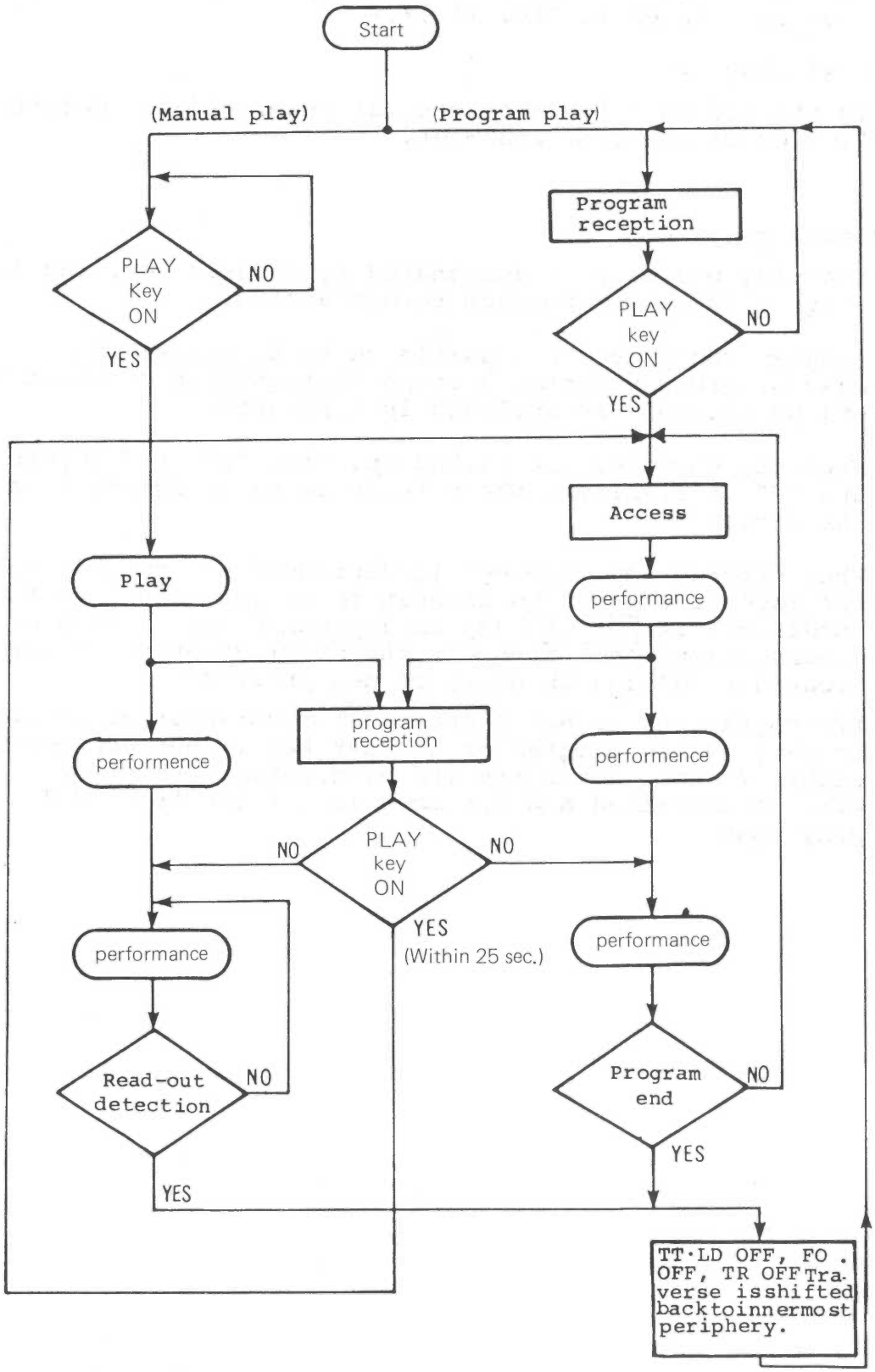


Fig. 11-17 Flow chart after TOC reading.

After TOC reading, either of manual play and program play can be used. (Refer to Fig. 11-17.)

— Manual play —

Play is started in order from the 1st tune, and is completed on detection of the last read-out.

— Program play —

(1) The play position is designated by program key, and the program is played through random access.

(2) Program reception is possible up to 63 steps. In the case of group program, 2 steps (designation of start and end positions) are included in 1 program.

(3) When the commands are filled up, then "F" is displayed. And "E" is displayed where there is no designation on the disc.

(4) When program key (10-key) is depressed during play mode, the mode is shifted to program reception mode. In this condition, if [enter] key is depressed with 1 step of program completed, then all the previous programs are cleared resulting in entry of new programs.

If program key is not depressed for consecutive 25 sec. or over during program or if PLAY key is not depressed within 25 sec. after the end of program, the program will be cancelled and the mode is shifted to manual play mode.

Random access operation

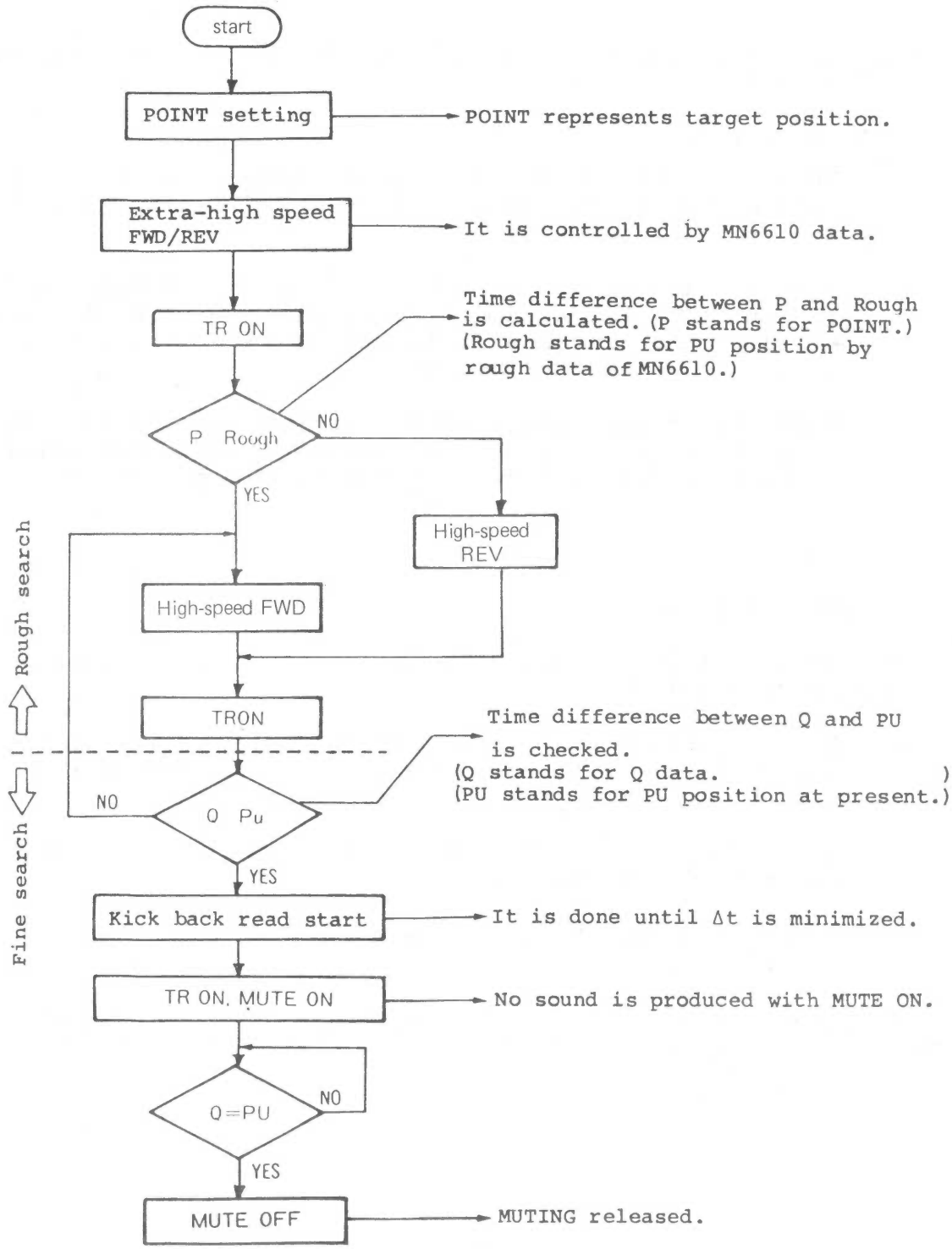


Fig. 11-18 Flow chart during random access

Random access operation includes rough search and fine search. (Refer to Fig. 11-18.)

— Rough search —

(1) Traverse is forwarded to the programmed target point (AMN, ASEC) by the data (1.25 m/s) of MN6610 in the extra-high speed mode.

(2) When it reaches the target point, it reads the Q data of disc with TR ON, and time difference ΔT is calculated, then the traverse is forwarded by $\Delta T + \alpha$ (or $\Delta T - \alpha$ in REV mode) in the same mode.

* At that point, the target position is very much close to the PU position, PU position is away from target position for kick back in the next time research.

— Fine search —

(3) Again Q data is read with TR ON, and time difference Δt is calculated.

(4) In kick back 1 read operation equivalent to Δt (unit in sec) x 3, it is repeated until Δt is minimized and Q data is nearer than target position.

(5) When the position in step (4) has been decided, MUTE ON is delivered with TR ON.

* Then the system is in play mode but no sound is produced.

(6) When Q data has reached the target position, audio signal is delivered with MUTE OFF. (Muting relay released.)

12. FL Display circuit

12–1. Function of FL display

FL display circuit performs TOC display, play position display and play time display to the data transferred from system microcomputer.
Bar graph and 7 segments are used for display.

12–2. Configuration of FL display

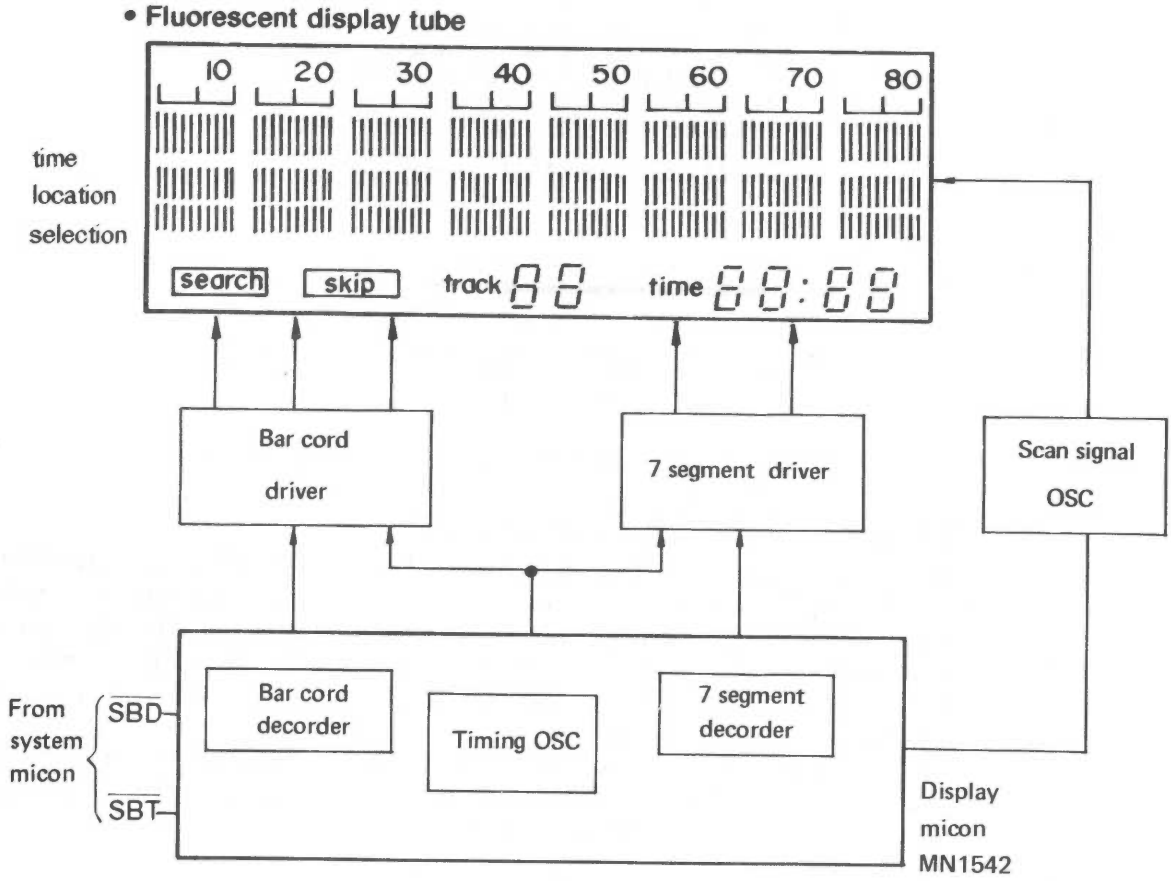


Fig. 12–1. FL Display Block Diagram

12–3. FL display circuit operation

FL display tube

A dynamic system with 8 divisions as in Fig. 12-2 is employed for FL display.

1G - 8G are the grid terminals of FL tube, which are controlled by scan signals.
The display data are connected to each bar graph, 7 segments and other display terminal plates from display microcomputer. The FL tubes light up when both grit and plate are at "H" timing.

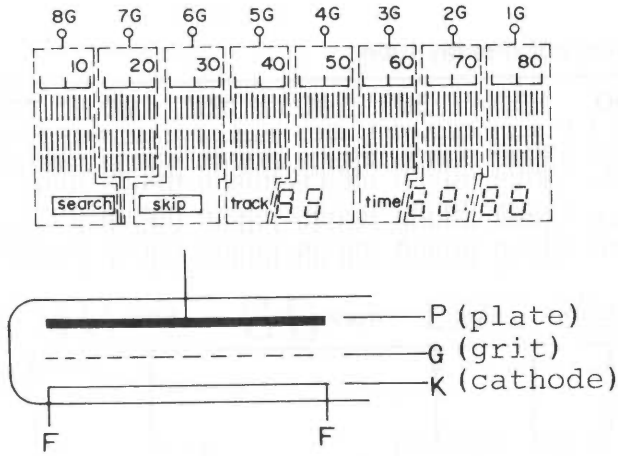


Fig. 12-2 Structure of FL tube

Scan signal generating circuit

The scan signals for dynamic lighting are 8 signals (1G - 8G), and the reference signal is generated by decoding the 3-bit signal at the counter output terminal in display microcomputer. The circuit is shown in Fig. 12-3.
The timings of IC501 (MN1542) pins 25 - 28 (P30 - P33) are shown in Fig. 12-4.
IC502 (MN4028) is BCD decoder that operates as in Table 12-1. IC511 and 512 are open collector type buffers that control the grit of FL tube.

IN PUT				OUT PUT
D	C	B	A	"H"
L	L	L	L	Q_0
L	L	L	H	Q_1
L	L	H	L	Q_2
L	L	H	H	Q_3
L	H	L	L	Q_4
L	H	L	H	Q_5
L	H	H	L	Q_6
L	H	H	H	Q_7

Table 12–1. MN4028 operation

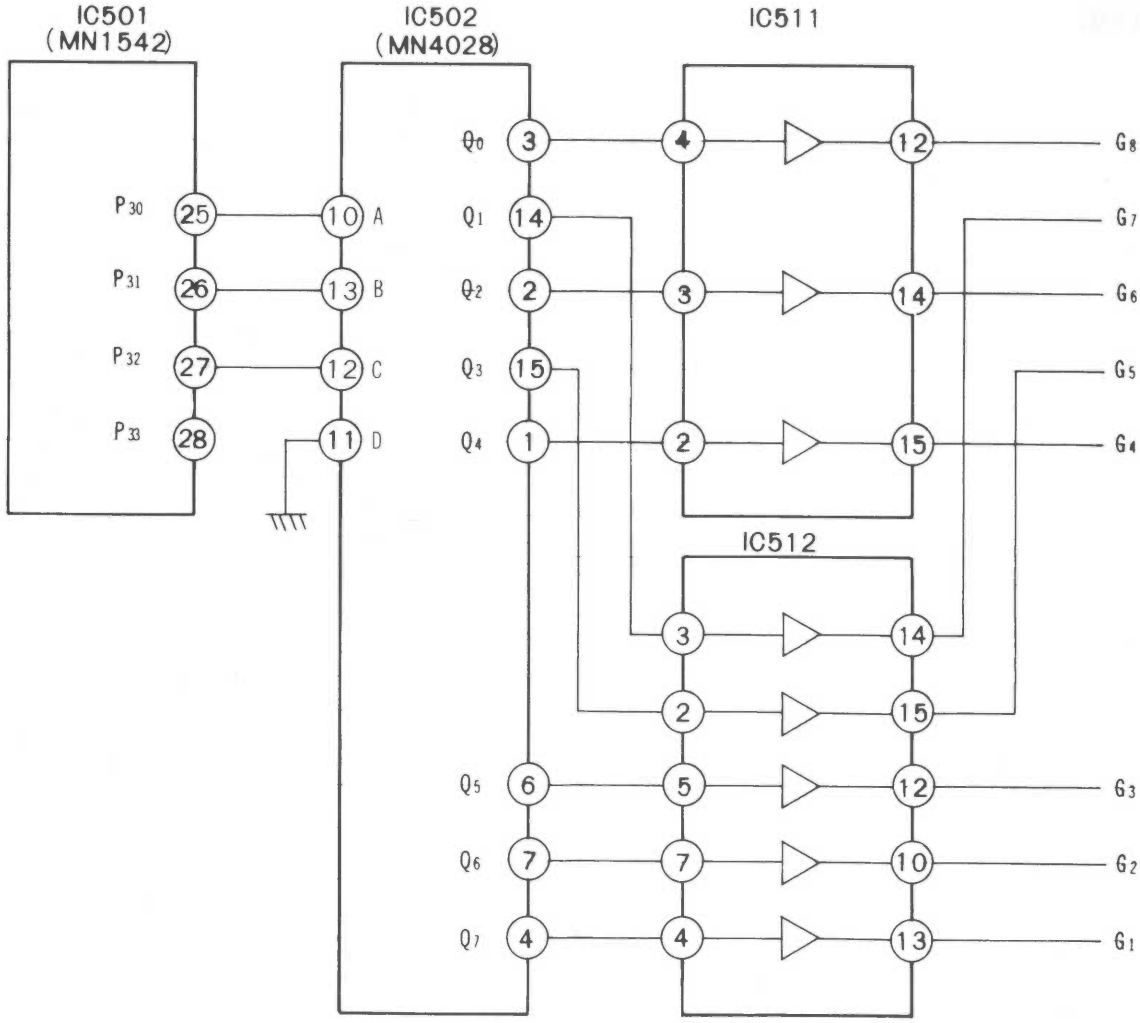


Fig. 12–3. Scan signal OSC circuit

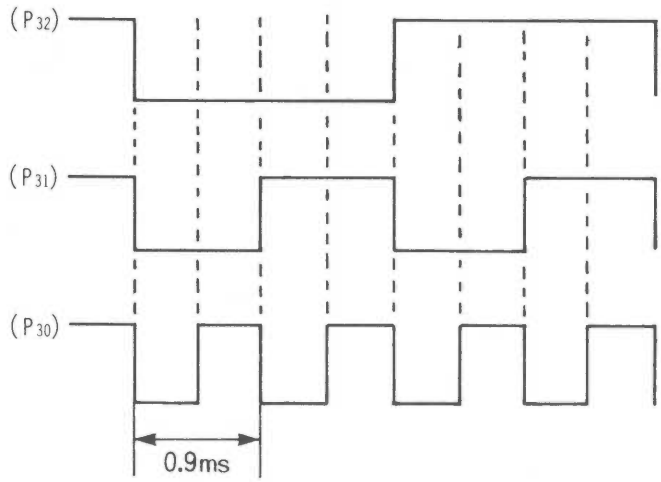


Fig. 12–4. Display Micon counter out-put

– MEMO –

Bar code display circuit

The data for bar code display are time (PU position) location (tune head position) and selection (memory position). These are capable of minute-by-minute display on the scale.

Each display is given by dynamic lighting, and the display microcomputer is provided with terminals corresponding to 10 bars.
P0 port, P1 port, P20 and P21 ports correspond to bars 1 - 10. Bar lighting data are switched in timing of P33, P23 and P22.

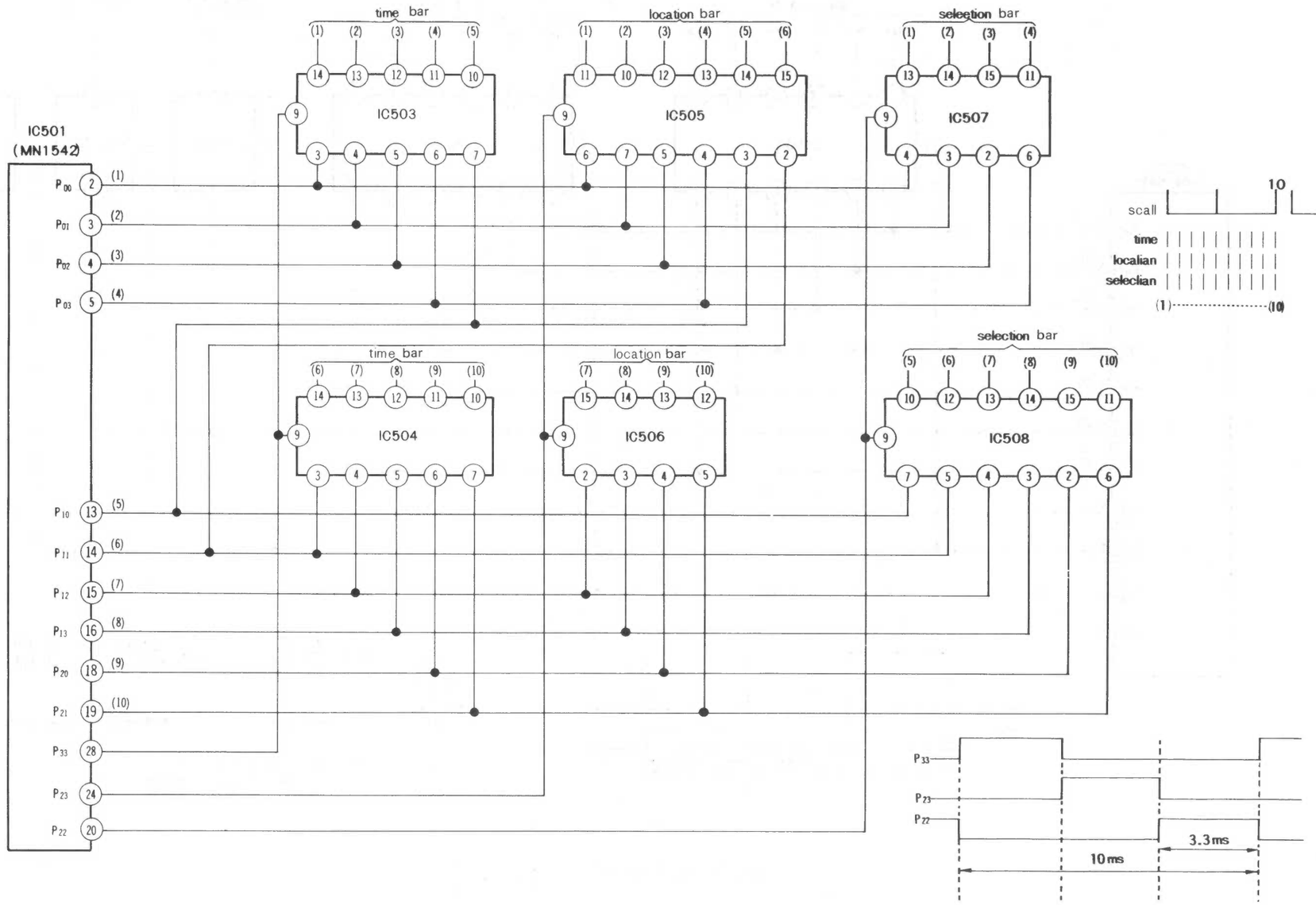


Fig. 12–5. Bar cord Drive circuit

7-segment display circuit

The data for 7-segment display are track (tune number) and time (tune time).
The outputs of 7-segment data are delivered from P4, P51 and P52 ports, and the lighting data are switched by P33 and P23.

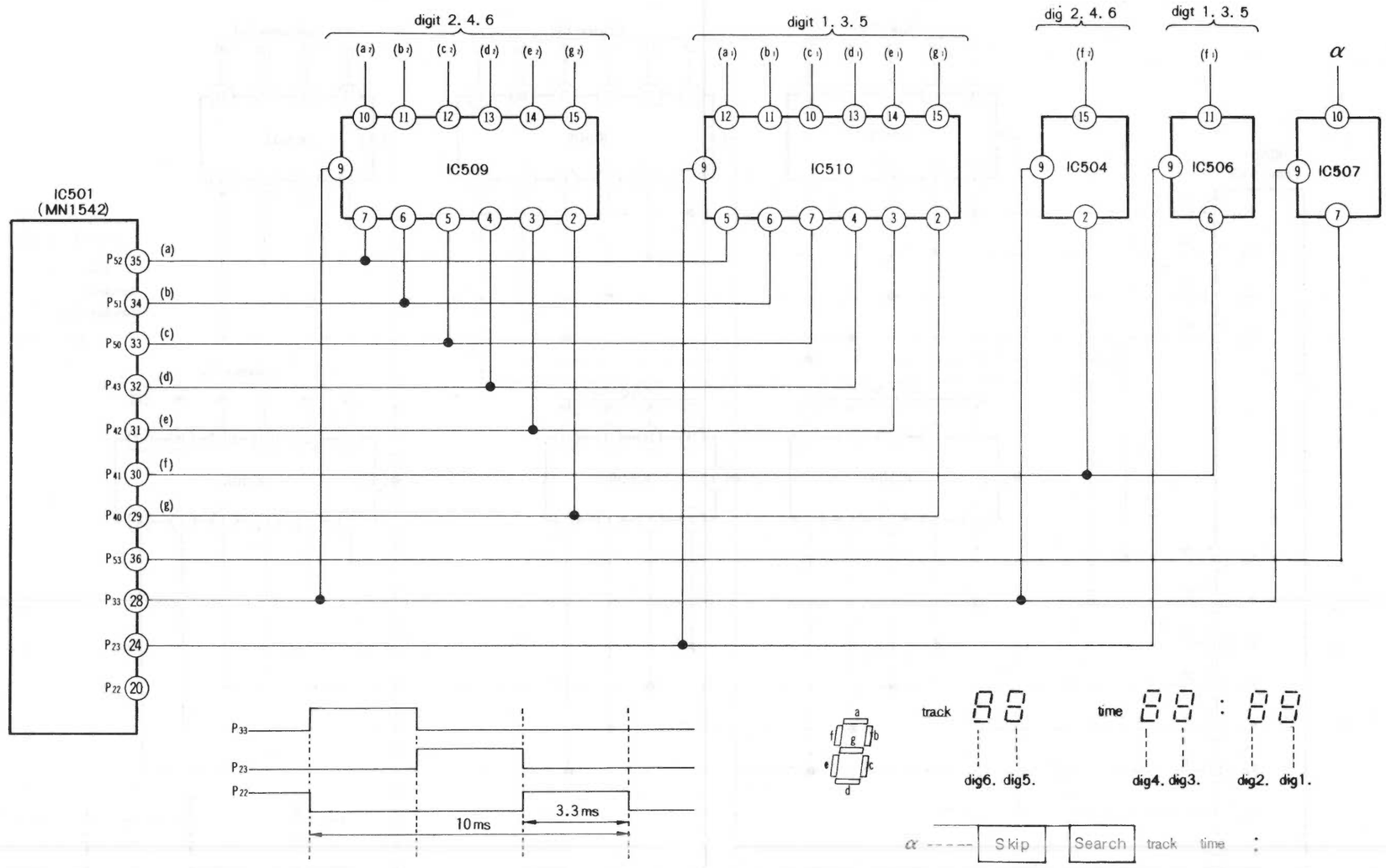
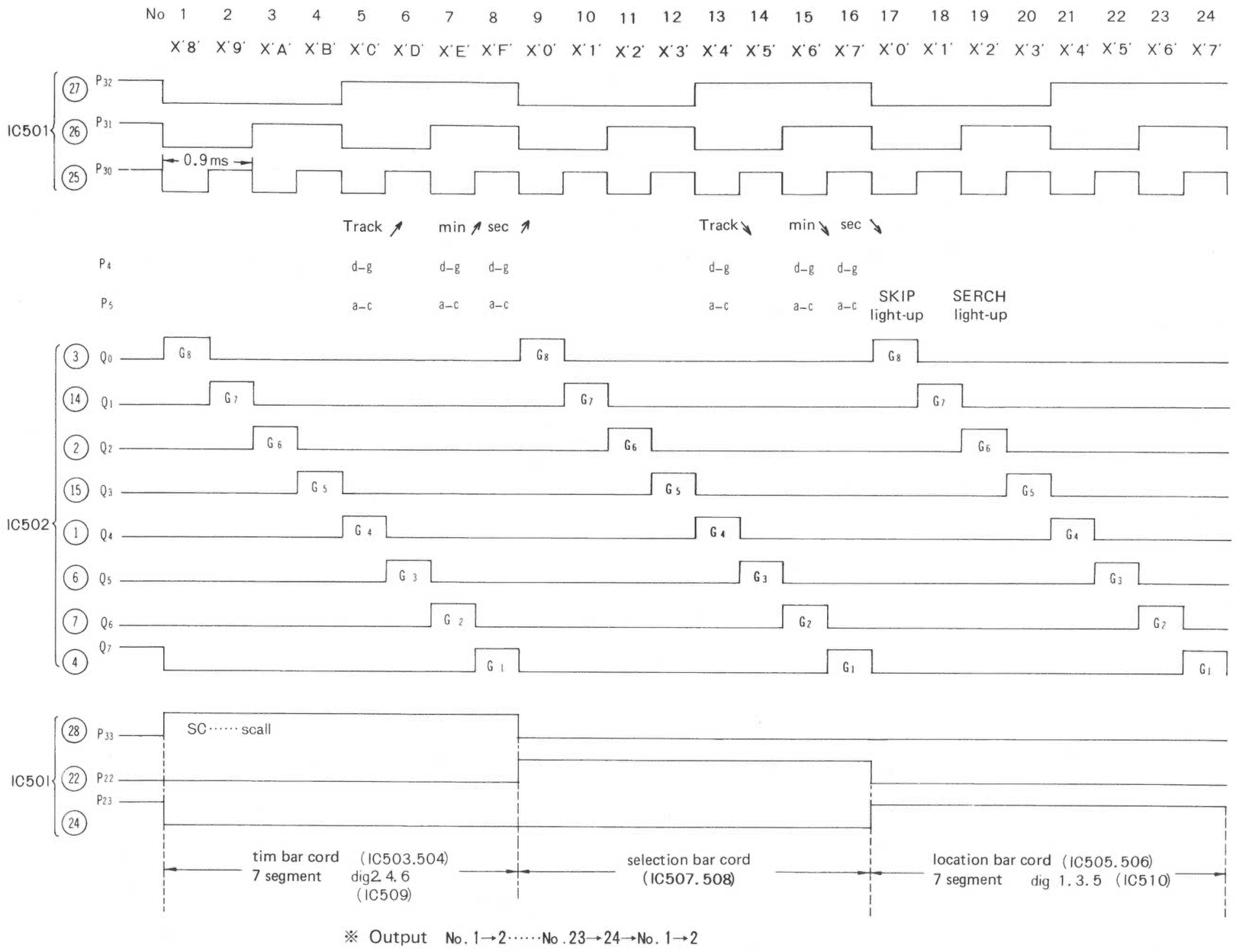


Fig. 12–6. 7 segment drive circuit

Timing chart



※ Output No. 1→2·····No .23→24→No. 1→2

12–7. Timing chart

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