

Digital Equalizer

DEQ7

SERVICE MANUAL



DEQ7

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IMPORTANT NOTICE

This manual has been provided for the use of authorized Yamaha Retailers and their service personnel. It has been assumed that basic service procedures inherent to the industry, and more specifically Yamaha Products, are already known and understood by the users, and have therefore not been restated.

WARNING: Failure to follow appropriate service and safety procedures when servicing this product may result in personal injury, destruction of expensive components and failure of the product to perform as specified. For these reasons, we advise all Yamaha product owners that all service required should be performed by an authorized Yamaha Retailer or the appointed service representative.

IMPORTANT: The presentation or sale of this manual to any individual or firm does not constitute authorization, certification, recognition of any applicable technical capabilities, or establish a principle-agent relationship of any form.

The data provided is believed to be accurate and applicable to the unit(s) indicated on the cover. The research, engineering, and service departments of Yamaha are continually striving to improve Yamaha products. Modifications are, therefore, inevitable and changes in specification are subject to change without notice or obligation to retrofit. Should any discrepancy appear to exist, please contact the distributor's Service Division.

WARNING: Static discharges can destroy expensive components. Discharge any static electricity your body may have accumulated by grounding yourself to the ground buss in the unit (heavy gauge black wires connect to this buss).

IMPORTANT: Turn the unit **OFF** during disassembly and parts replacement. Recheck all work before you apply power to the unit.

This product uses a lithium battery for memory back-up.

WARNING: Lithium batteries are dangerous because they can be exploded by improper handling. Observe the following precautions when handling or replacing lithium batteries.

- Leave lithium battery replacement to qualified service personnel.
- Always replace with batteries of the same type.
- When installing on the PC board, solder using the connection terminals provided on the battery cells. Never solder directly to the cells. Perform the soldering as quickly as possible.
- Never reverse the battery polarities when installing.
- Do not short the batteries.
- Do not attempt to recharge these batteries.
- Do not disassemble the batteries.
- Never heat batteries or throw them into fire.

ADVARSEL!

Lithiumbatteri. Eksplosionsfare.

Udskiftning må kun foretages af en sagkyndig, og som beskrevet i servicemanualen.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Freq. Response	20 Hz—20 kHz
Dynamic Range	86 dB
Harmonic Distortion	0.03% max. @ 1 kHz

INPUT

Number of Channels	Balanced × 2 (XLR type)
Nominal Level	+4 dBm/−20 dBm
Impedance	10 k-ohms
Level Control	Rotary, continuous
Level Monitor	8-segment LED

DIGITAL

Number of Channels	2
Sampling Freq.	44.1 kHz
Quantization	16 bits
Digital I/O	Yamaha-format digital input × 1 Yamaha-format digital output × 1

OUTPUT

Number of Channels	Balanced × 2 (XLR type)
Nominal Level	+4 dBm/−20 dBm
Impedance	600 ohms

MEMORY

Presets (ROM)	1—30
User Memory (RAM)	31—90 (Battery Backup)

MIDI CONTROL	Memory selection (1—90) by MIDI program change number. MIDI foot control message controls filter sweep in programs 9 and 10. Bulk dump & receive.
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FRONT PANEL

Keys	PARAMETER, DELAY/ LEVEL, DATA INCREMENT, DATA DECREMENT, STORE, RECALL, MEMORY INCREMENT, MEMORY DECREMENT, UTILITY, PROTECT ON/OFF, BYPASS
Jacks	FOOT CONTROL, BYPASS
Display	16 char. × 2 line backlit LCD 2-digit 7-segment LED

REAR PANEL

INPUT/OUTPUT Jacks	INPUT L, INPUT R, OUTPUT L, OUTPUT R, DIGITAL IN, DIGITAL OUT
Level Selectors	INPUT LEVEL (+4 dB/−20 dB), OUTPUT LEVEL (+4 dB/ −20 dB)
MIDI Terminals	IN, OUT

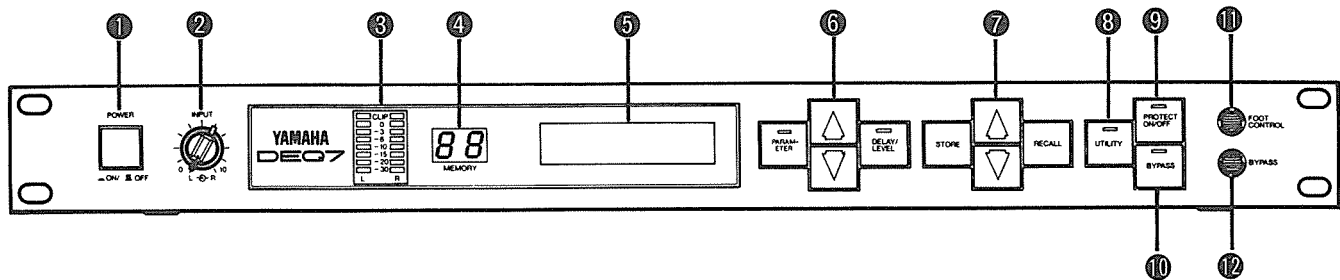
GENERAL

Power Supply	U.S. & Canada: 120 VAC, 30 W General Model: 220—240 VAC, 30W
Dimensions (W × H × D†)	480 × 45.2 × 285 mm (18-7/8'' × 1-3/4'' × 11-1/4'')
Weight	3.7 kg (8.2 lbs)

*0 dB = 0.775 Vr.m.s.

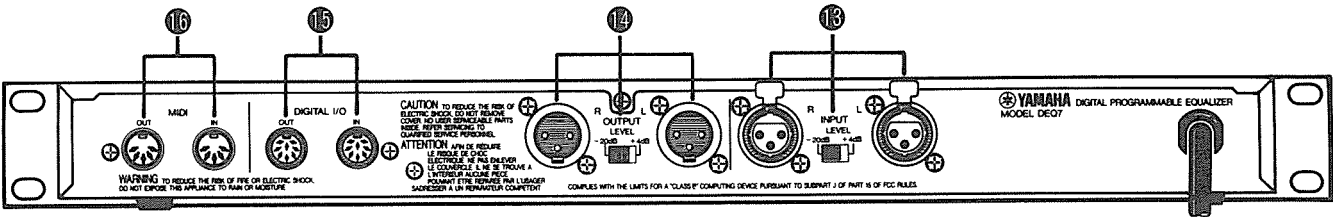
PANEL LAYOUT

● Front Panel



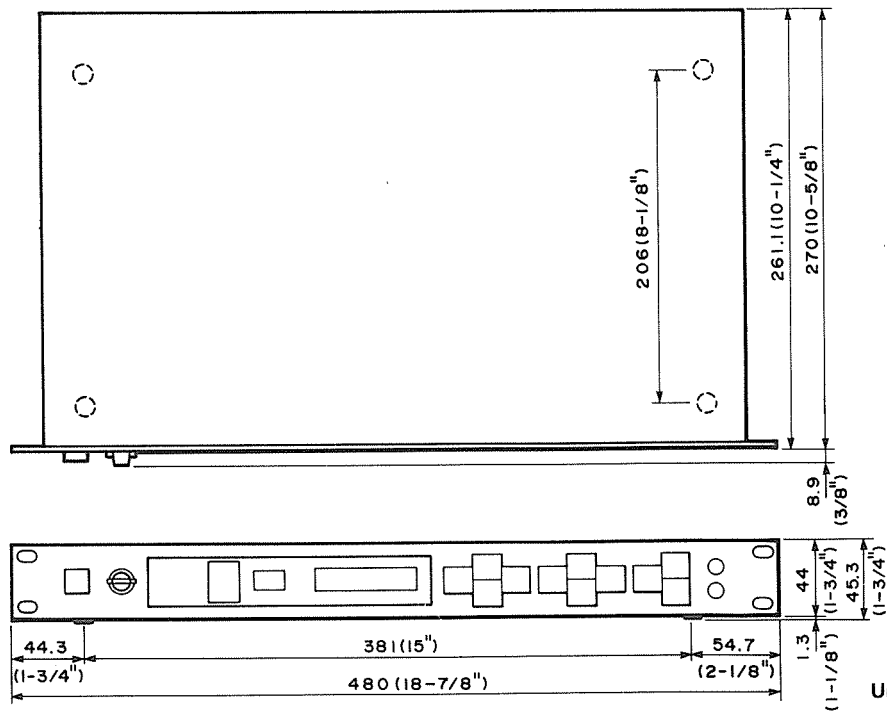
- ① POWER Switch
- ⑤ LCD Panel
- ⑨ PROTECT ON/OFF Key
- ② L/R INPUT Level Control
- ⑥ Parameter Editing Keys
- ⑩ BYPASS Key
- ③ Level Meters & CLIP Indicators
- ⑦ Program Selection & Storage Keys
- ⑪ FOOT CONTROL Jack
- ④ LED Memory Number Display
- ⑧ UTILITY Key
- ⑫ BYPASS Jack

● Rear Panel



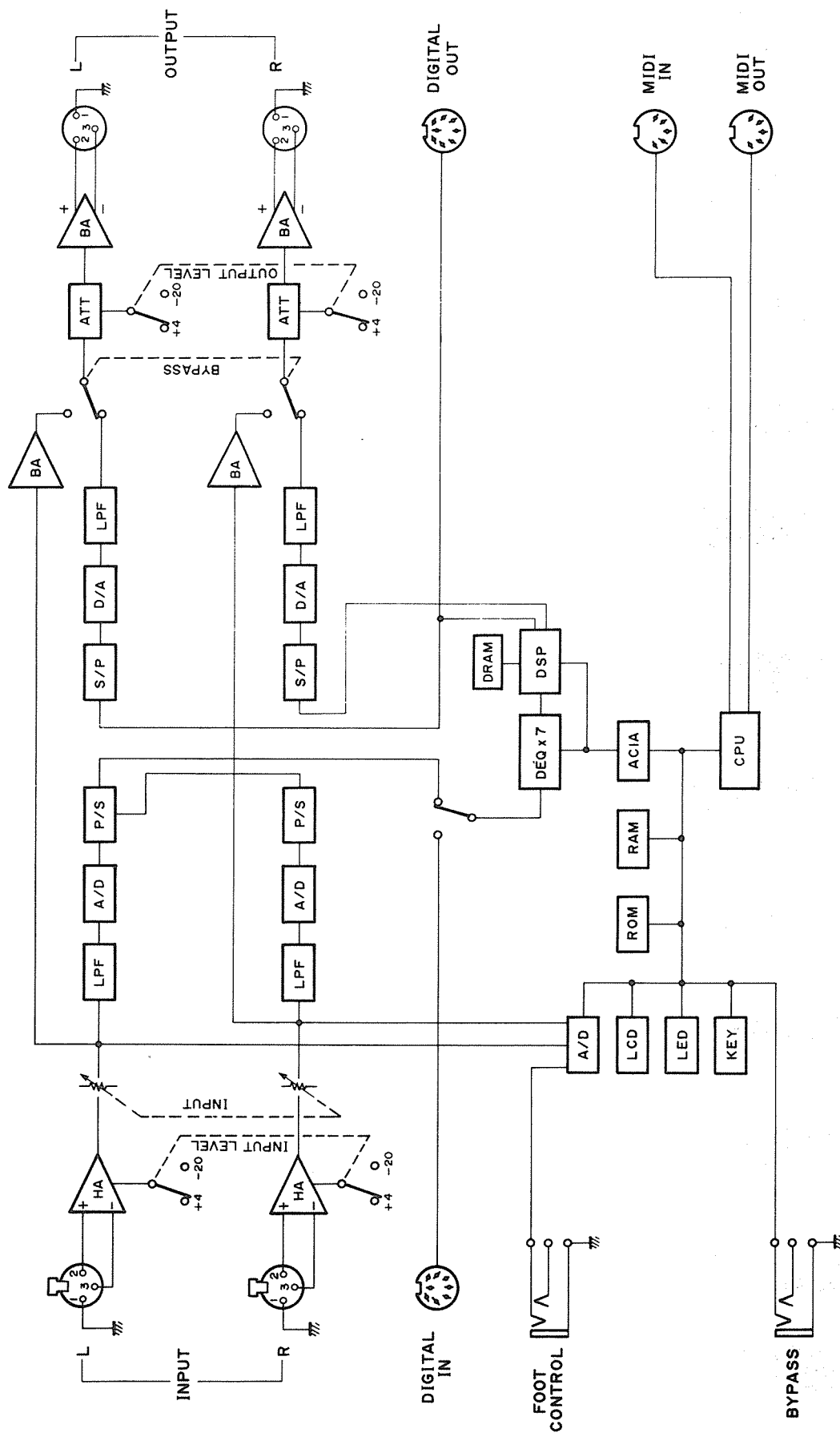
- ⑬ L/R INPUT Connectors & LEVEL Selector
- ⑮ DIGITAL I/O IN & OUT Connectors
- ⑭ L/R OUTPUT Connectors and LEVEL Selector
- ⑯ MIDI IN & OUT Connectors

DIMENSIONS

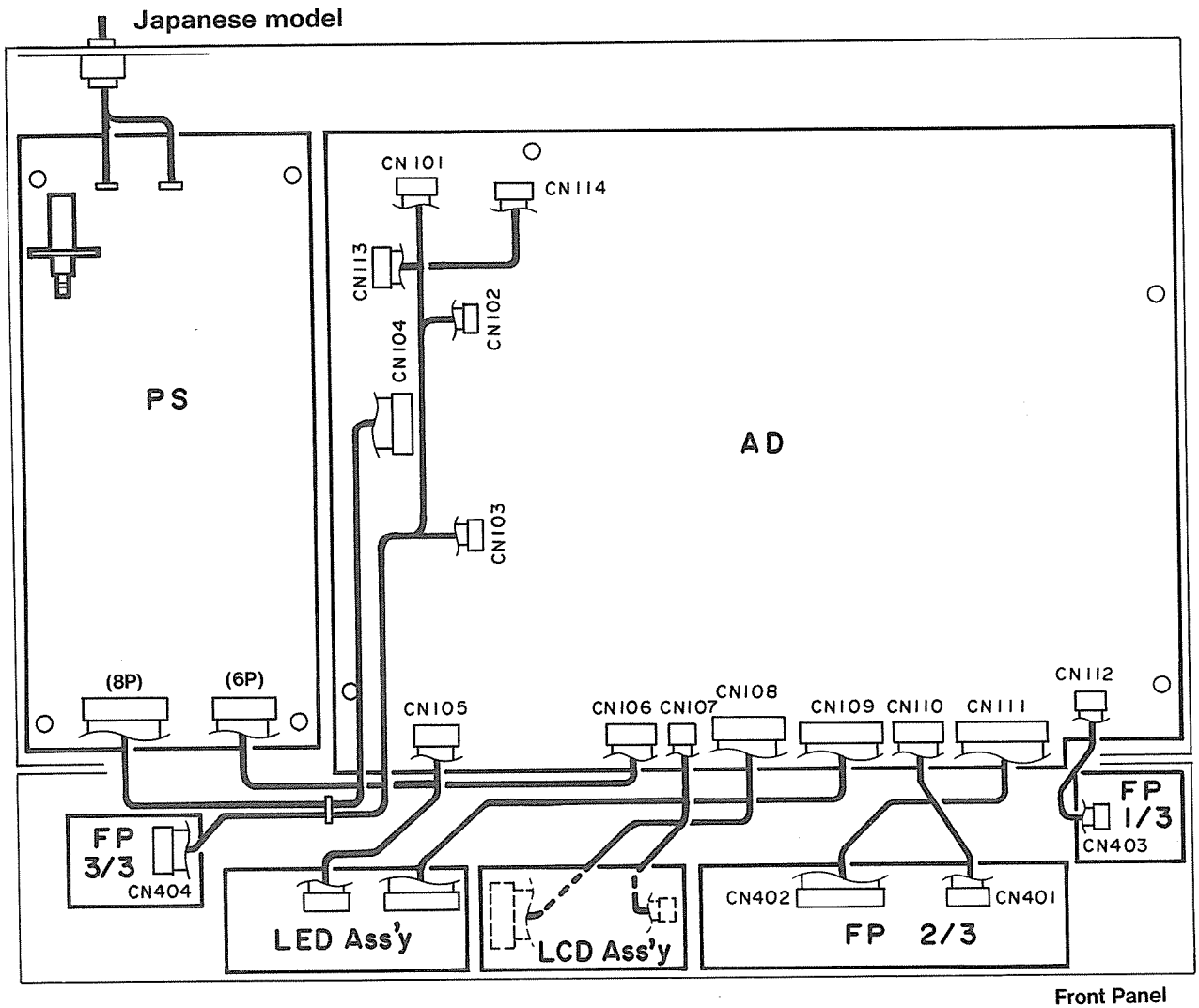


Unit : mm. (Inch)

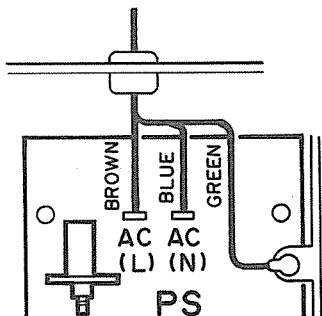
BLOCK DIAGRAM



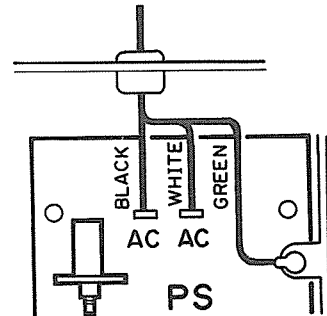
CIRCUIT BOARD LAYOUT & WIRING



North European and West Germany models



U.S. and Canadian models



LSI DATA TABLE

●HD6303RP (IG093500) CPU

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{ss}		Ground	21	V _{cc}		+5V
2	XTAL	I	Clock	22	A15	O	Address bus
3	EXTAL	I		23	A14	O	
4	NMI	I	Non-maskable Interrupt	24	A13	O	
5	IRQ1	I	Interrupt Request	25	A12	O	
6	RESET	I	Reset	26	A11	O	
7	STBY	I	Stand-by mode Signal	27	A10	O	
8	P20	I/O	Port	28	A9	O	(Data bus /) Address bus
9	P21	I/O		29	A8	O	
10	P22	I/O		30	D7/A7	I/O	
11	P23	I/O		31	D6/A6	I/O	
12	P24	I/O		32	D5/A5	I/O	
13	A0/P10	I/O	Address bus (/ Port)	33	D4/A4	I/O	
14	A1/P11	I/O		34	D3/A3	I/O	
15	A2/P12	I/O		35	D2/A2	I/O	
16	A3/P13	I/O		36	D1/A1	I/O	
17	A4/P14	I/O		37	D0/A0	I/O	
18	A5/P15	I/O		38	R/W	O	Read/Write control
19	A6/P16	I/O		39	AS	O	Address strobe
20	A7/P17	I/O		40	E	O	Enable

●HD6350P (IG132700) Asynchronous Communications Interface Adapter

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	V _{ss}		DC supply 0V	13	R/W	I	Read/Write
2	Rx Data	I	Receive data	14	E	I	Enable
3	Rx CLK	I	Receive clock	15	D7	I/O	Data bus
4	Tx CLK	O	Transmit clock	16	D6	I/O	
5	RTS	I/O	Request to send	17	D5	I/O	
6	Tx Data	O	Transmit data	18	D4	I/O	
7	IRQ	I	Interrupt request	19	D3	I/O	
8	CS0	I	Chip select	20	D2	I/O	
9	CS2	I		21	D1	I/O	
10	CS1	I		22	D0	I/O	
11	RS	I	Resist select	23	DCD	I	Data carrier detect
12	V _{cc}		DC supply	24	CTS	I	Clear to send

● **YM3804** (IT380400) Digital Signal Processor

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	MDAT15	I.O	Data bus	64	VSS		Ground
2	MDAT14	I.O		63	MDAT16	I.O	Data bus
3	MDAT13	I.O		62	MDAT17	I.O	
4	MDAT12	I.O		61	MDAT18	I.O	
5	MDAT11	I.O		60	MDAT19	I.O	
6	MDAT10	I.O		59	MDAT20	I.O	
7	MDAT9	I.O		58	MDAT21	I.O	
8	MDAT8	I.O		57	MDAT22	I.O	
9	MDAT7	I.O		56	MDAT23	I.O	
10	MDAT6	I.O		55	MOD0	I	MOD data input terminal
11	MDAT5	I.O		54	MOD1	I	
12	MDAT4	I.O		53	MOD2	I	
13	MDAT3	I.O		52	MOD3	I	
14	MDAT2	I.O		51	MOD4	I	
15	MDAT1	I.O		50	MOD5	I	
16	MDAT0	I.O		49	MOD6	I	
17	SI1	I	Serial data input terminal	48	MOD7	I	
18	SIO	I	Serial data output terminal	47	$\overline{TC}$	I	Initial clear
19	SO1	O		46	$\overline{CE}$	I	Chip enable
20	SO0	O	Select internal ACIA synchroni- zation mode	45	CLK	I	Master clock input terminal
21	XMD	I		44	$\overline{SYNC}$	I	Input for generating SYNC signals internally
22	XCLK	I	Time-out output terminal	43	TEST1	I	Terminal for internal test. To enter test mode, connect to GND. When in use, VDD.
23	$\overline{TO}$	O	Time-out output terminal	42	TESTR	I	
24	$\overline{CRS}$	I	CD counter reset	41	MADR0	O	Address bus
25	CDO	O	CD data output terminal	40	MADR1	O	
26	CDI	I	CD data input terminal	39	MADR2	O	
27	TMI	O	Unconditionally outputs the 15th bit of the Address Shift Register	38	MADR3	O	
28	$\overline{REF}$	O	Three-state. Memory which needs refreshing.	37	MADR4	O	
29	$\overline{OE}$	O	Three-state. Connect to memory OE.	36	MADR5	O	
30	$\overline{WE}$	O	Three-state. Memory read/write signal.	35	MADR6	O	
31	$\overline{CAS}$	O	Three-state. DRAM control signal	34	MADR7	O	
32	$\overline{RAS}$	O	Three-state. DRAM control signal	33	VDD		Power supply 5V

●PCM54HP (XA566001) Digital to Analog Converter

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	Vpot		Not used	15	DA3		Bit 13
2	DA15		Bit 1 (MSB)	16	DA2		Bit 14
3	DA14		Bit 2	17	DA1		Bit 15
4	NC		Not used	18	DA0		Bit 16 (LSB)
5	DA13		Bit 3	19	VO		Voltage Output
6	DA12		Bit 4	20	FBR		Not used
7	DA11		Bit 5	21	SUM		Summing Junction
8	DA10		Bit 6	22	COM		Common
9	DA9		Bit 7	23	IO		Current Output
10	DA8		Bit 8	24	NC		Not Used
11	DA7		Bit 9	25	B.OFFSET		Off set
12	DA6		Bit 10	26	+Vcc		+15V
13	DA5		Bit 11	27	MSB Adj		Not used
14	DA4		Bit 12	28	-Vee		-15V

●YM3020(XA860001) DAC

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	CH 1	O	Sample and hold analog SW output (ch1)	9	Vss		Ground
2	SMP1	I	Sample and hold (ch1)	10	RBH	I	} Bias R
3	SMP2	I	Sample and hold (ch2)	11	RBL	I	
4	SD	I	Serial data input	12	MP	I	1/2 VD bias (Middle point)
5	Form Select	I	Input form select (1:binary 0:2's complement)	13	To Buff	O	Analog output
6	Vss		Ground	14	COM	I	Ch1 and Ch2 analog SW common input
7	CLOCK	I	Clock for shift register and timing generator	15	ICL	I	Initial clear
8	VDD		Power supply	16	CH2	O	Sample and hold analog SW output (ch2)

●YM3608 (XA895001) Digital Equalizer

Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	Vdd	I	+5V	12	Vss	I	Earth (Ground)
2	XMD	I	Alteration of Sync. (=+5V) or Asynch. (=0V) for CDI input terminal (Synch: 1:1), Asynch: 16:1)	13, 14	SI0, SI1	I	INPUT for Serial data signal
3	CRS	I	Initialized Serial Control Interface	15, 16	SO0, DO1	O	OUTPUT for Serial data signal
4	CDI	I	Inputs of μ PGM, Para, Ser. Cont. Data of Control Reg.	17	OVF	O	Detector for OVER Flow
5	CDO	O	Outputs of μ PGM, Para, Ser Cont. Data of Control Reg.	18	TEST	I	For test. Normally connecting to +5V
6	XCLK	I	In/Out clock for CDI & CDO	19	C2	O	Output is delayed Data of 2nd bit of P. Reg. by 1 bit.
7	TRG	I	Determines transmit timing of PARA. to Para. Reg. from T BFR.	20	C1	O	Output is delayed Data of 1st bit of P. Reg. by 1 bit.
8	ESL	I	Timing determination of data for External at Ext. Shift CLK	21	C0	O	Output is delayed Data of 0 bit of P. Reg. by 1 bit.
9	ELD	I	Timing determination of data for Inner at Ext. Shift CLK	22	CEMD	I	+5V: It's necessary to input 2 Byte for CE to CDI 0V: It needs not to have a data for CE to CDI
10	ECLK	I	Input Shift CLK of IN/OUT SR at Ext Shift CLK	23	IC	I	Initialized for DEQ
11	CLK	I	System Clock	24	Sync	I	Synchro. signal for system

●YM3901 (XC282001) ADA

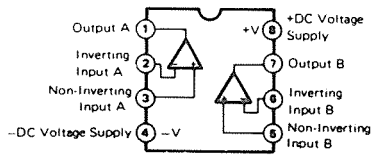
Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	MCLK	I	System clock	33	DA1	O	Outputs Parallel data 1 to DAC
2	SYNC	I	Input of system synch. signal	34	DA2	O	Outputs Parallel data 2 to DAC
3	SYO	O	Output of system synch. signal	35	DA3	O	Outputs Parallel data 3 to DAC
4	REST	I	System reset signal, except Ran. gen.	36	DA4	O	Outputs Parallel data 4 to DAC
5	DRST	I	Reset signal for Random generator	37	DA5	O	Outputs Parallel data 5 to DAC
6	MODE0	I	Selecting system mode	38	DA6	O	Outputs Parallel data 6 to DAC
7	MODE1	I		39	DA7	O	Outputs Parallel data 7 to DAC
8	MODE2	I		40	DA8	O	Outputs Parallel data 8 to DAC
9	DIC0	I	Mode selection for Diser	41	GND	I	Ground (Earth) Terminal
10	GND	I	Ground (Earth) Terminal	42	DA9	O	Outputs Parallel data 9 to DAC
11	DIC1	I	Mode selection for Diser	43	DA10	O	Outputs Parallel data 10 to DAC
12	DN	I	Selection of ser. data format (DSP/Normal)	44	DA11	O	Outputs Parallel data 11 to DAC
13	TD	I	For test, external synch. control	45	DA12	O	Outputs Parallel data 12 to DAC
14	TNC	I	Selection of ser. Input data mode at MODE 0 or 3 (Time sharing/NOT)	46	DA13	O	Outputs Parallel data 13 to DAC
15	DLY0	I	Selection of Phase lag value for DIN 1, 2	47	DA14	O	Outputs Parallel data 14 to DAC
16	DLY1	I		48	DA15	O	Outputs Parallel data 15 (MSB) to DAC
17	DIN1	I	Inputs serial data for DAC	49	CPIN	I	Inputs the output signal of comparator, at successive approximation
18	DIN2	I		50	ADCK	O	Inner successive comparating register CLOCK
19	DOUT	O	Outputs serial data after AD converting	51	SH1	O	Sample/hold signal 1, Outputs SW sel. signal at MODE 1.
20	DDO1	O	Outputs serial data of phase delay for DIN 1, 2	52	SH2	O	Sample/hold signal 2
21	DDO2	O		53	ASW1	O	(Mode 2 : Switch sel. signal)
22	DAOVC/PRIN	I	Over flow control terminal for DA. GND : OFF, 5V : ON or PRCN : 5V; Initialization of random number	54	SDEN	O	(Mode 4 : De-glitch signal 3) Outputs switch select signal
23	PRCN	I	For test, at 5V initialization of random number	55	REG2	O	Latch enable signal for data input from DIN 1, 2
24	TM1	O	Outputs timing signal	56	MPX1	O	For test, enable signal for register 2
25	D32	O	More delayed 32 bit in DIN 2 are output	57	REG1	O	For test, select data out
26	VDD	I	+ 5V DC voltage	58	VDD	I	For test, enable signal of register out
27	OVFL	O	Outputs over flow signal after AD converting (Active L)	59	MPX3	O	+ 5V DC voltage
28	PRDL	O	Outputs the timing of input for output serial ran. data from PRDO	60	DEGL11	O	For test, select signal out
29	PRDO	O	Outputs ser. random data (Two comp. data) for YM3015, 3020	61	DEGL12	O	De-glitch signal 11
30	DEG1	O	Outputs De-glitch signal	62	REG3	O	De-glitch signal 12
31	DEG2	O		63	ADCX	O	For test, enable signal for register 3
32	DAO	O	Outputs Parallel data 0 (LSB) to DAC	64	ADST	O	For test, outputs control signal of clock for successive approximation
							For test, outputs start signal for successive approximation

● ADC0844CCN (XC521001) A/D CŌNVERTER

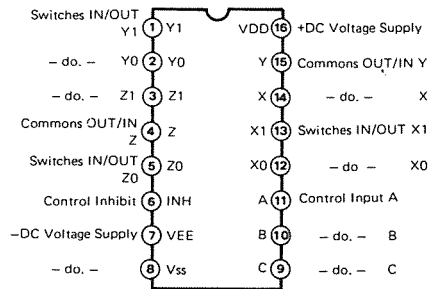
Pin No.	Name	I/O	Function	Pin No.	Name	I/O	Function
1	RD	I	Read control	11	D6	I/O	Data bus
2	CŠ	I	Chip select	12	D5	I/O	
3	CH1	I	Analog in	13	D4	I/O	
4	CH2	I		14	D3/A3	I/O	Data bus/Address bus
5	CH3	I		15	D2/A2	I/O	
6	CH4	I		16	D1/A1	I/O	
7	AG		Analog ground	17	D0/A0	I/O	
8	VREF	I	Reference voltage	18	INTR	O	Interrupt request
9	D7	I/O	Data bus	19	WR	I	Write control
10	DG		Digital ground	20	Vcc		Power supply

IC BLOCK DIAGRAM

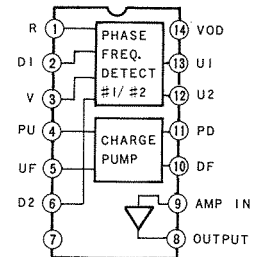
- **NJM4558DV** (IG001390)
 - **M5238P** (XA013001)
 - **NJM4556DE** (XA772001)
- Dual Operational Amplifier



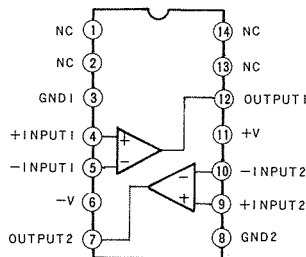
- **TC4053BP** (IG055100)
- Triple 2-Ch.
Multiplexer/Demultiplexer



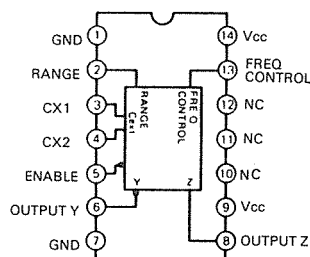
- **MC4044** (IG057900)
- Phase-Frequency



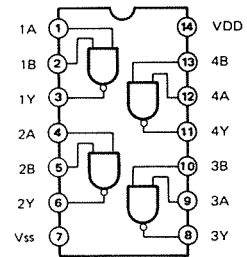
- **μPC319C** (IG086700)
- Voltage Comparator



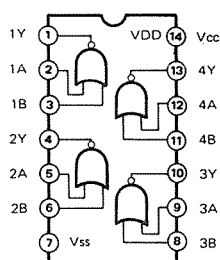
- **SN74LS624N** (IG136400)
- VCO



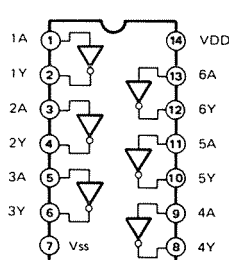
- **M74HC00P** (IG000080)
- Quad 2 Input NAND



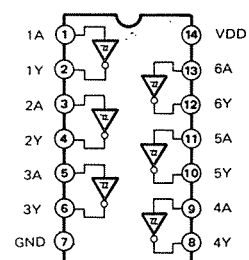
- **SN74HC02N** (IR000250)
- Quad 2 Input NOR



- **M74HC04P** (IR000480)
- Hex Inverter

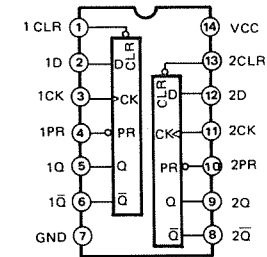


- **M74HC14P** (IR001480)
- Hex Inverter



● **M74HC74P** (IR007480)

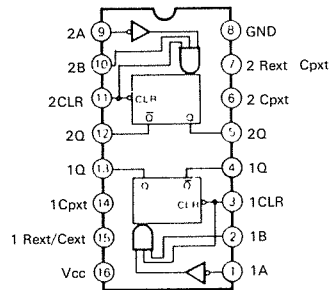
Dual D-Type Flip-Flop



INPUTS				OUTPUTS	
PR	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q _o	Q̄ _o

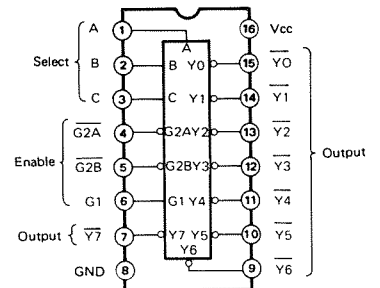
● **TC74HC123P** (IR012300)

Dual Retriggerable Single Shot



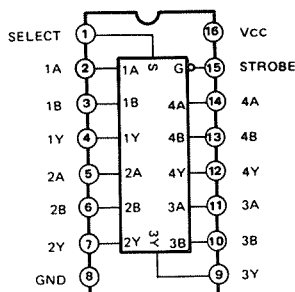
● **M74HC138P** (IR013880)

3 to 8 Demultiplexer



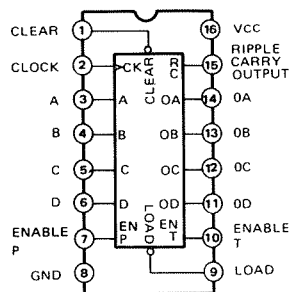
● **TC74HC157P** (IR015700)

Quad 2 to 1 Multiplexer



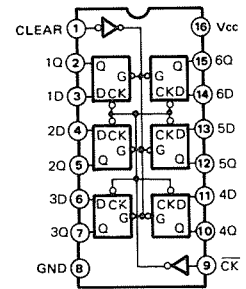
● **M74HC163P** (IR016380)

SYNC. Binary Counter



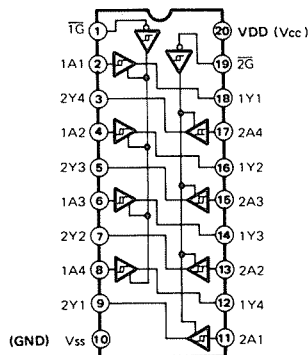
● **M74HC174P** (IR017480)

Hex D-Type Flip-Flop



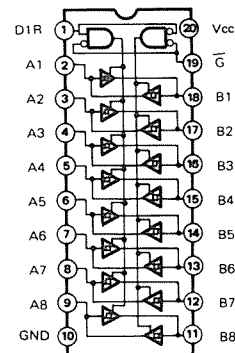
● **M74HC244P** (IR024480)

Octal 3-State Bus Buffer



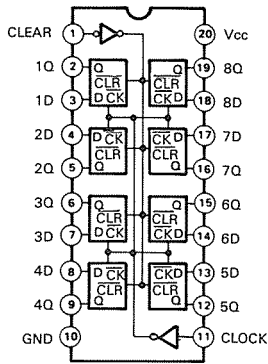
● **TC74HC245P** (IR024500)

Octal 3-State Bus Transceiver



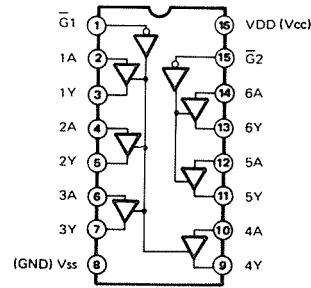
● **M74HC273P** (IR027380)

Octal D-Type Flip-Flop



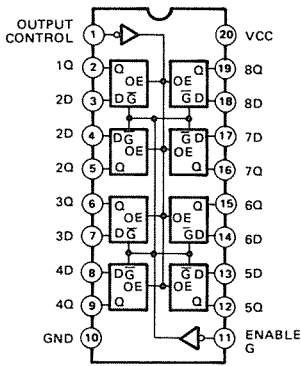
● **M74HC367** (IR036780)

Hex 3-State Bus Buffer



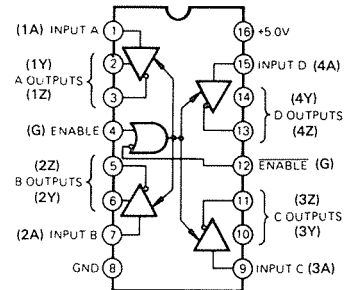
● **M74HC373P** (IR037380)

Octal 3-State D-Type Latch



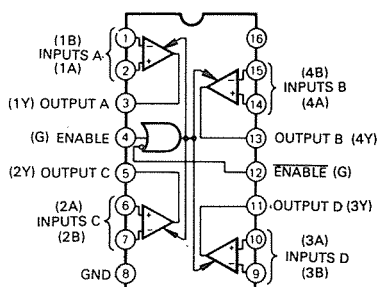
● **AM26LS31PC** (XC570001)

Line Driver



● **AM26LS32PC** (XC571001)

Line Receiver



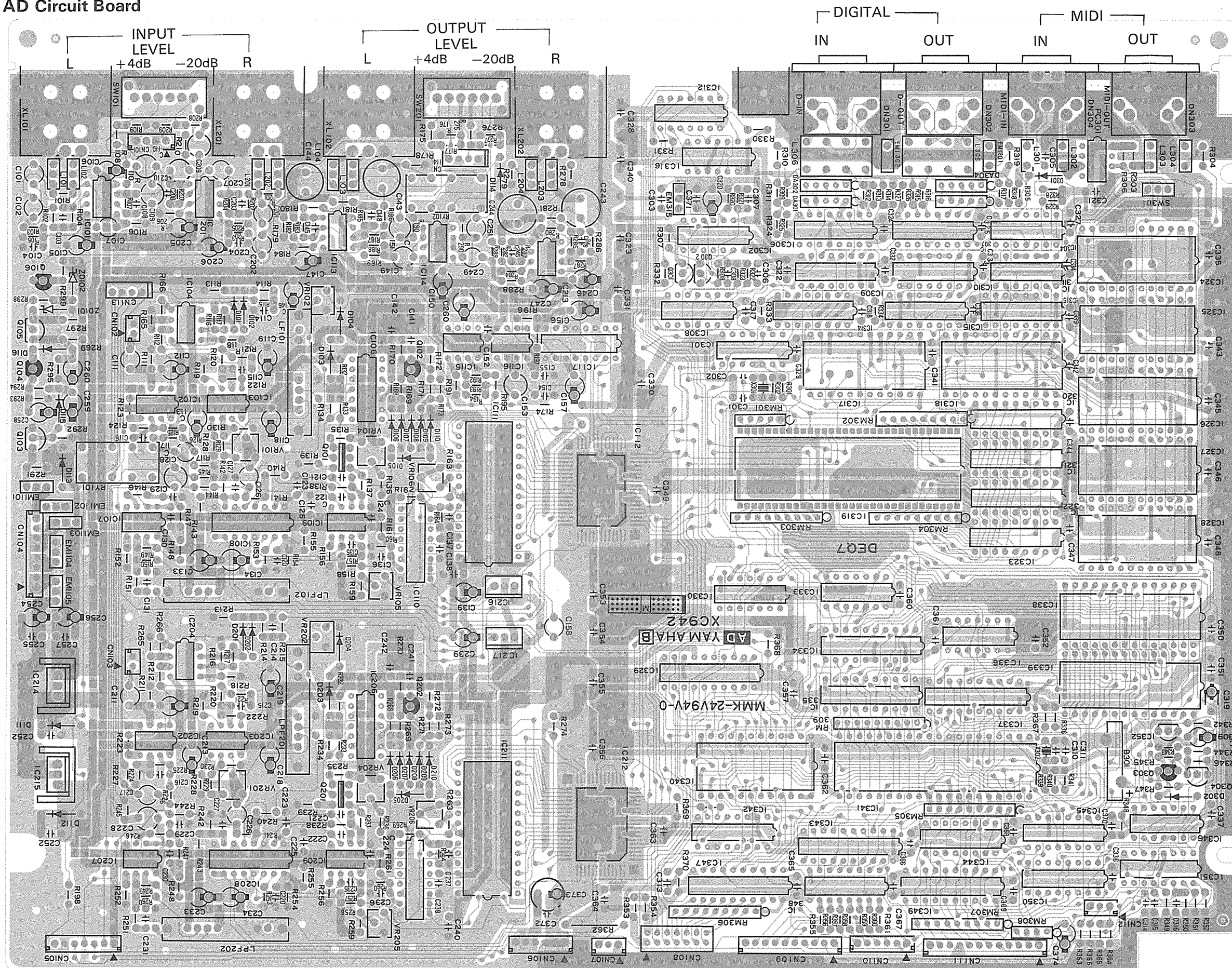
CIRCUIT BORDS

AD Circuit Board

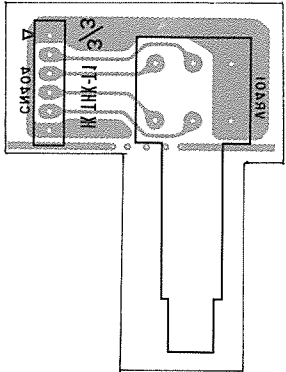
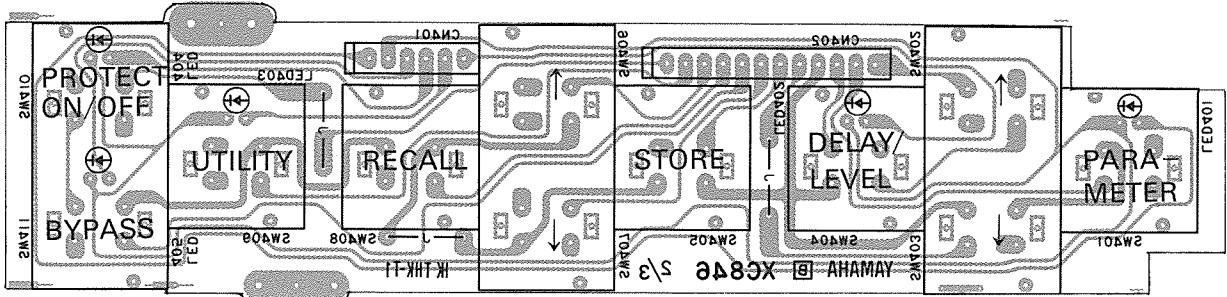
Notes)

1. Circuit Board:	XC942A0	7. Zener Diode	
		ZD101, 102	RD5 . 6EB2 5 . 6V
2. IC		8. Diode Array	
IC 101~104 , 107, 207		DA301, 303:	DAP401
114~116, 201~204:	NJM4558DV (IG001390) OP AMP.	302, 304:	DAN401 25mA
106, 206:	μ PC319C (IG086700) COMPARATOR		
108, 110, 208, 210:	TC4053BP (IG055100) MPX	9. Metal Film Resistor	
109, 209:	M5238P (XA013001) OP AMP.	R102, 104, 202, 204:	30.0K Ω 1/4W
111, 211:	PCM54HP (XA566001) DAC	103, 105, 203, 205:	15.0K Ω 1/4W
112, 212:	YM3901 (XC282001) ADA	137, 237:	7.5K Ω 1/4W
113, 213:	NJM4556DE (XA772001) OP AMP.	180, 181, 280, 281:	120.0 Ω 1/4W
117:	YM3020 (XA860001) DAC	182, 186, 282, 286:	11.0K Ω 1/4W
214:	μ PC7815H (IG063900) 15V1A	183, 185, 283, 285:	10.0K Ω 1/4W
215:	μ PC7915H (IG077500) -15V1A	184, 187, 284, 287:	5.1K Ω 1/4W
216:	NJM7808FA (XD801001) REGULATOR	188, 189, 288, 289:	4.7K Ω 1/4W
217:	NJM7908FA (XD802001) REGULATOR		
301, 304, 311, 330:	M74HC04P (IR000480) INV	10. Metal Oxide Resistor	
302:	SN74LS624N (IG136400) VCO	R362:	6.8 Ω 1W
306:	AM26LS32PC (XC571001) Line Receiver		
307:	AM26LS31PC (XC570001) Line Driver	11. Resistor Array	
308:	MC4044 (IG057900) F . DETECT	RM301:	RMLS4
309:	TC74HC157P (IR015700) DATA-SE	302~304, 306, 307:	RMLS8-103J
310, 314, 315:	M74HC163P (IR016380) CNT	305, 309:	RMLS8-472J
312:	M74HC00P (IR000080) NAND	308:	RMLS3-103J
313, 342:	TC74HC123P (IR012300) MONO-FF		
316, 336:	M74HC74P (IR007480) DFF	12. Trimmer Potentiometer	
317, 318, 324~328:	YM3608 (XA895001) DEQ	VR101, 104, 201, 204:	B30.0K 3P EVN
319:	YM3804 (IT380400) DSP	102, 105, 202, 205:	B10K 3P POT
320~323:	MB81464-12 (XA457001) DRAM 256K	106, 206:	B3.0K 3P EVN
329:	ADC0844CCN (XC521001) A/D CONVERTER		
333:	SN74HC02N (IR000250) NOR	13. Monolithic Cera. Cap.	
334:	TBP28L22N (XD468001) BPROM 256K	C312, 313:	1.5 μ F 25V
335, 337:	M74HC373P (IR037380) D-LATCH		
338:	(XD467B00) EPROM	14. FL Coil	
339:	TC5565L-12, 15 (IG148500) SRAM 64K	L101~104, 201~204	
340:	HD6350P (IG132700) Interface	301~304:	FL5R200QNT 20 μ H
341:	HD6303RP (IG093500) 8BIT CPU	305, 306:	D-08C2 15 μ H
343:	M74HC273P (IR027380) DFF		
344:	M74HC367 (IR036780) BUS . DRIV	15. EMI Filter	
345:	M74HC138P (IR013880) DECO-8	EM101~105,301,302,315 :	LS MT Y223NB
346:	M74HC14P (IR001480) INV $\times$ 6		
347:	TC74HC245P (IR024500) BUS . BUF	16. Active Low Pass Filter	
349:	M74HC244P (IR024480) BUS . BUF	LPF101, 102, 201, 202:	LP20C9B6
350:	M74HC174P (IR017480) D . FF		
352:	PST518A (IG124300) RESET	17. Ceramic Resonator	
		X301:	5.6448MHz
3. Photo Coupler		302:	4.0MHz
PC301:	TLP552 (IK000470)		
4. Transistor		18. Slide Switch	
Q101, 201:	2SC3064 F, G	SW101, 201:	HSW0273-01-220
102, 104, 106, 202, 303:	2SA1015 Y		
103, 105, 301, 302, 304:	2SC1815 Y	19. Din Jack	
5. Transistor Array		DN301, 302:	5P TCS4650
IC348:	TD62506P	303, 304:	8P TCS4680
351:	TD62003P		
6. Diode		20. Relay	
D101~110, 201~210		RY101, 102:	DC RZ-12 12V
301, 302:	1SS176		
111, 112:	11ES4	21. Connector	
113~116:	1SS133	XL101, 201 :	XLB-3-31 IN
		102, 202 :	XLB-3-32 OUT

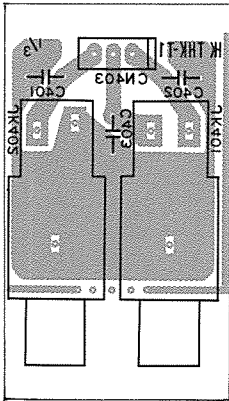
●AD Circuit Board



● FP Circuit Board



Pattern side



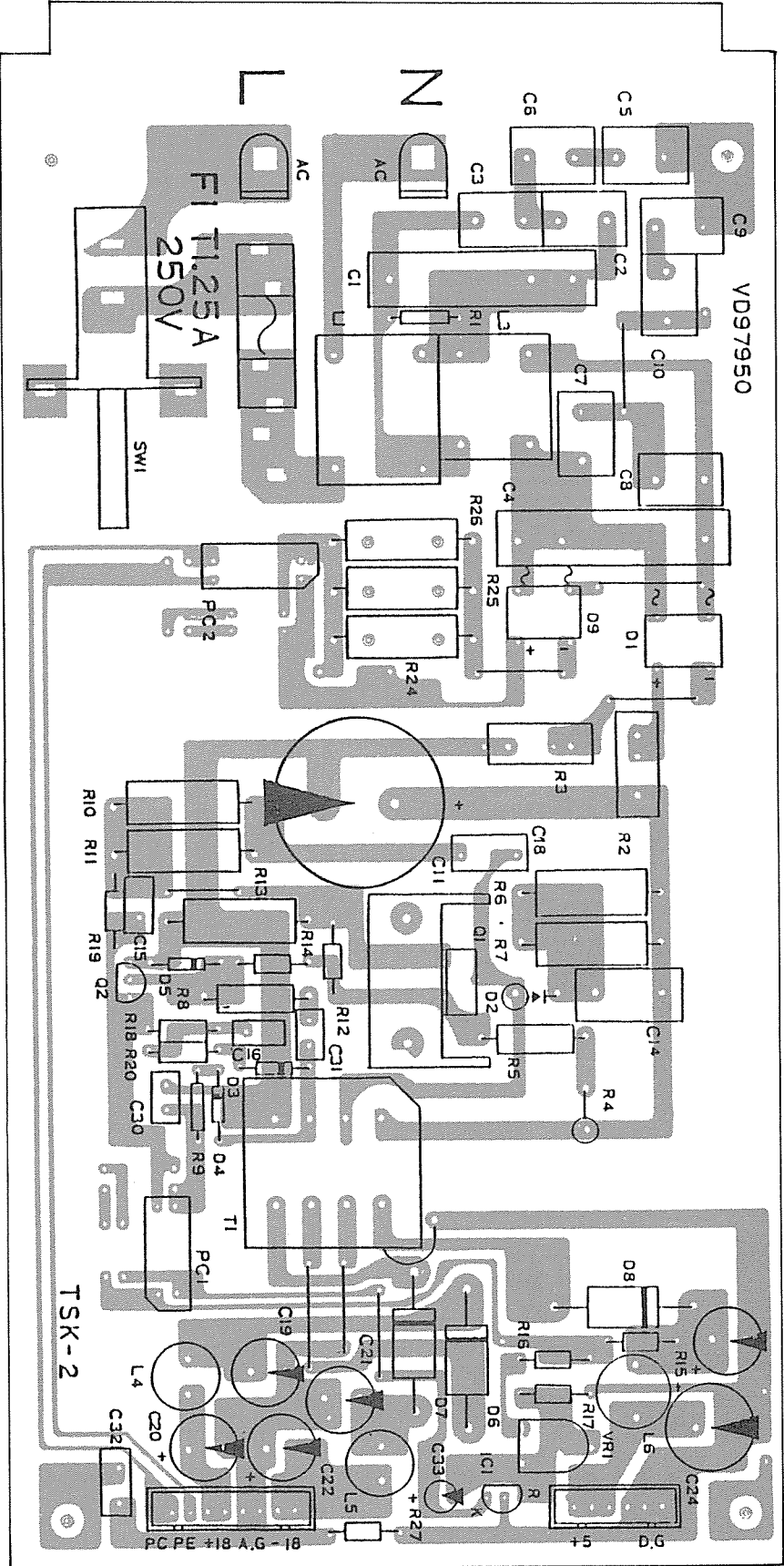
Pattern side

Notes)

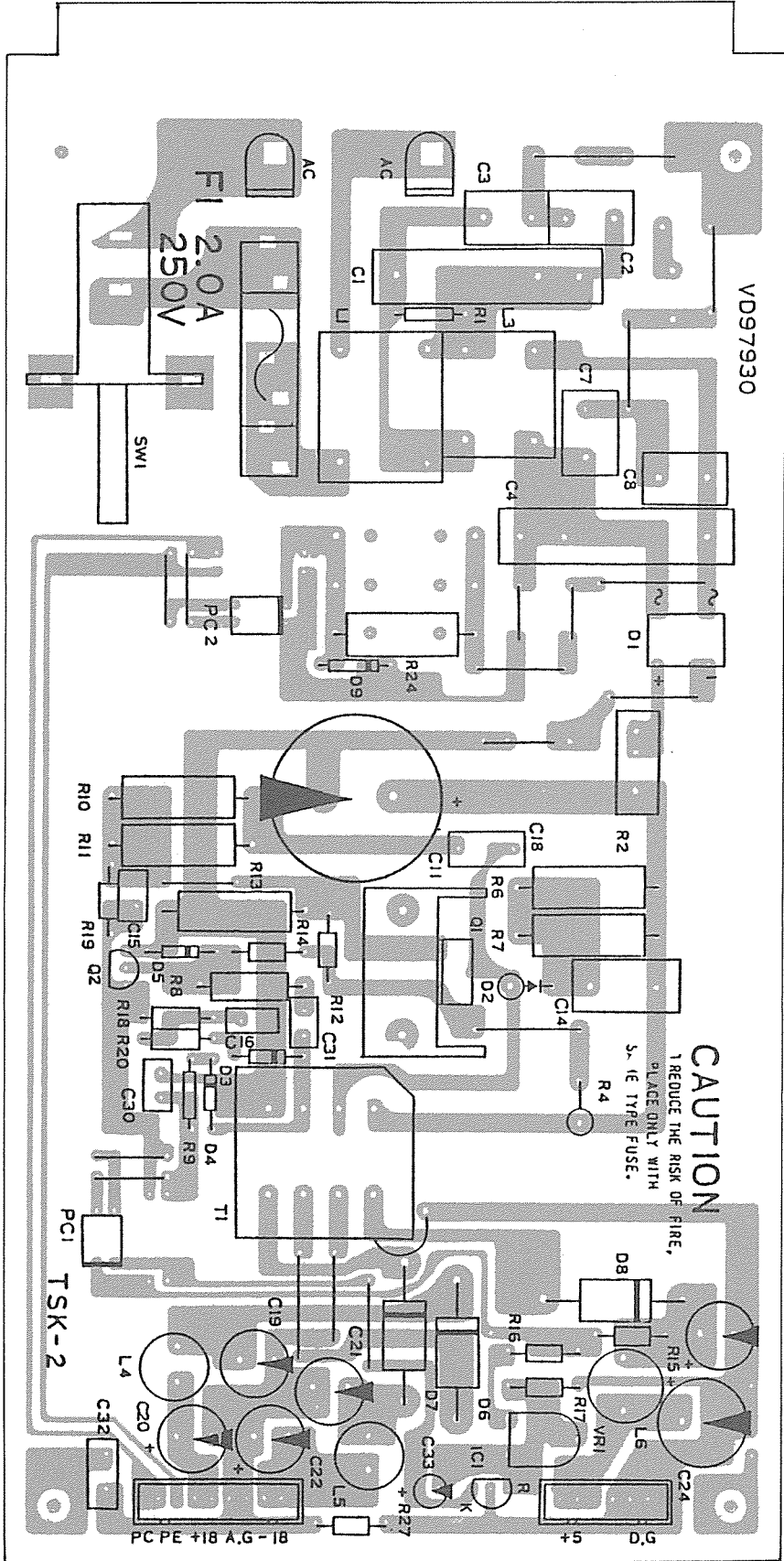
- | | | |
|---|-----------------|----------|
| 1. Circuit Board: | XC846B0 | |
| 2. LED
LED401~405: | LN242RP RED | |
| 3. Rotary Pot
VR401: | A10.0K PK124221 | |
| 4. Semiconductive Cera. Cap.
C401~403: | 0.1 μ F 25V | |
| 5. Push Switch
SW401~411: | KHH10908 | |
| 6. Phone Jack
JK401: | HLJ0544 | STEREO |
| 402: | HLJ0544 | MONAURAL |

● Power Supply Unit

● European model

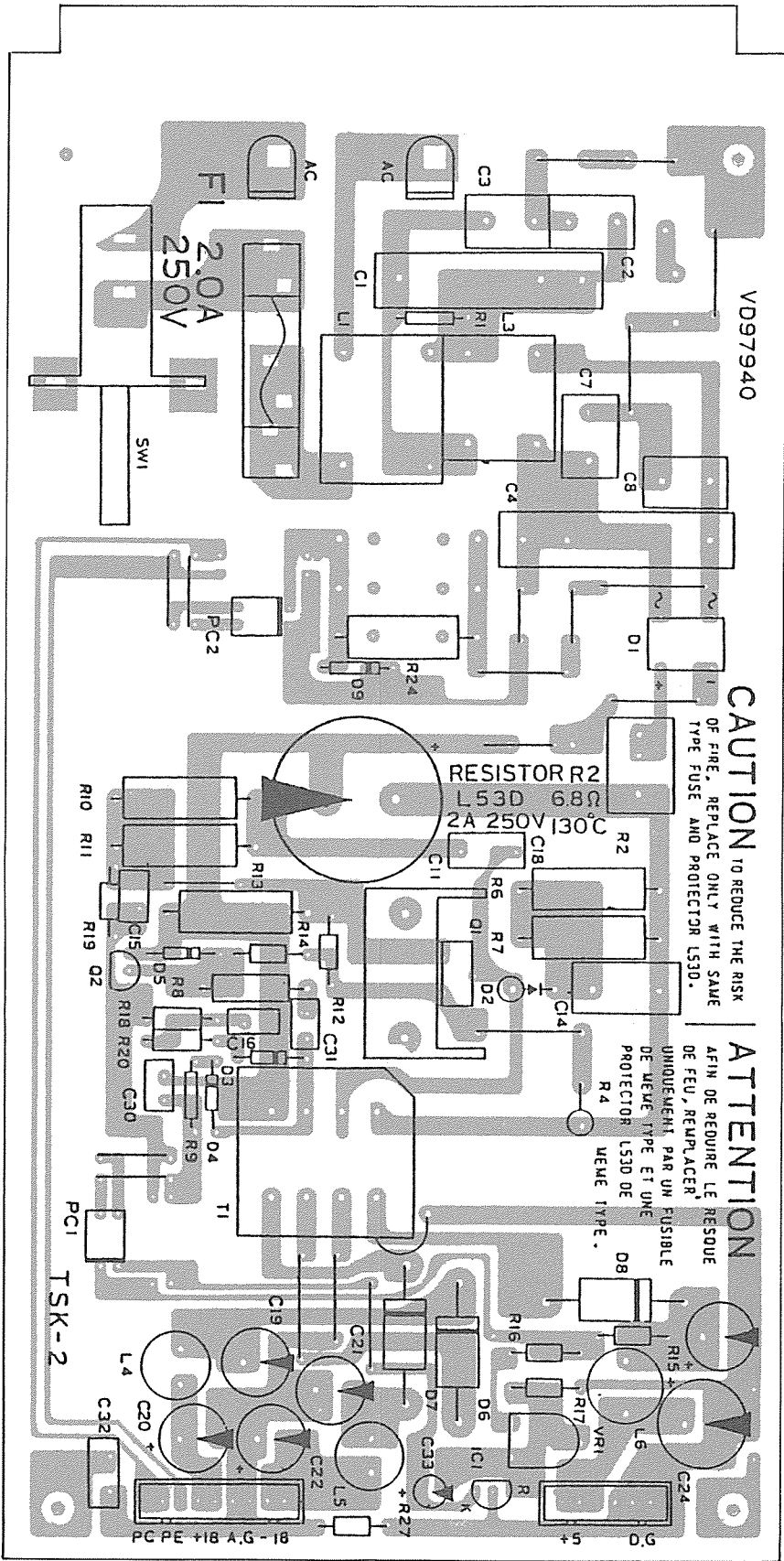


● U.S. model



YG-4047-014 △ : European model
YG-4047-012 △ : U.S.model
YG-4047-013 △ : Canadian model

● Canadian model



components side

Notes)

- IC
IC1: μ PC1093J (IX802360) Regulator
- Photo Coupler
PC1, 2: PC817 (IK000480) U,C
PC511 (IK000490) H,D
- Transistor
Q2 : 2SC2655
- FET
Q1: 2SK319 U,C
2SK513 H,D
- Diode
D1 : S1WB40 U,C
S1WB60 H,D
D2 : 10DF6
D3, 4: 1SS84
D6, 7: 31DF1
D8 : 31DQ04
D9 : 1SS1555 U,C
S1WB60 H,D
- Zener Diode
D5 : RD15E

Fuse

Destination	F 1
U,C	2.0A 250V ST4
H,D	1.25A 250V EAK

■ MIDI DATA FORMAT

● Transmission Data

1. System Exclusive Message

1-1 1 memory bulk data

status	1111 0000 (F0h)	SYSTEM EXCLUSIVE
ID number	0100 0011 (43h)	YAMAHA
sub status	0000 nnnn	nnnn=channel number n=0(channel no.1)— n=15(channel no.16)
format number	0111 1110 (7Eh)	UNIVERSAL BULK DUMP
byte count	0000 0001 0000 0111	
header	0100 1100 (4Ch) "L" 0100 1101 (4Dh) "M" 0010 0000 (20h) " " 0010 0000 (20h) " " 0011 1000 (38h) "8" 0011 0011 (33h) "3" 0011 0101 (35h) "5" 0011 0110 (36h) "6" 0100 1101 (4Dh) "M" ;memory parameter data 0mmm mmmm	mmmmmmm=memory number m=1(memory no.1)— m=90(memory no.90),
data	0000 dddd 0000 dddd : : 0000 dddd 0000 dddd	1st byte 2nd byte 124th byte 125th byte
check sum	0eee eeee	
EOX	1111 0111 (7 (F7h)	END OF EXCLUSIVE

1-2 1bank program change assignment table bulk data

status	1111 0000 (F0h)	SYSTEM EXCLUSIVE
ID number	0100 0011 (43h)	YAMAHA
sub status	0000 nnnn	nnnn=channel number n=0(channel no.1)— n=15(channel no.16)
format number	0111 1110 (7Eh)	UNIVERSAL BULK DUMP
byte count	0000 0001 0000 1010	
header	0100 1100 (4Ch) "L" 0100 1101 (4Dh) "M" 0010 0000 (20h) " " 0010 0000 (20h) " " 0011 1000 (38h) "8" 0011 0011 (33h) "3" 0011 0101 (35h) "5" 0011 0110 (36h) "6" 0101 0100 (54h) "T" ;table data 0bbb bbbb	bbbbbbb=bank number
data	0ddd dddd 0ddd dddd : : 0ddd dddd 0ddd dddd	1st byte 2nd byte 127th byte 128th byte
check sum	0eee eeee	
EOX	1111 0111 (F7h)	END OF EXCLUSIVE

1-3 60memory & All banks bulk data

status	1111 0000 (F0h)	
	:	memory31
EOX	1111 0111 (F7h)	:
	:	:
status	1111 0000 (F0h)	:
	:	memory90
EOX	1111 0111 (F7h)	:
status	1111 0000 (F0h)	:
	:	bank 1
EOX	1111 0111 (F7h)	:
	:	:
status	1111 0000 (F0h)	:
	:	bank4
EOX	1111 0111 (F7h)	:

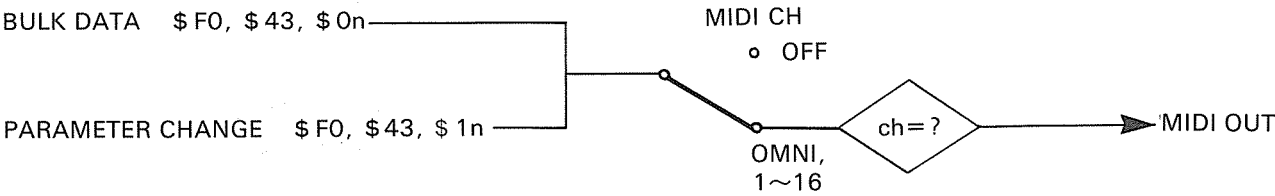
2. Parameter Change

Status	1111 0000 (F0h)	SYSTEM EXCLUSIVE	
ID number	0100 0011 (43h)	YAMAHA	
sub status	0001 nnnn	nnnn=channel number	n=0 (channel no.1) — n=15 (channel no.16)
parameter group	Oggg gghh	※ 1	
parameter number	0ppp pppp		
data	0000 dddd		
	0000 dddd		
EOX	1111 0111 (F7h)	END OF EXCLUSIVE	

※ 1

gggg	hh	ppppppp	dddd dddd	description
	0	0	0-255	L DELAY code
		1	0-255	R DELAY code
		2	0-100	L OUT LEVEL
		3	0-100	R OUT LEVEL
		4+0		parameter 1
		:	:	:
		:	:	:
		:	:	:
		4+41		parameter 42

●Transmission Conditions



● Reception Data

1. SYSTEM EXCLUSIVE MESSAGE

1-1 1 memory bulk data

Same as "1 memory bulk data" in "Transmission Data" section.

1-2 1 bank program change assignment table bulk data

Same as "1 bank program change assignment table bulk data" in "Transmission Data" section.

1-3 60 memory & All banks bulk data

Same as "60 memory & All banks bulk data" in "Transmission Data" section.

1-4 1 memory bulk dump request

status	1111 0000 (F0h)	SYSTEM EXCLUSIVE
ID number	0100 0011 (43h)	YAMAHA
sub status	0010 nnnn	nnnn=channel number n=0 (channel no. 1) – n=15 (channel no. 16)
format number	0111 1110 (7Eh)	UNIVERSAL BULK DUMP REQUEST
header	0100 1100 (4Ch)	"L"
	0100 1101 (4Dh)	"M"
	0010 0000 (20h)	" "
	0010 0000 (20h)	" "
	0011 1000 (38h)	"8"
	0011 0011 (33h)	"3"
	0011 0101 (35h)	"5"
	0011 0110 (36h)	"6"
	0100 1101 (4Dh)	"M" ; memory parameter data
	0mmm mmmm	mmmmmmm=memory number m=1 (memory no. 1) – m=90 (memory no. 90),
	1111 0111 (F7h)	END OF EXCLUSIVE

1-5 1 Bank program Change assignment table bulk dump request

status	1111 0000 (F0h)	SYSTEM EXCLUSIVE
ID number	0100 0011 (43h)	YAMAHA
sub status	0010 nnnn	nnnn=channel number n=0 (channel no. 1) – n=15 (channel no. 16)
format number	0111 1110 (7Eh)	UNIVERSAL BULK DUMP REQUEST
header	0100 1100 (4Ch)	"L"
	0100 1101 (4Dh)	"M"
	0010 0000 (20h)	" "
	0010 0000 (20h)	" "
	0011 1000 (38h)	"8"
	0011 0011 (33h)	"3"
	0011 0101 (35h)	"5"
	0011 0110 (36h)	"6"
	0101 0100 (54h)	"T" ; table data
	0bbb bbbb	bbbbbbb=bank number b=1-4
	1111 0111 (F7h)	END OF EXCLUSIVE

2. Parameter change

Same as "Parameter Change" in "Transmission Data" section.

2. NOTE ON

status	1001 nnnn	nnnn=channel number	n=0 (channel no. 1)— n=15 (channel no. 16)
1st data	0kkk kkkk	kkkkkkkk=note number	
2nd data	0vvv vvvv	vvvvvvvv=velocity	

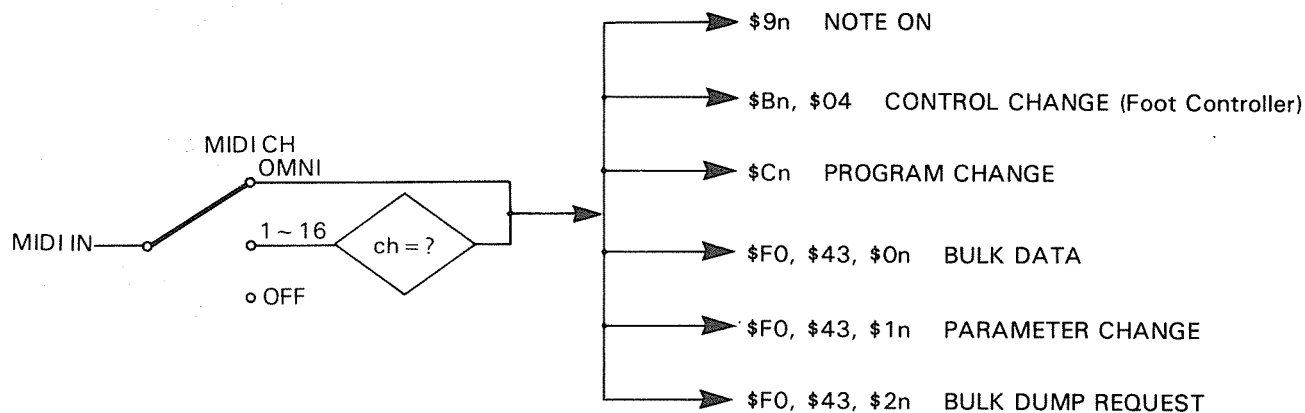
3. CONTROL CHANGE Foot Controller

status	1011 nnnn	nnnn=channel number	n=0 (channel no. 1)— n=15 (channel no. 16)
1st data	0000 0100	control number=4 (Foot Controller)	
2nd data	0vvv vvvv	vvvvvvvv=control value	

4. PROGRAM CHANGE

status	1100 nnnn	nnnn=channel number	n=0 (channel no. 1)— n=15 (channel no. 16)
data	0ppp pppp	pppppppp=program number	p=0 (program no. 1)— p=127 (program no. 128)

● Reception Conditions



Function ...		Transmitted	Recognized	Remarks
Basic Default		x	1 - 16, off	memorized
Channel Changed		x	1 - 16, off	
Mode Default		x	OMNION/OMNIOFF	memorized
Mode Messages		x	x	
Mode Altered		*****	x	
Note		x	0 - 127	
Number : True voice		*****	x	
Velocity Note ON		x	x	
Note OFF		x	x	
After Key's		x	x	
Touch Ch's		x	x	
Pitch Bender		x	x	
Control	4	x	o	Foot Controller
Change				
Prog		x	o 0 - 127 *1	
Change : True #		*****		
System Exclusive		o	o	Bulk dump
System : Song Pos		x	x	
: Song Sel		x	x	
Common : Tune		x	x	
System : Clock		x	x	
Real Time : Commands		x	x	
Aux : Local ON/OFF		x	x	
: All Notes OFF		x	x	
Mes- : Active Sense		x	x	
sages: Reset		x	x	
Notes: *1 For program 1 - 128, memory #1 - #90 is selected.				

■ TEST PROGRAM

1. Test Program Entry

- (1) While pressing the "DELAY/LEVEL" and "PROTECT ON/OFF" switches, turn the POWER switch on.
The data in Memory location 1 through 30 will be duplicated to Memory location 31 through 90.
- (2) While pressing the "PARAMETER" and "PROTECT ON/OFF" switches, turn the POWER switch on.
The Test Program will be activated.
The message will appear in the LCD as shown below,

TEST ACIA

and the 7-segments LED will indicate "0".

- (3) On the normal operation, when the power switch is turned on, the ROM and RAM checks will be performed automatically.
And the DEQ, DSP check will be performed too.
- (4) The test-number will be indicated in the 7-segments LED.
Select a test-number with following operation.
Pressing the "↑" (Memory Up) switch will increase the test-number, and pressing the "↓" (Memory Down) switch will decrease it.
Press the "RECALL" switch to initiate the test.
- (5) When the test 19 is activated after completion of the tests 1 through 18, the normal operation will be restored. When the test 90 is activated, the normal operation will be restored regardless of the completion of the tests.

2. TEST 1 : LCD Check

- (1) Select the test-number "1", and press the "RECALL" switch to initiate the test.
- (2) The entire LCD is turned "ON and OFF" five times.
- (3) Verify the proper lighting of all dots in the LCD.

3. TEST 2 : LED Check

- (1) Select the test-number "2", and press the "RECALL" switch to initiate the test.
- (2) The 7-segments LED will indicate the figures of "0" to "99" in sequence.
- (3) The switch LED indicators will light one after another in order of "PARAMETER", "DELAY/LEVEL", "UTILITY", "PROTECT ON/OFF" and "BYPASS".
- (4) All of the LED indicators and segments will simultaneously light ON about three seconds.
- (5) Verify the proper lighting of all LED indicators and segments.

4. TEST 3 : Switch Check

- (1) Connect the foot controller and foot switch to the FOOT CONTROL and BY-PASS jacks.
- (2) Select the test-number "3", and press the "RECALL" switch to initiate the test.
- (3) The switch number "00" will appear in the LCD as shown below.

TEST SW, JK 00

Press the switch of which the number is indicated in the LCD.

Pressing the correct switch can advance the program.

The order is as shown below;

(00) [PARAMETER]	(06) [↓] (Memory Down)
(01) [↑] (Parameter Up)	(07) [RECALL]
(02) [↓] (Parameter Down)	(08) [UTILITY]
(03) [DELAY/LEVEL]	(09) [PROTECT ON/OFF]
(04) [STORE]	(10) [BYPASS]
(05) [↑] (Memory Up)	(FC) FOOT CONTROLLER
	(BP) FOOT SWITCH

- (4) When these tests have been completed successfully, an "OK" message will appear in the LCD.
- (5) If an incorrect switch is pressed, an error message "NG" will appear in the LCD. Press the "RECALL" switch to return the routine to the procedure (2).
And press the switches again in correct order.

5. TEST 4 : MIDI Check

In this routine, it is checked if the data sent from the MIDI OUT can be received at the CPU through the MIDI IN.

- (1) Connect the MIDI IN jack to the MIDI OUT with a MIDI cable.
- (2) Select the test-number "4", and press the "RECALL" switch to initiate the test.
- (3) A result of the test will be displayed in the LCD.
when the test is OK,

TEST MIDI OK

If the output data from the MIDI OUT don't return to the CPU through the MIDI IN, nor the received data at the CPU is not correct,

TEST MIDI NG

6. TEST 5, 6 : AD OFFSET Adjustment

- (1) Connect a power amplifier and a monitor speaker to the L and R OUTPUT connectors in order to obtain sound check.
- (2) Select the test-number "5" or "6", and press the "RECALL" switch to initiate the test.

If an OFFset voltage is present, the click noise can be heard from the monitor speaker.

TEST OFFSET L (TEST5)

TEST OFFSET R (TEST6)

- (3) Adjust VR104 and VR204 on the AD circuit board to minimize the click noise level.

7. TEST7, 8: D/A Dither Adjustment

- (1) Select the test-number "7", and press the "RECALL" switch to initiate the test.

TEST DITHER LDA (TEST 7)

- (2) Adjust VR105 on the AD circuit board to minimize the noise level at the L OUTPUT connector.
- (3) Select the test-number "8", and press the "RECALL" switch to initiate the test.

TEST DITHER RDA (TEST 8)

- (4) Adjust VR205 on the AD circuit board to minimize the noise level at the R OUTPUT connector.

8. TEST9, 10: A/D Dither Adjustment

- (1) Select the test-number "9", and press the "RECALL" switch to initiate the test.

TEST DITHER LAD (TEST9)

- (2) Adjust VR102 on the AD circuit board to minimize the noise level at the L OUTPUT connector.
- (3) Select the test-number "10", and press the "RECALL" switch to initiate the test.

TEST DITHER RAD (TEST10)

- (4) Adjust VR202 on the AD circuit board to minimize the noise level at the R OUTPUT connector.

9. TEST 11—16: DRAM check

- (1) Select the tests-number "11" to "16", and press the "RECALL" switch to initiate the tests.
- (2) The message will be displayed in the LCD as shown below.

TEST DRAM XXX (example)

Test-number nn	DRAM IC Number				Display in XXX
	MSB			LSB	
11	IC322	IC323	IC320	IC321	THR
12	IC323	IC320	IC321	0000	04B
13	IC320	IC321	0000	0000	08B
14	IC321	0000	0000	0000	12B
15	1000	0000	0000	0000	-MX
16	0111	1111	1111	1111	+MX

10. TEST 17, 18: Peak/Dip Check

- (1) Select the test-number "17" or "18", and press the "RECALL" switch to initiate the test.

TEST DEQ PEAK (TEST17)

TEST DEQ DIP (TEST18)

- (2) Each peak/dip frequency of DEQ-LSIs is regulated as shown in the table.

■CHECKS

DEQ-LSI	IC328	IC327
Peak/Dip frequency	32Hz	63Hz

IC326	IC325	IC324	IC318	IC317
125Hz	250Hz	500Hz	1KHz	2KHz

- (3) When 1KHz input signals are applied to the L and R INPUT connectors, and the input signals have been adjusted so that the output signal of 0dBm is obtained at the L OUTPUT connector.
- (4) When the test 17 is activated, output signal of $+18\text{dBm} \pm 1.5\text{dB}$ at the L OUTPUT connector.
- (5) When the test 18 is activated, output signal of $-18\text{dBm} \pm 1.5\text{dB}$ at the L OUTPUT connector.

1. PREPARATIONS

1-1 Preparatory Settings

- Unless otherwise specified, the volume on the front panel and switches on the rear panel are to be set as follows:
INPUT VOL MAX
INPUT LEVEL SW101, 102 +4dB
- Each load of the OUTPUT L and R connector is to be serially connected to a load resistor(600 Ω).
- "Recall" the Memory "01" on the main program.

1-2 Measuring Instruments

- For the distortion measurement, a low-pass filter with cut-off frequency of 80 kHz and -6dB/OCT must be used.
- For the noise level measurement, a low-pass filter with the cut-off frequency of 12.7kHz and -6dB/OCT must be used.
- The output impedance of the AF signal generator must be less than 600 Ω .
- The input impedance of the measuring instruments must be over 1 M Ω .

2. INSPECTIONS

2-1 Gain

2-1-1 Total gain

When the input signals below are applied to the INPUT connector, switching of the LEVEL switch enables the output signals of the table below to be obtained at the OUTPUT L and R connectors. (After inspection, set the LEVEL switches to +4dB.)

INPUT LEVEL	OUTPUT LEVEL	INPUT	OUTPUT
+4	+4	-6dBm	$+4 \pm 1\text{dBm}$
+4	-20	-6dBm	$-20 \pm 3\text{dBm}$
-20	+4	-30dBm	$+4 \pm 3\text{dBm}$
-20	-20	-30dBm	$-20 \pm 3\text{dBm}$

(Signal Frequency: 1kHz)

2-1-2 Bypass circuit

When the BYPASS switch is switched ON according to the conditions of Table 2-1-1, output signals of $+4 \pm 2\text{dBm}$ are obtained at the L and R OUTPUT connectors.

(After inspection, set the BYPASS switch to OFF.)

2-2 Frequency Characteristics

When an input signal of approximately -10 dBm is applied from the INPUT connector in the according to the status of Table 2-1-1 and the conditions stated in section 2-1-2, the frequency characteristics of the OUTPUT L and R connectors are within the range listed in the table below. The reference frequency used is 1kHz.

	20Hz~5kHz	6kHz~19kHz	22kHz
2-1-1	± 1	± 1.5	less than -10
2-1-2	± 1	± 1.5	$+1$ -3

(dBm)

2-3 Distortion Factor

2-3-1 Maximum output distortion

With the conditions set according to Table 2-1-1, the distortion factor should be less than 0.1%.

2-3-2 Distortion factor of distortionless output

When a 1kHz input signal is applied to the INPUT connector, the distortion factor just before the clipping of the output waveforms at the L and R OUTPUT connectors should be less than -0.03% (OUTPUT waveforms can be observed by utilizing the monitor output of the distortion meter or connect an oscilloscope to the output load).

2-4 Maximum Output

When a 1kHz input signal is applied to the INPUT connector according to the

conditions of section 1-1, the maximum level of the output signal at the L and R OUTPUT connectors should be $+18.5\text{ dBm}$ with a distortion factor of less than 1%.

2-5 Meter Sensitivity

When 1kHz input signals are applied to the L and R INPUT connectors according to the conditions of section 1-1, and the input level is set to $+2.0\text{dBm}$, the "0" level of the level meter is illuminated. When the input levels are set to -3.0dBm , the "0" level is turned out.

At this point, all level except "0" and "CLIP" are illuminated.

When the input level is set to 9.0dBm , the "CLIP" of the level meter is illuminated, and when the input level is set to 8.5dBm , the "CLIP" is turned out.

When the input is opened, all level LED are turned out.

2-6 Muting Circuit

After the POWER switch is turned ON, muting is effective for three to four seconds, and no output signals are generated.

After this time delay output signals can be obtained at each OUTPUT connector.

When the POWER switch is turned OFF, muting becomes effective so that no clicking noise is generated.

2-7 Noise Level

With the same conditions as stated in 1-1, the noise levels of the L and R OUTPUT connectors are less than -70dBm .

Be sure waiting for approximately 5 minutes after the power switch is turned on, in order to make this inspection.

■ ADJUSTMENTS

1. PREPARATIONS

1-1. Preparatory Setting

- Turn the L and R INPUT volumes to minimum (0).
- Between each ④ and ⑤ pins of the L and R OUTPUT, a load resistor (600Ω) is to be serially connected. Connect each ⑤ and ⑥ pins of the L and R OUTPUT.
- Turn SW101, 102 to "+4".
- Turn VR102, 105, 106, 202, 205, 206 to minimum.

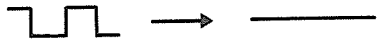
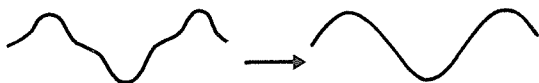
1-2. Measuring Instruments

- For the distortion measurement, a low-pass filter with cut-off frequency of 80k Hz and -6dB/OCT must be used.
- For the noise level measurement, a low-pass filter with the cut-off frequency of 12.7kHz and -6dB/OCT must be used.
- The output impedance of the AF signal generator must be less than 600Ω.
- The input impedance of the measuring instruments must be over 1MΩ.

2. ADJUSTMENTS

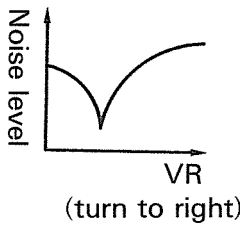
2-1. Adjustments

- Turn SW102, 103, 104, 202, 203, 204 to "ON" and SW302, 303 to "N".

Adjustment	Input Signal	Measure at	Procedure
① A/D Full Scale	Apply +9dBm/1kHz signal to each pin ④ of L and R INPUT.	CN105 —pin③, ⑤	Adjust VR101 and VR102 so that the output signal becomes 5 V.
	Apply +8.5dBm/1k Hz signal to each pin ④ of L and R INPUT.		Adjust VR101 and VR102 so that the output signal becomes 0 V.
② Total Gain	Apply +8.5dBm/1k Hz signal to each pin ④ of L and R INPUT	L and R OUTPUT —pin④	Adjust VR106 and VR206 so that the output level becomes $+18.5 \pm 1$ dBm. The output level remainder of L and R OUTPUT is to be less than 1dBm.
③ Offset	Connect each pins ④ and ⑤ of L and R INPUT.	IC111 —pin⑨ IC211 —pin⑨	Activate the Test 5 of the Test Program. Adjust VR104 and VR204 so that the wave becomes a horizontal line as shown below. 
④ MSB	Apply a sine wave signal of 1kHz to each pin ④ of L and R INPUT.	L and R OUTPUT —pin④	Adjust the input signal so that the output wave of approximately -50 dBm is obtained. If the offset adjustment has been completed, the output wave form will be distorted. Adjust VR107 and VR207 so that the output wave form becomes a sine wave as shown below. 

2-2. Dither Adjustments

● Turn SW302 and SW303 to “T”.

Adjustment	Test Program	Measure at	Output Signal	Procedure
D/A Left	7	L OUTPUT—pin $\oplus$	 (turn to right)	Adjust VR105 to minimize the noise level.
D/A Right	8	R OXTPUT—pin $\oplus$		Adjust VR205 to minimize the noise level.
A/D Left	9	L OUTPUT—pin $\oplus$		Adjust VR102 to minimize the noise level.
A/D Right	10	R OUTPUT—pin $\oplus$		Adjust VR202 to minimize the noise level.

■ DISASSEMBLY PROCEDURE

1. Removal of Top Cover (Fig. 1)

- (1) Remove the 8 screws **A** (3×8 bind head screw) and remove the top cover.

2. Removal of AD Circuit Board

- (1) Remove the top cover. (Refer to 1. Removal of Top Cover)
- (2) Remove the rear panel. (Fig. 2, 3)
 - Remove the 3 screws **B** (3×6 bind tapping screw) and 11 screws **C** (3×8 bind head screw) and 1 screw **D** (3×6 bind tapping screw) and remove the rear panel by pulling up.
- (3) Remove the 2 screws **E** (3×6 bind tapping screw) and disconnect all connectors on the AD circuit board, and remove the AD circuit board. (Fig. 2)

3. Removal of Power Supply Unit

- (1) Remove the top cover. (Refer to 1. Removal of Top Cover)
- (2) Remove the 4 screws **F** (3×6 bind tapping screw) and disconnect 2 connectors on the power supply unit, and remove the power supply unit. (Fig. 2)

4. Removal of FP Circuit Boards (1/3, 2/3, 3/3), LED Ass'y and LCD Ass'y

- (1) Remove the top cover. (Refer to 1. Removal of Top Cover)
- (2) Remove the front panel. (Fig. 2, 3)
 - Pull out the INPUT knobs.
 - Remove the 2 screws **G** (3×6 bind tapping screw) and 4 screws **H** (3×6 bind tapping screw) and remove the front panel.

4-1. Removal of FP Circuit Board 1/3

- Remove the 2 hexagonal nuts **I** (φ9) and disconnect 1 connector for the FP circuit board 3/3 on the AD circuit board, and remove the FP circuit board 3/3. (Fig. 4)

4-2. Removal of FP Circuit Board 2/3

- Disconnect 2 connectors for the FP circuit board 2/3 on the AD circuit board, and remove the FP circuit board 2/3.

4-3 Removal of FP Circuit Board 3/3

- Remove the power supply unit. (Refer to 3. Removal of Power Supply Unit)
- Remove the 1 hexagonal nut **J** (φ9) and disconnect 1 connector on the FP circuit 1/3, and

connect 1 connector on the FP circuit board 1/3, and remove the FP circuit board 1/3. (Fig. 4)

4-4 Removal of LED Ass'y

- Remove the 2 screws **K** (3×8 bind head screw) and disconnect 2 connectors on the LED ass'y, and remove the LED ass'y. (Fig. 4)

4-5 Removal of LCD Ass'y

- Remove the 2 screws **L** (2.6×5 pan head screw) and disconnect 2 connectors for the LCD ass'y on the AD circuit board, and remove the LCD ass'y. (Fig. 4)

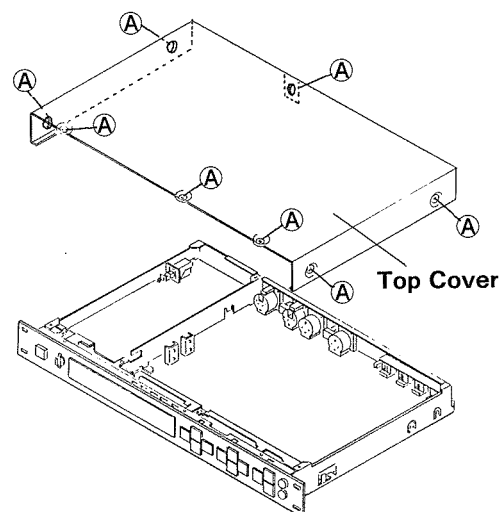


Fig. 1

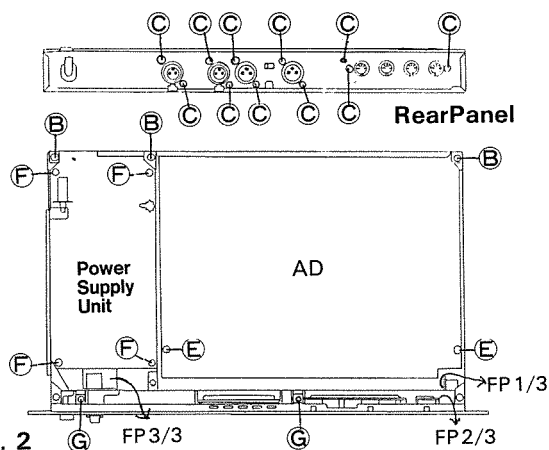


Fig. 2

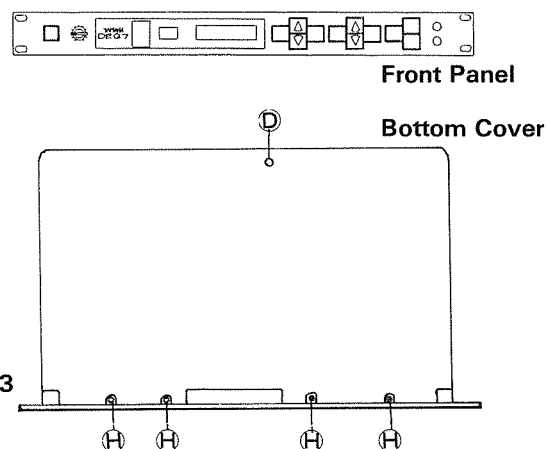


Fig. 3

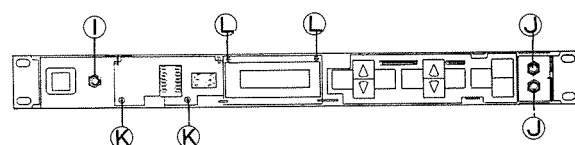


Fig. 4

Front view after removed
the front panel

Digital Equalizer



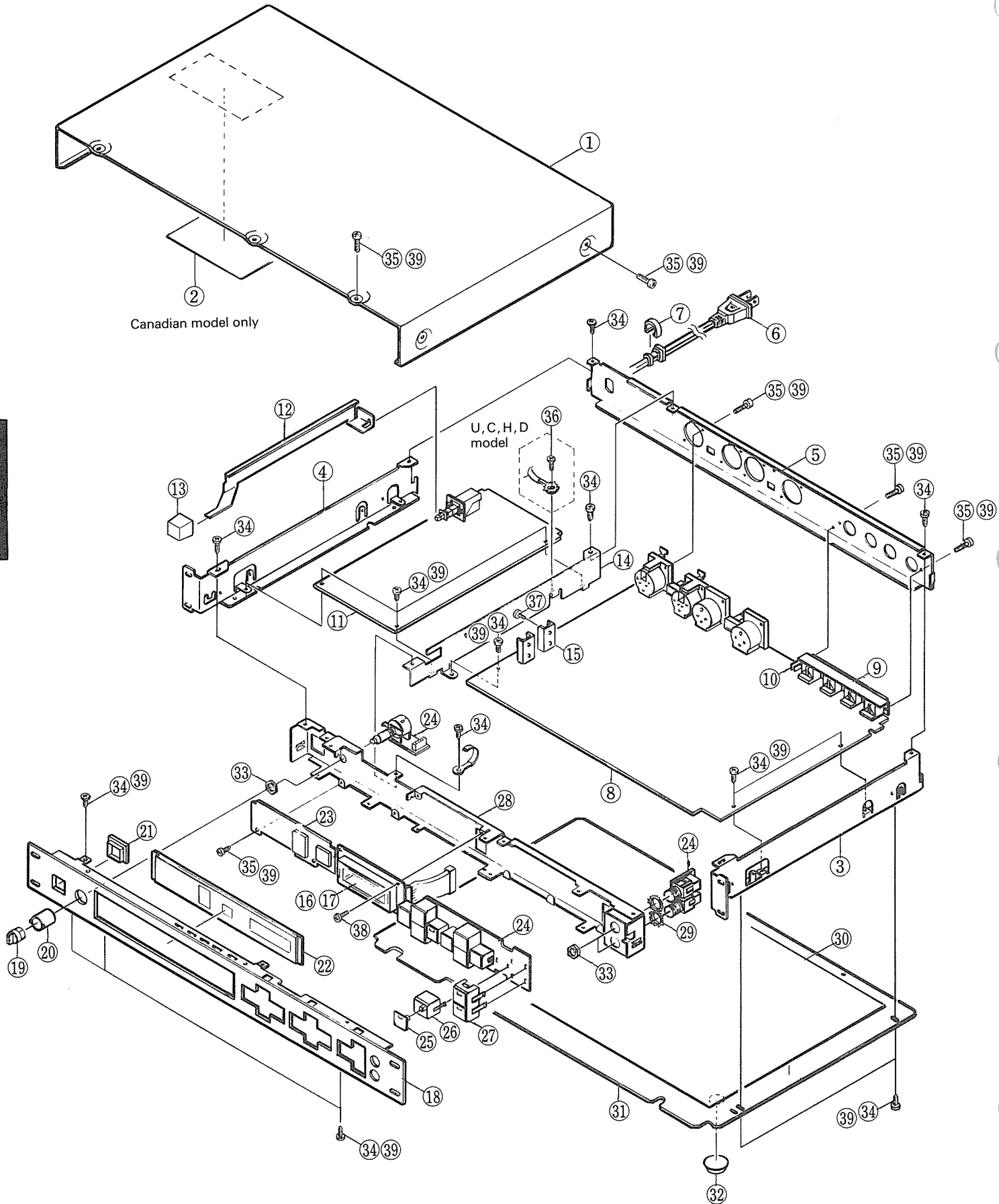
PARTS LIST

DEQ7

Notes DESTINATION ABBREVIATIONS

J : Japanese model	A : Australian model
U : U.S. model	E : European model
C : Canadian model	D : West German model
X : General model	B : British model
M : South African model	I : Indonesian model
H : North European model	

OVERALL ASSEMBLY



OVERALL ASSEMBLY

Ref	Part No	Description		部品名	Remarks	ランク
1	VD726400	Top Cover		トップカバー		09
2	VB747700	Isolation Sheet		絶縁シート	C	01
3	VD729200	Side Flame,R		サイドフレイム R		04
4	VD729500	Side Flame,L		サイドフレイム L		04
5	VD726100	Rear Panel		リアパネル	J	07
5	VD974500	Rear Panel		リアパネル	U,C	07
5	VD974600	Rear Panel		リアパネル	H,D	07
6	MG001820	AC Cord	7A 3.0M	電源コード	J	05
6	MG000270	AC Cord	10A 3.3M	電源コード	U,C	09
6	MG000450	AC Cord	6A 3.5M	電源コード	H,D	
7	VD705000	Cord Strain Relief	SR-5KN-4	コードストッパー	U,C	02
7	CB032840	Cord Strain Relief	SR-5N-4	コードストッパー	H,D	01
8	VD023300	Circuit Board	AD	ADシート		81
9	VD756700	DIN Socket Holder		DINソケットホルダー		02
10	VC719300	Terminal Plate	P-424	ターミナル金具		01
11	VD979200	Power Supply Unit		電源ユニット	J	20
11	VD979300	Power Supply Unit		電源ユニット	U	20
11	VD979400	Power Supply Unit		電源ユニット	C	20
11	VD979500	Power Supply Unit		電源ユニット	H,D	21
12	VE624200	Rod		ロッド		03
13	CB812380	Push Button		プッシュボタン		01
14	VD728800	Stay		ステー		03
15	BA011870	Heat Sink		放熱器		03
16	VA883800	LCD Assembly	16X2	LCD Ass'y		
17	VA885300	LCD Display	LCH-522-04NE-3	液晶ディスプレイ		17
18	VD726700	Front Panel		フロントパネル		11
19	VA029300	Knob		ノブ		01
20	VE186900	Knob	LOW	ノブ		02
21	VE338200	Escutcheon,Switch	(L) GY	SWエスカッション	Power	02
22	VD731200	Meter Cover		メーターカバー		07
23	VD979600	LED Assembly	LT-4087	LED Ass'y		10
24	VD968900	Circuit Board	FP	FPシート		10
25	VD377400	Key Top	PARAMETER	ノブトップキャップ		01
25	VD758400	Key Top	DELAY/LEVEL	ノブトップキャップ		
25	VD379900	Key Top	STORE	ノブトップキャップ		01
25	VD758600	Key Top	RECALL	ノブトップキャップ		
25	VD380400	Key Top	UTILITY	ノブトップキャップ		01
25	VD164800	Key Top	↑	ノブトップキャップ		01
25	VD163300	Key Top	↓	ノブトップキャップ		01
25	VD758500	Key Top	PROTECT ON/OFF	ノブトップキャップ		
25	VD380600	Key Top	BYPASS	ノブトップキャップ		01
26	VE338100	Escutcheon,Switch	(S) GY	SWエスカッション	Single	
27	VE338000	Escutcheon,Switch	(W) GY	SWエスカッション	Double	
28	VD726200	Sub Chassis		サブシャーシ		06
29	AA805820	Spacer		スペーサー		01
30	VD731100	Isolation Sheet,L		絶縁シート (L)		04
31	VE719400	Bottom Cover		ボトムカバー		07
32	CB037120	Foot		スベリ座		01
33	LX200060	Hexagonal Nut	9.0 FNM33G	特殊六角ナット		01
34	EI330066	Bind Tapping Screw	3.0X6 FCM3BL	ハインドタッピングネジ		01
35	ED330086	Bind Head Screw	3.0X8 FCM3BL	バインド小ネジ		01
36	ED340066	Bind Head Screw	4.0X6 FCM3BL	バインド小ネジ	U,C,H,D	01
37	EI330086	Bind Tapping Screw	3.0X8 FCM3BL	ハインドタッピングネジ		01
38	EA326056	Pan Head Screw	2.6X5 FCM3BL	ナベ小ネジ		01
39	EV413036	Toothed Lock Washer	A3.0 FCM3BL	歯付座金内歯形		01

*:New Parts (新規部品)

ランク:Japan Only

ELECTRICAL PARTS

Ref	Part No	Description		部 品 名	Remarks	ランク
	VD023300	Circuit Board	AD	A D シート		81
	VD968900	Circuit Board	FP	F P シート		10
	VD023300	Circuit Board	AD	A D シート		81
	XD801001	IC	NJM7808FA	I C	REGULATOR	03
	XD802001	IC	NJM7908FA	I C	REGULATOR	03
	IG001390	IC	NJM4558DV	I C	OP AMP.	03
	XA013001	IC	M5238P	I C	OP AMP.	04
	XA772001	IC	NJM4556DE	I C	OP AMP.	03
	IG063900	IC	μ PC7815H	I C	15V1A	05
	IG077500	IC	μ PC7915H	I C	-15V1A	05
	IG086700	IC	μ PC319C	I C	COMPARATOR	05
	IG055100	IC	TC4053BP	I C	MPX	05
	IG057900	IC	MC4044	I C	F.DETECT	08
	IG124300	IC	PST518A	I C	RESET	03
	IG136400	IC	SN74LS624N	I C	VCO	07
	IR000080	IC	M74HC00P	I C	NAND	01
	IR000250	IC	SN74HC02N	I C	NOR	03
	IR000480	IC	M74HC04P	I C	INV	03
	IR001480	IC	M74HC14P	I C	INV × 6	04
	IR007480	IC	M74HC74P	I C	DFF	03
	IR012300	IC	TC74HC123P	I C	MONO-FF	04
	IR013880	IC	M74HC138P	I C	DECO-8	04
	IR015700	IC	TC74HC157P	I C	DATA-SE	03
	IR016380	IC	M74HC163P	I C	CNT	04
	IR017480	IC	M74HC174P	I C	D.FF	04
	IR024480	IC	M74HC244P	I C	BUS.BUF	06
	IR024500	IC	TC74HC245P	I C	BUS.BUF	07
	IR027380	IC	M74HC273P	I C	DFF	05
	IR036780	IC	M74HC367	I C	BUS.DRIV	04
	IR037380	IC	M74HC373P	I C	D-LATCH	05
	XC570001	IC	AM26LS31PC	I C	Line Driver	05
	XC571001	IC	AM26LS32PC	I C	Line Receiver	05
	IG093500	IC	HD6303RP	I C	8BIT CPU	16
	IG132700	IC	HD6350P	I C	Interface	08
	XA895001	IC	YM3608	I C	DEQ	16
	IG148500	IC	TC5565L-12.15	I C	SRAM 64K	21
	XA457001	IC	MB81464-12	I C	DRAM 256K	12
	XD468001	IC	TBP28L22N	I C	BPROM 256K	07
	XD467B00	IC		I C	EPROM	
	IT380400	IC	YM3804	I C	DSP	17
	XA566001	IC	PCW54NP	I C	DAC	12
	XA860001	IC	YM3020	I C	DAC	09
	XC282001	IC	YM3901	I C	ADA	15
	XC521001	IC	ADC0844CCN	I C	A/D CONVERTER	09
	XC561001	Active Low Pass Filter	LP20C9B6	アクティブ L P F		08
	IK000470	Photo Coupler	TLP552	フォトカプラ		06
	IA101521	Transistor	2SA1015 Y	トランジスタ		03
	IC181520	Transistor	2SC1815 Y	トランジスタ		03
	VC845000	Transistor	2SC3064 F,G	トランジスタ		01
	IG127300	Transistor Array	TD62003P	トランジスタアレイ		04
	IG138700	Transistor Array	TD62506P	トランジスタアレイ		03
	VB481900	Diode	11ES4	ダイオード		01
	IX000760	Diode	1SS176	ダイオード		01
	IF003450	Diode	1SS133	ダイオード		01
	IF002140	Zener Diode	RD5.6EB2 5.6V	ツェナーダイオード		01
	IF007640	Diode Array	DAN401 25mA	ダイオードアレイ		03
	IF004060	Diode Array	DAP4	ダイオードアレイ		03
	HU575120	Metal Film Resistor	120.0Ω 1/4W	金属皮膜抵抗		02
	HU576470	Metal Film Resistor	4.7KΩ 1/4W	金属皮膜抵抗		02
	HU576510	Metal Film Resistor	5.1KΩ 1/4W	金属皮膜抵抗		02
	HU576750	Metal Film Resistor	7.5KΩ 1/4W	金属皮膜抵抗		02
	HU597100	Metal Film Resistor	10.0KΩ 1/4W	金属皮膜抵抗		04
	HU577110	Metal Film Resistor	11.0KΩ 1/4W	金属皮膜抵抗		02
	HU577150	Metal Film Resistor	15.0KΩ 1/4W	金属皮膜抵抗		02
	HU597300	Metal Film Resistor	30.0KΩ 1/4W	金属皮膜抵抗		03
	HL313680	Metal Oxide Resistor	6.8Ω 1W	酸化金属被膜抵抗		01
	HZ002870	Resistor Array	RMLS4	抵抗アレイ		01
	HZ004730	Resistor Array	RMLS8-103J	抵抗アレイ		02
	VB594000	Resistor Array	RMLS8-472J	抵抗アレイ		01
	VC467600	Resistor Array	RMLS3-103J	抵抗アレイ		
	VB135200	Trimmer Potentiometer	B3.0K 3P EVN	半固定ポリウム		01
	VB135500	Trimmer Potentiometer	B30.0K 3P EVN	半固定ポリウム		01
	VB844900	Trimmer Potentiometer	B10K 3P POT	半固定ポリウム		06
	FZ004110	Semiconductive Cera. Cap.	0.1μF 16V	半導体セラコン		01
	FZ005610	Monolithic Cera. Cap.	1.5μF 25V	積層セラコン		03
	VB835000	Coil	FL5R200QNT	コイル	20μH	01
	VA928400	Coil	D-08C2	コイル	15μH	05
	FZ005920	EMI Filter	LS MT Y223NB	L C フィルター E M I		02

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[illegible]

